

## Description

The 74LVT245BB is an octal transceiver designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) Pin can be used to disable the device so the buses effectively are isolated.

The device is designed for operation with a power supply range of 2.7V to 3.6V.

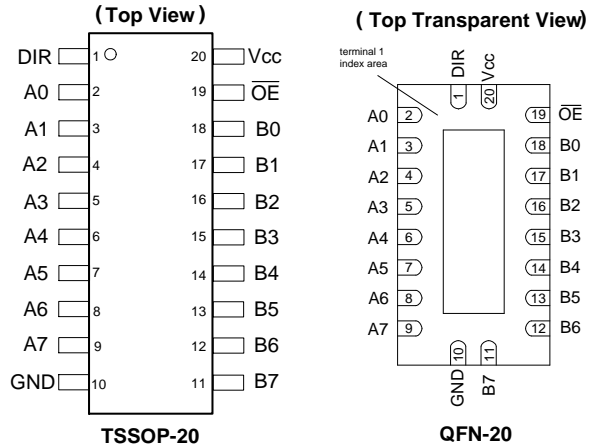
The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output preventing damaging current backflow when the device is powered down.

## Features

- Supply Voltage Range from 2.7V to 3.6V
- Outputs Sink 64mA or Source 32mA
- CMOS Low Power Consumption
- $I_{OFF}$  Supports Partial Power-Down Operation
- Inputs or Outputs Accept Up to 5.5V
- Inputs Include Bus-Hold – No Resistors on Unused Inputs.
- Inputs can be Driven by 3.3V or 5V Allowing for Mixed Voltage Applications
- Schmitt Trigger Action at All Inputs
- Outputs in 3-State During Power Up – Allows for Hot Insertion
- Outputs Have Less than 125 $\mu$ A Leakage when Forced to 5.5V
- ESD Protection Tested per JESD 22
  - Exceeds 200-V Machine Model (A115)
  - Exceeds 2000-V Human Body Model (A114)
  - Exceeds 1000-V Charged Device Model (C101)
- Latch-Up Exceeds 500mA per JESD 78, Class II
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen and Antimony free, "Green" and Lead-Free.
  3. Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Assignments

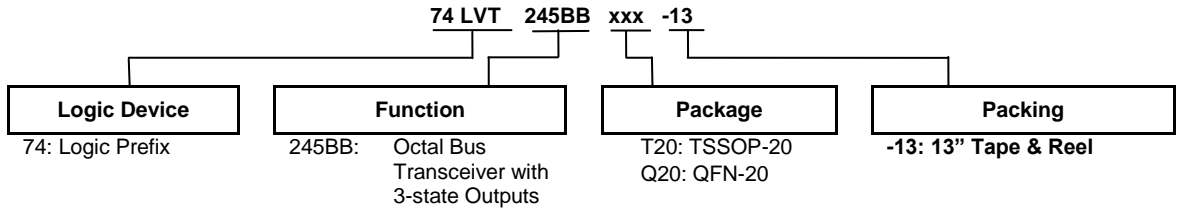


## Applications

- General Purpose Logic
- Bus Driving
- Power Down Signal Isolation
- Wide Array of Products such as:
  - Servers, PCs, Notebooks, Netbooks, Ultrabooks
  - Networking Computer Peripherals, Hard Drives, CD/DVD ROM
  - TVs, DVDs, DVRs, Set Top Boxes

NEW PRODUCT

**Ordering Information**



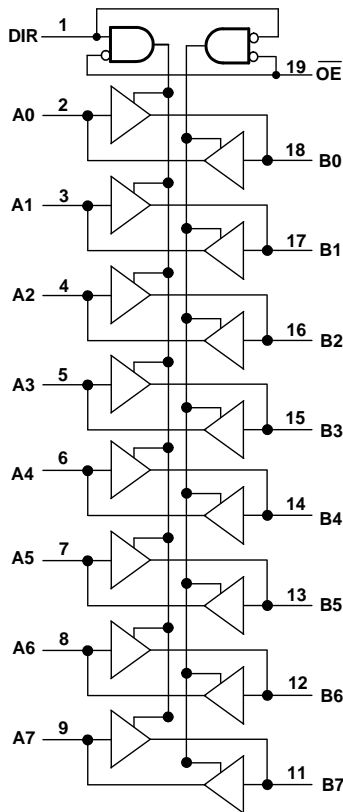
Part Number	Package Code	Package (Note 4 & 5)	Package Size	13" Tape and Reel	
				Quantity	Part Number Suffix
74LVT245BBT20-13	T20	TSSOP-20	6.4mm x 6.5mm x 1.2mm 0.65mm lead pitch	2,500/Tape & Reel	-13
74LVT245BBQ20-13	Q20	V-QFN4525-20	2.5mm x 4.5mm x 0.95mm 0.50mm lead pitch	2,500/Tape & Reel	-13

- Notes:
4. Pad layout as shown on Diodes Incorporated's package outline PDFs, which can be found on our website at <http://www.diodes.com/package-outlines.html>.
  5. V-QFN4525-20 is a JEDEC recognized naming convention that specifies the package thickness category as V and the number 4525 describes the package as 4.5mm x 2.5mm.

**Pin Descriptions**

Pin Number	Pin Name	Description
1	DIR	Direction
2	A0	Data I/O
3	A1	Data I/O
4	A2	Data I/O
5	A3	Data I/O
6	A4	Data I/O
7	A5	Data I/O
8	A6	Data I/O
9	A7	Data I/O
10	GND	Ground
11	B7	Data I/O
12	B6	Data I/O
13	B5	Data I/O
14	B4	Data I/O
15	B3	Data I/O
16	B2	Data I/O
17	B1	Data I/O
18	B0	Data I/O
19	$\overline{OE}$	Output Enable
20	V <sub>CC</sub>	Supply Voltage

**Logic Diagram**



**Function Table**

INPUTS		Operation
$\overline{OE}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Bus Isolation

**Absolute Maximum Ratings** (Notes 6 & 7)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	kV
ESD CDM	Charged Device Model ESD Protection	1	kV
ESD MM	Machine Model ESD Protection	200	V
V <sub>CC</sub>	Supply Voltage Range	-0.5 to +4.6	V
V <sub>I</sub>	Input Voltage Range (Note 7)	-0.5 to +7.0	V
V <sub>O</sub>	Output Voltage Range Output in OFF of HIGH State (Note 7)	-0.5 to +7.0	V
I <sub>IK</sub>	Input Clamp Current V <sub>I</sub> < 0V	-50	mA
I <sub>OK</sub>	Output Clamp Current V <sub>O</sub> < 0V	-50	mA
I <sub>OL</sub>	Output Current – LOW State	128	mA
I <sub>OH</sub>	Output Current – HIGH State	-64	mA
T <sub>J</sub>	Operating Junction Temperature	-40 to +150	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>TOT</sub>	Total Power Dissipation	500	mW

- Notes:
- Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.
  - Forcing the maximum allowed voltage could cause a condition exceeding the maximum current or conversely forcing the maximum current could cause a condition exceeding the maximum voltage. The ratings of both current and voltage must be maintained within the controlled range.

**Recommended Operating Conditions** (Note 8)

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	—	2.7	3.6	V
V <sub>I</sub>	Input Voltage	—	0	5.5	V
V <sub>O</sub>	Output Voltage	—	0	5.5	V
I <sub>OH</sub>	High-Level Output Current	V <sub>CC</sub> = 3.0V	—	-32	mA
I <sub>OL</sub>	Low-Level Output Current	V <sub>CC</sub> = 3.0V	—	32	mA
		V <sub>CC</sub> = 3.0V (Note 9)	—	64	
Δt/ΔV	Input Transition Rise or Fall Rate	—	—	10	ns/V
T <sub>A</sub>	Operating Free-Air Temperature	—	-40	+125	°C

- Notes:
- Unused inputs should be held at V<sub>CC</sub> or ground.
  - For I<sub>ol</sub> > 32mA the current duty cycle ≤ 50%, Frequency > 1Khz.

**Electrical Characteristics**

Symbol	Parameter	Test Conditions	V <sub>CC</sub>	T <sub>A</sub> = -40°C to +85°C			Unit	
				Min	Typical	Max		
V <sub>IK</sub>	Input Clamping Voltage	I <sub>IK</sub> = -18mA	2.7V	-1.2	-0.9	—	—	
V <sub>IH</sub>	High-Level Input Voltage	—	2.7V to 3.6V	2.0	—	—	V	
V <sub>IL</sub>	Low-Level input Voltage	—	2.7V to 3.6V	—	—	0.8	V	
V <sub>OH</sub>	High-Level Output Voltage	I <sub>OH</sub> = -100μA	2.7V to 3.6V	V <sub>CC</sub> -0.2	V <sub>CC</sub> -0.1	—	V	
		I <sub>OH</sub> = -8mA	2.7V	2.4	2.5	—		
		I <sub>OH</sub> = -34mA	3.0V	2.0	2.2	—		
V <sub>OL</sub>	Low-Level Output Voltage	I <sub>OL</sub> = 100μA	2.7V to 3.6V	—	0.1	0.2	V	
		I <sub>OL</sub> = 24mA	2.7V	—	0.3	0.5		
		I <sub>OL</sub> = 16mA	3.0V	—	0.25	0.4		
		I <sub>OL</sub> = 24mA	3.0V	—	0.3	0.5		
		I <sub>OL</sub> = 64mA	3.0V	—	0.4	0.55		
I <sub>OFF</sub>	Power Down Leakage Current	V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5V	0V	—	±1	±100	μA	
I <sub>O-Leakage</sub>	Output Leakage Current	V <sub>O</sub> = 5.5V; Output HIGH	3.6V	—	60	125	μA	
I <sub>OZPU</sub>	Power-Up I/O Leakage	V <sub>O</sub> = 0.5V to 3.0V $\overline{OE}$ = Don't Care	0V to 1.2V	—	15	±100	μA	
I <sub>OZPD</sub>	Power-Down I/O Leakage	V <sub>O</sub> = 0.5V to 3.0V $\overline{OE}$ = Don't Care	0V to 1.2 V	—	15	±100	μA	
I <sub>I</sub>	Input Current Control Pins	V <sub>I</sub> = 5.5V	0V or 3.6V	—	1	10	μA	
		V <sub>I</sub> = V <sub>CC</sub> or GND	3.6V	—	±0.1	±1		
	Input Current I/O Data Pins	V <sub>I</sub> = 5.5V	3.6V	—	1	20	μA	
		V <sub>I</sub> = V <sub>CC</sub>	3.6V	—	.1	1		
		V <sub>I</sub> = GND	3.6V	-5	-1			
I <sub>BHL</sub>	Bus Hold LOW Current	V <sub>I</sub> = 0.8V	3.0V	75	150	—	μA	
I <sub>BHH</sub>	Bus Hold HIGH Current	V <sub>I</sub> = 2.0V	3.0V	-150	-75	—	μA	
I <sub>BHLO</sub>	Bus Hold LOW Overdrive Current	V <sub>I</sub> = 3.6V	0V to 3.0V	500	—	—	μA	
I <sub>BHHO</sub>	Bus Hold HIGH Overdrive Current	V <sub>I</sub> = 3.6V	0V to 3.0V	—	—	-500	μA	
I <sub>CC</sub>	Supply Current	V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0	3.6 V	—	—	—	mA	
		Outputs HIGH		—	0.13	0.19		
		Output LOW		—	3	12		
		Outputs Disabled		—	0.13	0.19		
ΔI <sub>CC</sub>	Additional Supply Current	One Input at V <sub>CC</sub> -0.6V Others at V <sub>CC</sub> or Ground I <sub>O</sub> = 0A	3.0V to 3.6V	—	100	200	μA	
C <sub>I</sub>	Input Capacitance	Control Pins	V <sub>I</sub> = GND or V <sub>CC</sub>	0V to 3.6V	—	4	—	pF
		I/O Pins			—	10	—	

**Switching Characteristics** (Figure 1)

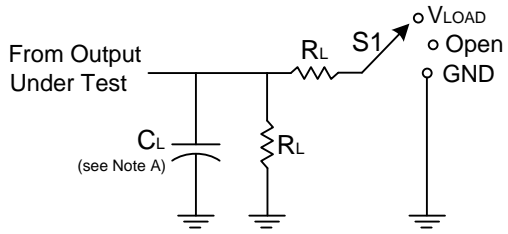
Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = -40°C to +85°C			Unit
			Min	Typ	Max	
t <sub>PLH</sub>	LOW to HIGH Propagation Delay A <sub>N</sub> to B <sub>N</sub> or B <sub>N</sub> to A <sub>N</sub>	2.7V	—	—	5.5	ns
		3.3V ± 0.3	1.2	2.4	4.8	
t <sub>PHL</sub>	HIGH to LOW Propagation Delay A <sub>N</sub> to B <sub>N</sub> or B <sub>N</sub> to A <sub>N</sub>	2.7V	—	—	4.7	ns
		3.3V ± 0.3	1.2	2.4	4.4	
t <sub>PZH</sub>	Z-State to HIGH Enable Time $\overline{OE}$ to A <sub>N</sub> or $\overline{OE}$ to B <sub>N</sub>	2.7V	—	—	8.9	ns
		3.3V ± 0.3	1.3	3.3	7.7	
t <sub>PZL</sub>	Z-State to LOW Enable Time $\overline{OE}$ to A <sub>N</sub> or $\overline{OE}$ to B <sub>N</sub>	2.7V	—	—	6.9	ns
		3.3V ± 0.3	1.7	3.2	6.4	
t <sub>PHZ</sub>	HIGH to Z-State Disable Time $\overline{OE}$ to A <sub>N</sub> or $\overline{OE}$ to B <sub>N</sub>	2.7V	—	—	6.5	ns
		3.3V ± 0.3	2.2	3.6	6.0	
t <sub>PLZ</sub>	LOW to Z-State Disable Time $\overline{OE}$ to A <sub>N</sub> or $\overline{OE}$ to B <sub>N</sub>	2.7V	—	—	5.5	ns
		3.3V ± 0.3	2.2	3.4	5.5	

**Package Characteristics**

Symbol	Parameter	Package	Test Conditions	Min	Typ.	Max	Unit
θ <sub>JA</sub>	Thermal Resistance Junction-to-Ambient	TSSOP-20	(Note 10)	—	74	—	°C/W
θ <sub>JC</sub>	Thermal Resistance Junction-to-Case	TSSOP-20	(Note 10)	—	15	—	°C/W
θ <sub>JA</sub>	Thermal Resistance Junction-to-Ambient	V-QFN4525-20	(Note 10)	—	67	—	°C/W
θ <sub>JC</sub>	Thermal Resistance Junction-to-Case	V-QFN4525-20	(Note 10)	—	20	—	°C/W

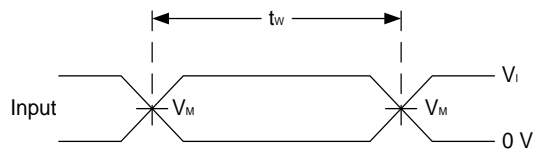
Note: 10. Test conditions for TSSOP-20 and V-QFN4525-20: Devices mounted on 4 layer FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout per JESD 51-7.

**Parameter Measurement Information**

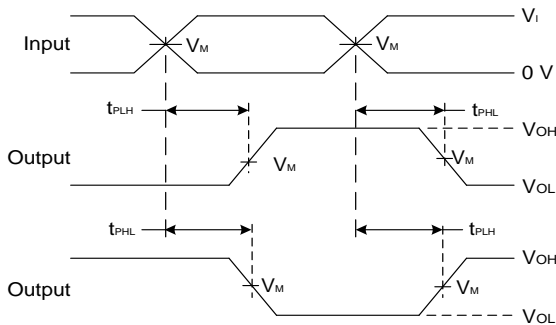


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

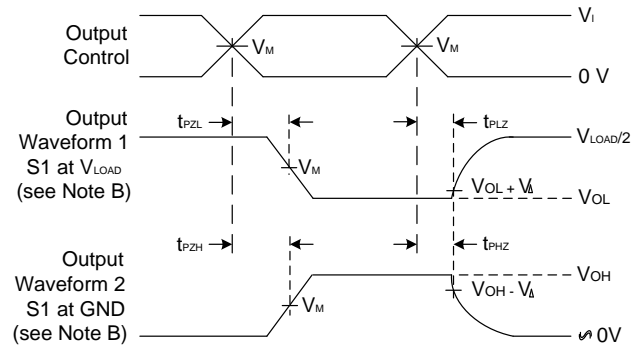
$V_{CC}$	Inputs		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_R/t_F$					
$3.3V \pm 0.3V$	2.7V	$\leq 2.5ns$	1.5V	6V	50pF	500Ω	0.3V



**Voltage Waveform Pulse Duration**



**Voltage Waveform Propagation Delay Times  
Inverting and Non Inverting Outputs**



**Voltage Waveform Enable and Disable Times  
Low and High Level Enabling**

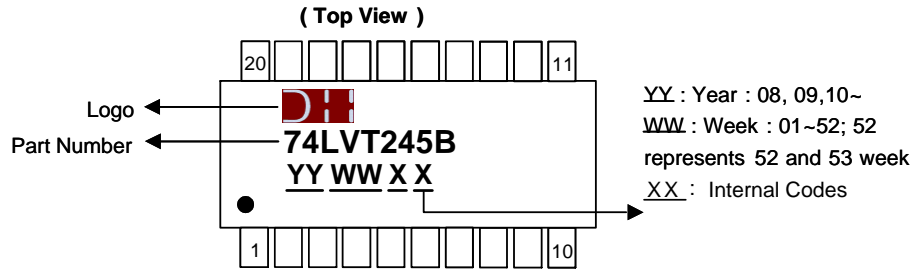
- Notes: A. Includes test lead and test apparatus capacitance.  
 B. All pulses are supplied at pulse repetition rate  $\leq 10$  MHz.  
 C. Inputs are measured separately one transition per measurement.

**Figure 1 Load Circuit and Voltage Waveforms**

NEW PRODUCT

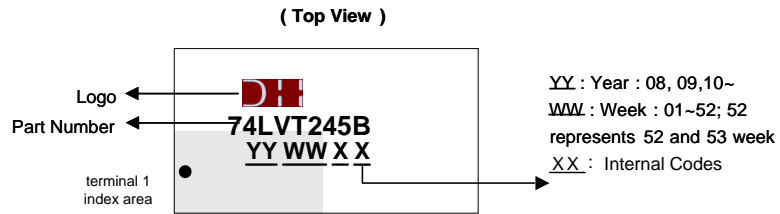
**Marking Information**

1) TSSOP20



Part Number	Package
74LVT245BBT20-13	TSSOP-20

2) QFN-20 (V-QFN4525-20)

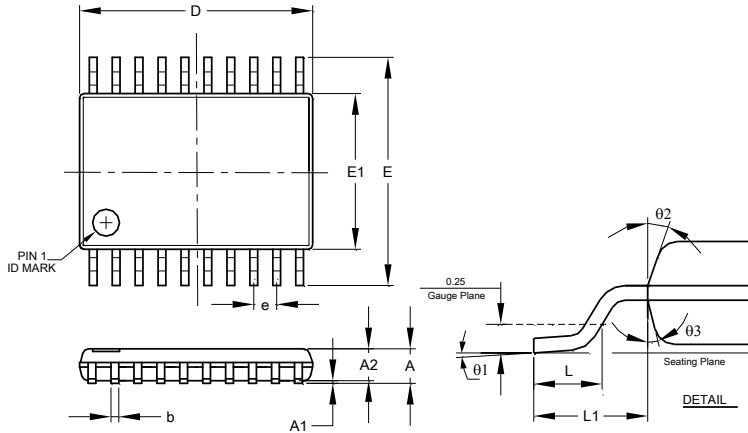


Part Number	Package
74LVT245BBQ20-13	V-QFN4525-20

**Package Outline Dimensions**

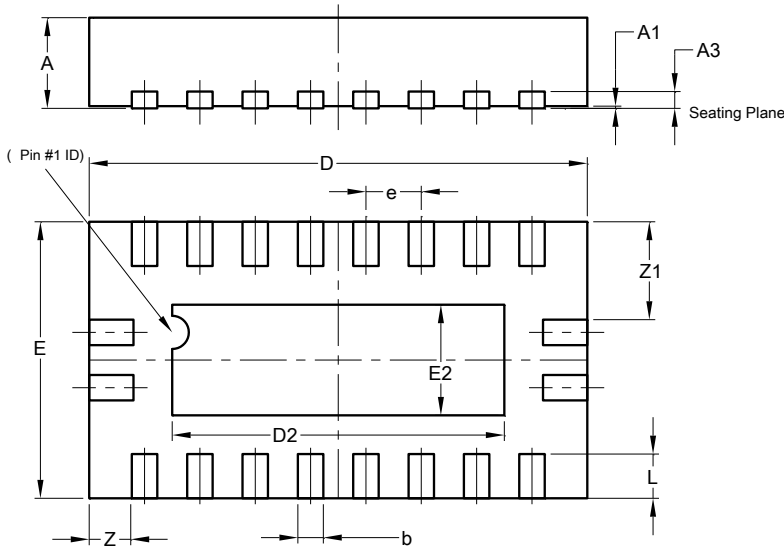
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**TSSOP-20**



TSSOP-20			
Dim	Min	Max	Typ
A	—	1.20	—
A1	0.05	0.15	—
A2	0.80	1.05	—
b	0.19	0.30	—
c	0.09	0.20	—
D	6.40	6.60	6.50
E	6.20	6.60	6.40
E1	4.30	4.50	4.40
e	0.65 BSC		
L	0.45	0.75	0.60
L1	1.0 REF		
theta1	0°	8°	—
theta2	10°	14°	12°
theta3	10°	14°	12°
All Dimensions in mm			

**V-QFN4525-20**



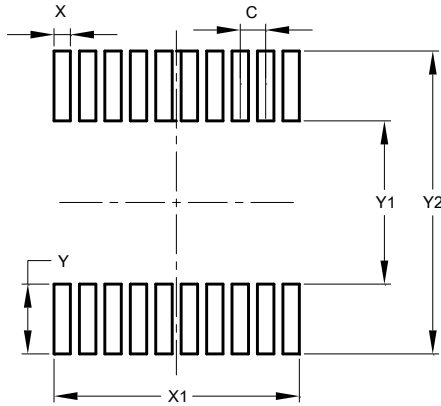
V-QFN4525-20			
Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	—	—	0.15
b	0.18	0.30	0.23
D	4.45	4.55	4.50
D2	2.85	3.15	3.00
E	2.45	2.55	2.50
E2	0.85	1.15	1.00
e	0.50BSC		
L	0.30	0.50	0.40
Z	—	—	0.385
Z1	—	—	0.885
All Dimensions in mm			



**Suggested Pad Layout**

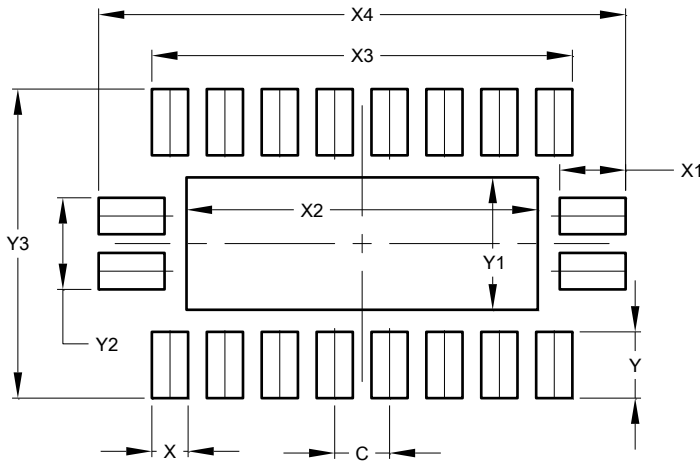
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**TSSOP-20**



Dimensions	Value (in mm)
C	0.650
X	0.420
X1	6.270
Y	1.780
Y1	4.160
Y2	7.720

**V-QFN4525-20**



Dimensions	Value (in mm)
C	0.500
X	0.330
X1	0.600
X2	3.200
X3	3.830
X4	4.800
Y	0.600
Y1	1.200
Y2	0.830
Y3	2.800

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