

## Description

The AP33771C is a highly integrated USB Type-C® PD 3.1 sink controller to support Extended Power Range (EPR)/Adjustable Voltage Supply (AVS) up to 28V and Standard Power Range (SPR)/Programmable Power Supply (PPS) up to 21V. The device is targeted for DC power request and control for Type-C Connector-equipped Devices (TCDs) through simple external resistor setting.

For a simple TCD without a system MCU, the AP33771C initiates desired power request by interpreting matching resistance values of the VSEL pin (voltage) and ISEL pin (current) after Power On Reset (POR), Table 2.

Based on the high-voltage process, the AP33771C offers short-protection between CC1/CC2 pins to adjacent high-voltage pin up to 34V. Smart built-in firmware of the AP33771C offers comprehensive safety protection schemes, including overvoltage protection (OVP), undervoltage protection (UVP), overcurrent protection (OCP), and moisture detection between DP and DN. An LED indicator is used to show the PD power negotiation status. The automatic cable voltage drop compensation is implemented to cover practical usage situations. Meanwhile, the AP33771C can indicate the insertion orientation of the Type-C attachment.

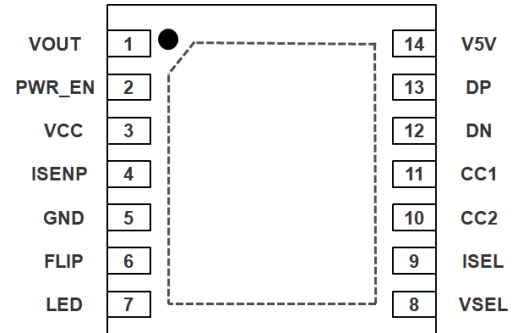
## Features

- USB PD 3.1 v1.6 Certified with TID: 9960
- Operating Voltage Range of VCC: 3V to 31V
- Supports PD 3.1 EPR/AVS up to 28V and SPR/PPS up to 21V
- Voltage/Current Selections Through Resistors Settings
- Support FLIP Indication of the Type-C Attachment
- Support OVP with Hard Reset and Auto Restart
- Support UVP and OCP with Output Power Shutdown
- Driver for Output Enable nMOS Switch
- Supports Dead Battery Function
- Automatic Cable Voltage Drop Compensation
- VBUS Short Protection on CC1/CC2 Pins up to 34V
- Moisture Detection Between DP and DN
- LED Indication for Different Negotiation Results
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative. <https://www.diodes.com/quality/product-definitions/>**

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.  
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.  
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Assignments

(Top View)



**W-DFN3030-14 (Type A1)**

## Applications

- USB Type-C connector-equipped battery-powered devices
- USB Type-C connector-equipped DC-power input devices
- USB PD 3.1 testers



## Pin Descriptions

Pin No.	Pin Name	Type*	Pin Function
1	VOUT	AHV	Terminal for VOUT monitoring and discharge path
2	PWR_EN	AHV	To control external VOUT nMOS switch ON (High) or OFF (Low)
3	VCC	AHV	The power supply of the AP33771C. A 1 $\mu$ F cap is required to connect this pin to GND pin.
4	ISENP	AHV	Current sense positive node
5	GND	GND	Ground
6	FLIP	DO	Flip indicator of Type-C plug-in attachment with CC1 (Low) or CC2 (High)
7	LED	DO	LED indicator of the system status
8	VSEL	AI	Voltage selection by connecting a corresponding resistor
9	ISEL	AI	Current selection by connecting a corresponding resistor
10	CC2	AIO	Type-C configuration channel 2
11	CC1	AIO	Type-C configuration channel 1
12	DN	AIO	USB 2.0 data negative node
13	DP	AIO	USB 2.0 data positive node
14	V5V	AP	5V LDO output if VCC is on. A 1 $\mu$ F cap is required to connect this pin to GND.
—	EPAD	GND	Exposed pad is suggested to connect to Ground

\* AHV – Analog High Voltage pin  
 AP – Power for Analog Circuit and Analog Input/Output pins, 5.0V operation  
 AI – Analog Input pin  
 AIO – Analog Input/Output pin. DP/DN & CC1/CC2 are 3.3V operation.  
 DO – Digital Output pin. All are 5.0V operation.

**Table 1. Pin Descriptions of AP33771C Sink Controller**

**Functional Block Diagram**

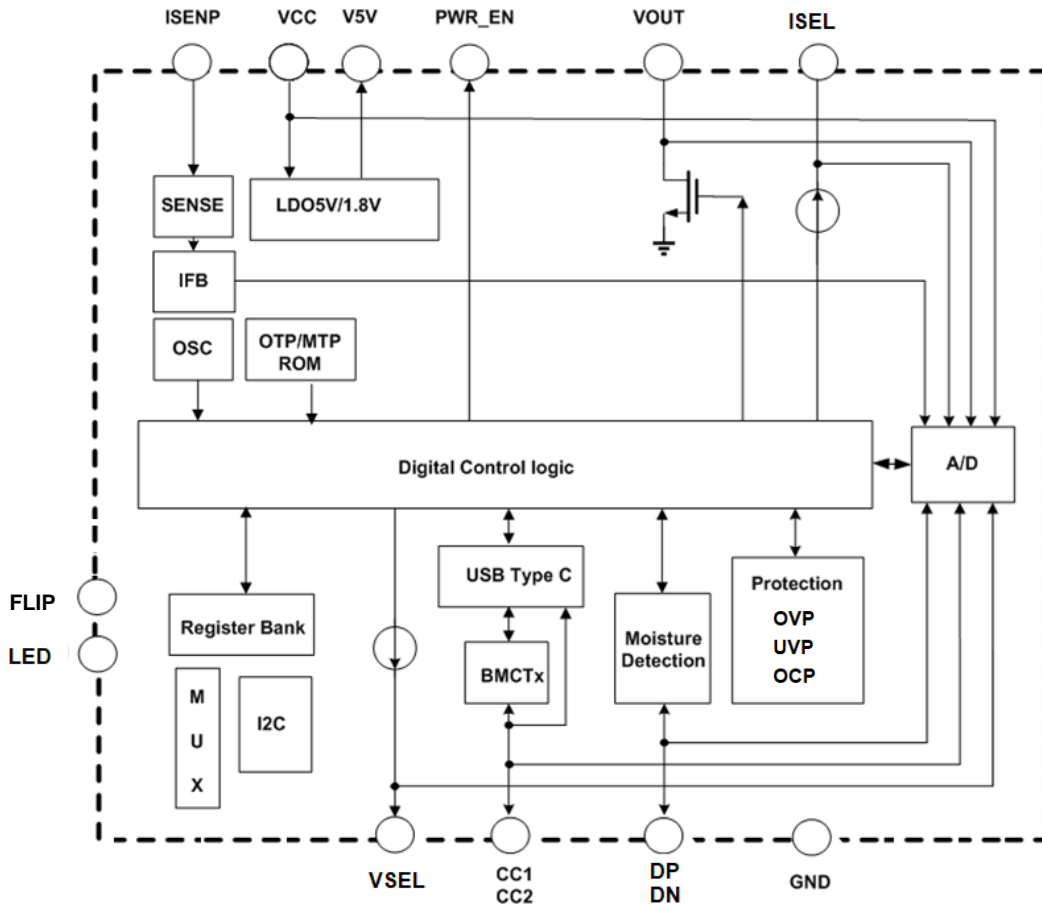


Figure 2. The Functional Block Diagram of AP33771C PD 3.1 Sink Controller

### Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V <sub>VCC</sub>	Input Voltage at VCC Pin	-0.3 to 34	V
V <sub>V5V</sub>	Input Voltage at V5V Pin	-0.3 to 7	V
V <sub>VSEL</sub> , V <sub>ISEL</sub> , V <sub>LED</sub> , V <sub>FLIP</sub>	Input Voltage at VSEL, ISEL, LED, FLIP Pins	-0.3 to 7	V
V <sub>VOUT</sub> , V <sub>ISENP</sub>	Input Voltage at VOUT, ISENP Pins	-0.3 to 31	V
V <sub>PWR_EN</sub>	Input Voltage at PWR_EN Pin	-0.3 to 38	V
—	Voltage from PWR_EN to VCC Pin	-16 to 4	V
V <sub>CC1</sub> , V <sub>CC2</sub>	Input Voltage at CC1, CC2 Pins	-0.3 to 34	V
V <sub>DP</sub> , V <sub>DN</sub>	Input Voltage at DN, DP Pins	-0.3 to 7	V
T <sub>J</sub>	Operating Junction Temperature	-40 to +150	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
T <sub>LEAD</sub>	Lead Temperature (Soldering, 10s)	+300	°C
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient) (Note 5)	122	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case) (Note 5)	27	°C/W
ESD	Human Body Model	2	kV
ESD	Charged Device Model	750	V

- Notes:
- Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
  - Test condition: device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

### Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V <sub>VCC</sub>	Power Supply Voltage at VCC Pin	3.3	31	V
V <sub>V5V</sub>	Input Voltage at V5V Pin	4.37	5.33	V
V <sub>DP</sub> , V <sub>DN</sub>	Input Voltage at DP, DN Pins	2.75	3.25	V
T <sub>J</sub>	Junction Temperature Range	-40	+125	°C

**Electrical Characteristics** (@ T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>VCC SECTION</b>						
V <sub>ST</sub>	Startup Voltage	—	2.5	2.8	3.5	V
V <sub>UVLO</sub>	Minimum Operating Voltage	—	2.3	2.7	3	V
V <sub>VCC_HYS</sub>	VCC Hysteresis (V <sub>ST</sub> -V <sub>UVLO</sub> )	—	0.05	—	—	V
I <sub>VCC_OPR</sub>	Operating Supply Current	V <sub>VCC</sub> = 5V	—	3.3	6	mA
<b>CC1/CC2 SECTION</b>						
V <sub>L_RD3A</sub>	Low Voltage Threshold Used to Distinguish R <sub>D</sub> Attached or Detached for 3A Delivery	—	—	1.35	—	V
V <sub>H_RD3A</sub>	High Voltage Threshold Used to Distinguish R <sub>D</sub> Attached or Detached for 3A Delivery	—	—	2.0	—	V
<b>VOLTAGE SELECTION AND CURRENT SELECTION</b>						
I <sub>VSEL</sub>	VSEL Current Source (Note 6)	—	—	20.5	—	μA
I <sub>VSEL_Range</sub>	VSEL Current Source Range (Note 6)	—	-3	—	+3	%
I <sub>ISEL</sub>	ISEL Current Source (Note 6)	—	—	20	—	μA
I <sub>ISEL_Range</sub>	ISEL Current Source Range (Note 6)	—	-3	—	+3	%
<b>FLIP and LED SECTION</b>						
V <sub>O</sub>	FLIP, LED Output Voltage Range (Note 6)	V <sub>VCC</sub> = 5V	4.37	4.85	5.33	V
I <sub>SS</sub>	FLIP, LED Sink/Source Capability (Note 6)	—	2	—	—	mA
<b>PROTECTION FUNCTION SECTION</b>						
V <sub>OVP5V</sub>	OVP_5V Enable Voltage (Notes 6 & 7)	—	—	7	—	V
V <sub>OVP20V</sub>	OVP_20V Enable Voltage (Notes 6 & 7)	—	—	22	—	V
V <sub>OVP28V</sub>	OVP_28V Enable Voltage (Notes 6 & 7)	—	—	31	—	V
t <sub>DEBOUNCE_OVP</sub>	OVP Debounce Time (Note 8)	—	—	90	—	ms
t <sub>OV_DELAY</sub>	Delay from OVP Threshold Trip to nMOS Gate Turn-Off (Note 6)	—	—	—	50	ms
T <sub>OTP</sub>	Internal OTP Temperature	—	—	+135	—	°C
T <sub>OTP_HYS</sub>	OTP Hysteresis	—	—	+10	—	°C
<b>V5V SECTION</b>						
V <sub>V5V</sub>	V5V Output Range	—	4.37	4.85	5.33	V
I <sub>V5V</sub>	V5V Source Capability	—	—	30	—	mA

- Notes:
6. Guaranteed by design.
  7. 110% OVP setting @PDO > 18V. PDO+2V OVP setting @PDO ≤ 18V.
  8. OVP blanking time during V<sub>O</sub> transition from high output voltage to low output voltage, such as 9V to 5V, or 12V to 5V.

## Functional Description

### Overview

The AP33771C, a highly integrated USB Type-C PD 3.1 sink controller, supports EPR/AVS up to 28V and provides SPR/PPS up to 21V. The device is targeted for DC power request and control for flexible Type-C Connector-equipped Devices (TCDs) without an embedded host MCU. The AP33771C generates a Request Data Object (RDO) of voltage and current through resistor settings in VSEL and ISEL pins, and then automatically initiates the PD negotiation process with the attached Type-C PD Compliance charger (through Type-C to Type-C cable) or legacy Type-C charger (through Type-A to Type-C cable) after the POR initialization.

### VCC and VOUT

VCC pin is the power supply input of the AP33771C, which is derived from the VBUS output of the PD source. Also, it provides a discharge path for VBUS input power in case the hard reset, overvoltage fault, or detachment of a connected device. A low pass filter or capacitor decoupling in VCC pin is suggested.

The AP33771C monitors the output voltage at VOUT pin, connected to the nMOS Enable Switch, which also has a built-in discharge path. A 100Ω resistor between MOS output and AP33771C VOUT pin is required.

### CC1/CC2 Connection and FLIP Indication

The Configuration Channel pins (CC1/CC2) are used for connection and attachment detection, plug orientation determination and system configuration. As soon as the PD source adapter is plugged into the AP33771C-embedded TCD device, one of the R<sub>DS</sub> will be pull down and the CC/VCONN connection and data path routing are established accordingly. At the same time, the source adapter enables VBUS and VCONN power supply, and then starts broadcasting PD source capabilities and PD negotiation through CC pin, which is connected to the internal Bi-phase Mark Code (BMC) block.

During the cable attachment, the configuration information and source capabilities are stored in the AP33771C internal registers. The AP33771C uses FLIP pin for CC flip indication. If CC is connected to CC1 (non-flipped), the FLIP output is low. If CC is connected to CC2 (flipped), the FLIP output is high.

### Sink RDO Selection

The AP33771C sink controller generates a RDO of voltage and current to negotiate a power profile with a PD source controller. The voltage and current values are determined from the hardware setting. With a constant current source output from the VSEL and ISEL pins, system designers connect suitable resistors to both pins, and the AP33771C measures the voltage levels at these two pins through internal ADC. Up to eight resistors are supported both in voltage and current selections. It is suggested to use the resistors with ±1% accuracy to connect to the VSEL and ISEL pins to ensure the request selection. The mapping between VSEL/ISEL amplitudes and resistance values are illustrated in Table 2 below. It reminds system designers that if current requirement is greater than 3A, a suitable e-Marker cable with over 3A current rating is needed.

Index	1	2	3	4	5	6	7	8
VSEL	5V	9V	12V	15V	20V	28V	Reserved	Reserved
ISEL	1A	1.5A	2A	2.5A	3A	3.5A	4A	5A
Resistance (kΩ, 1%)	100	82	66	52	39	26	15	5.1

Table 2. The Mapping Between VSEL/ISEL Amplitudes and Resistance Values

## Functional Description (continued)

### Matching Mechanism

After the POR initiation, the AP33771C starts the PD negotiation with the external PD source. All of the source capability information is received and stored into its internal registers during the handshake. The matching mechanism of PDO selection used in AP33771C is summarized in the Table 3, where voltage matching is performed firstly, and then current matching is proceeded if voltage match happens.

Source PDO	Voltage Match Criteria*	Current Match Criteria*
Fixed PDO	$V_{VSELMIN} \leq V_{FIXED} \leq V_{VSEL}$	$I_{ISEL} \leq I_{MAX}$
PPS APDO	$V_{MIN} \leq V_{VSEL} \leq V_{MAX}$	$I_{ISEL} \leq I_{MAX}$
AVS APDO	$V_{MIN} \leq V_{VSEL} \leq V_{MAX}$	$V_{VSEL} \times I_{ISEL} \leq PDP$

- \*  $V_{VSEL}$ : Voltage selected by VSEL pin
- $I_{ISEL}$ : Current selected by ISEL pin
- $V_{FIXED}$ : Voltage of Fixed PDO
- $V_{MIN}$ : Minimum Voltage of PPS/AVS PDO
- $V_{MAX}$ : Maximum Voltage of PPS/AVS PDO
- $I_{MAX}$ : Maximum Current of PDO
- PDP: Output Power of AVS PDO (W)
- $V_{SELMIN}$ : Predetermined Minimum value of  $V_{VSEL}$

**Table 3. RDO Matching Mechanism Used in the AP33771C Sink Controller**

If the PD source supports EPR Mode and VSEL is set  $\geq 28V$ , the AP33771C will enter EPR mode and enable EPR request firstly. If more than one PDO are matched, the PPS/AVS PDOs have higher priority over the Fixed PDOs. If more than one PPS/AVS PDO are matched, the PDO with the lowest voltage takes precedence over the others. Typically, higher PPS/AVS voltages are accompanied by lower  $I_{MAX}$  currents.

During the voltage matching of fixed PDO, the selection criterion is to select the PDO closest to  $V_{VSEL}$  in descending order from the PDOs equal to  $V_{VSEL}$ . The fixed PDO selection has a lower limit,  $V_{VSELMIN}$ , which is a predetermined parameter during the firmware programming. If the selected Fixed PDO is lower than  $V_{VSELMIN}$ , the system enters the mismatch state. For the AP33771C, the predetermined value of  $V_{VSELMIN}$  is set to 5V.

After voltage matching process is completed, the PDOs that meet the voltage matching criteria will perform current matching flow again. During the current matching process, fixed PDO or PPS APDO with  $I_{MAX}$  greater than  $I_{ISEL}$  will be selected, and AVS APDO with PDP greater than  $V_{VSEL} \times I_{ISEL}$  will be selected.

During the PD handshake between the TCD and the external PD source, the AP33771C acquires and stores source capability into relevant registers. If there are valid source capabilities that match with the RDO selection before timeout, the AP33771C policy engine then requests a suitable power profile from the source adapter. If there is still no valid source capability matched to the RDO after timeout, the AP33771C indicates mismatch information through the LED indicator.

### nMOS VOUT Enable Switch

Taking VBUS voltage as input, the built-in charge-pump circuit generates a high voltage gate driver (PWR\_EN) to drive an external low cost high-side nMOS switch. A suitable small resistance is suggested to connect the PWR\_EN to the nMOS gate. Once the PDO negotiations are matched with each other between source side and sink side, PWR\_EN enables the nMOS switch and VBUS is connected to VOUT. Otherwise, the nMOS switch will not be turned on, and VBUS is disconnected from VOUT.

Meanwhile, the nMOS VOUT enable switch is also used for power protection. When output overvoltage, undervoltage, overcurrent or even moisture detection occurs, the associated VOUT MOS Switches are turned off to protect the electrical appliances from possible damage.

### Power Protection

Based on high-voltage process, the AP33771C offers short-protection between CC1/CC2 pins to adjacent high-voltage pin up to 34V. In addition, the smart built-in firmware of the AP33771C offers comprehensive safety protection schemes, including OVP, UVP, and OCP. When the power protection occurs, the associated VOUT MOS switch is turned off to disconnect VBUS from VOUT.



## Functional Description (continued)

The AP33771C triggers the OVP protection when VBUS voltage is higher than OVP threshold voltage. The Table 4 below summarizes the correspondence between VREQ and OVP threshold voltage, where VREQ is the requested voltage after successful power negotiation with the PD source controller, and OVP threshold is set to be 2V above VREQ. If VBUS voltage is higher than OVP threshold after the de-bounce time limit, the AP33771C will issue hard reset to the source adapter and enter the FAULT state by turning off nMOS switch to disconnect VBUS from VOUT. The AP33771C will automatically restart as soon as the VOUT discharging is completed.

Index	1	2	3	4	5	6	7	8
VREQ	5V	9V	12V	15V	20V	28V	Reserved	Reserved
OVP Threshold	7V	11V	14V	17V	22V	30V	—	—

**Table 4. Correspondence Between VREQ and OVP Threshold Voltage**

The AP33771C also triggers the UVP protection when VBUS voltage is lower than UVP threshold voltage. The UVP threshold voltage is set at 80% of the requested voltage (VREQ).

The AP33771C supports OCP to control the output load condition. When the OCP function is enabled, the AP33771C monitors the output current through detection of IR drop on the 5mΩ Rsense resistor. Once the TCD device draws more current than the OCP threshold level (110% of the requested current IREQ, the requested current after successful negotiation with the source), the AP33771C enables OCP by turning off the nMOS switch to disconnect VBUS from VOUT.

### Moisture Detection

The AP33771C supports the moisture detection through DP/DN pins. As soon as the Type-C connector is plugged in, the impedance between the DN/DP pins to ground is evaluated by internal ADC digitization and firmware calculation. If the impedance level is below the pre-determined threshold, the VOUT MOS switch is turned off to disconnect VBUS from VOUT, and the LED is switched to 2-sec flicker mode accordingly.

### LED Indication

The user is informed of the system status by the LED blinking patterns, which summarizes LED indication and VOUT status in each state, as shown in Table 5 below.

State	LED Indication	VOUT	Comments
INIT	NA	OFF	During VBUS/Rd attachment and AP33771C initialization
CHARGING	4-sec Breathing	ON	Successful negotiation or enter Non-PD Mode and start charging
MISMATCH	Full Light	OFF	Voltage or Current mismatch
MOISTURE	2-sec Flicker	OFF	DP/DN abnormal impedance detected
FAULT	0.6-sec Flicker	OFF	OVP, OCP or UVP occurs.

**Table 5. Flash LED Indication for Different Negotiation Results**

### Cable Voltage Drop Compensation for PD Mode

After the AP33771C completes the RDO negotiation based on VSEL and ISEL and enables the VOUT MOS Switch, the AP33771C monitors the VOUT voltage level. If the VOUT voltage (VOUT) fails to reach more than 6% below the selected voltage (VSEL), the AP33771C activates automatic Type-C cable voltage drop compensation scheme, shown as Table 6.

Source PDO	Compensation Criteria	Compensation Manner	Voltage Compensation Upper Limit
Fixed PDO	$V_{VOUT} < V_{VSEL} \times 0.94$ (Note 9)	PDO Position +1 (next higher voltage PDO)	4.0V (Note 10)
PPS APDO	$V_{VOUT} < V_{VSEL} \times 0.94$ (Note 9)	Voltage + 0.1V each voltage drop compensation iteration	1.3V (Note 11)

- Notes:
- 9. Enables voltage drop compensation when  $V_{VOUT} < V_{VSEL} \times (1 - 6\%)$ .
  - 10. Upper limit of voltage compensation is set at 4.0V to prevent subsequent circuit from potential damage. For example, PDO 5V can only be raised to next PDO 9V.
  - 11. The Type-C to Type-C compliance cables have typically end-to-end resistance of 250mΩ of any length. The maximum voltage drop compensation allowed is 1.3V, from source-end to sink-end of a Type-C to Type-C cable should be within 1.25V for maximum current of 5A.

**Table 6. Cable Voltage Drop Compensation Criteria for PD Mode**

## Functional Description (continued)

The V<sub>OUT</sub> voltage behavior comparison between compensation and non-compensation is shown in Table 7 below. If the voltage drop compensation fails, it means that no suitable PDO is found or voltage compensation exceeds the upper limit.

Source PDO	V <sub>SEL</sub>	Before Compensation		After Compensation	
		Original Request Voltage	V <sub>OUT</sub>	Adjusted Request Voltage (V <sub>AREQ</sub> )	V <sub>OUT</sub>
Fixed_5V	5V	Fixed_5V	< 4.7V	Fixed_5V	< 4.7V
Fixed_5V / Fixed_9V	5V	Fixed_5V	< 4.7V	Fixed_9V	9V-Cable Voltage Drop (1.3V max) (Note 13)
Fixed_5V / Fixed_9V / PPS_3.3V to 11V	5V	PPS_5V	< 4.7V	PPS_5V+Voltage Drop (1.3V max) (Note 12)	≥ 4.7V
Fixed_5V / Fixed_9V / PPS_3.3V to 11V	5V	PPS_5V	< 4.7V	PPS_5V+1.3V	< 4.7V

Notes: 12. If the cable voltage drop from the source-end to the sink-end is 1.0V, adjusted V<sub>AREQ</sub> would be 5.7V for V<sub>OUT</sub> to reach 4.7V.  
 13. If the cable voltage drop from the source-end to the sink-end is 1.0V, adjusted V<sub>AREQ</sub> would be 9V and V<sub>OUT</sub> would be 8V.

**Table 7. V<sub>OUT</sub> Voltage Behavior Under PD Mode with Cable Drop Compensation**

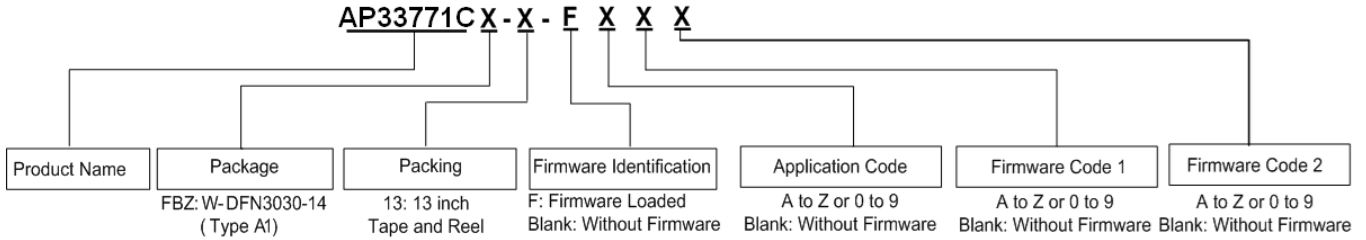
### Legacy Type-A Charger with Type-A to Type-C Cable

When the energy source is from a legacy Type-A charger with Type-A to Type-C cable connection to the TCD, the AP33771C enters the Non-PD mode after PD negotiation fails. Table 8 below shows the Non-PD mode state of AP33771C.

Non-PD Mode State			
V <sub>SEL</sub>	V <sub>SELMIN</sub>	V <sub>OUT</sub>	State
V <sub>SEL</sub> = 5V	5V	ON	CHARGING
V <sub>SEL</sub> ≥ 9V	5V	ON	CHARGING

**Table 8. V<sub>OUT</sub> Voltage Status under Non-PD Mode**

**Ordering Information**

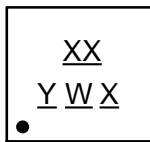


Part Number	Package	Identification Code	Packing	
			Qty.	Carrier
AP33771CFBZ-13-FA01	W-DFN3030-14 (Type A1)	6X	3000	13" Tape & Reel

**Marking Information**

W-DFN3030-14 (Type A1)

**( Top View )**

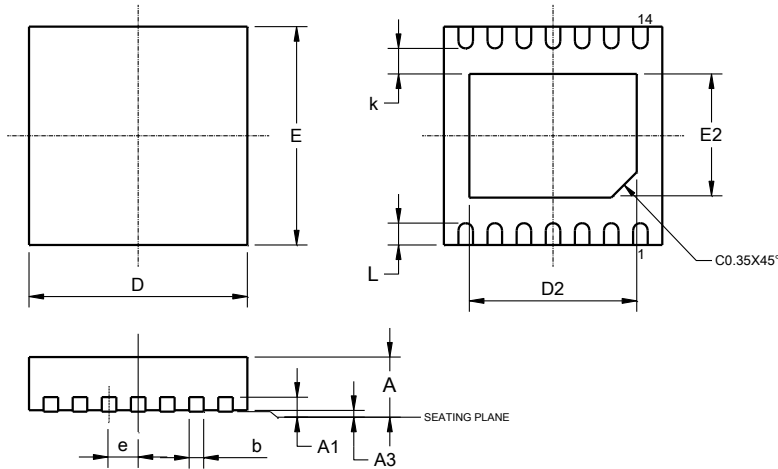


- XX : Identification Code
- Y : Year : 0 to 9 (ex: 3 = 2023)
- W : Week : A to Z : week 1 to 26;  
a to z : week 27 to 52; z represents week 52 and 53
- X : Internal Code

**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

W-DFN3030-14 (Type A1)

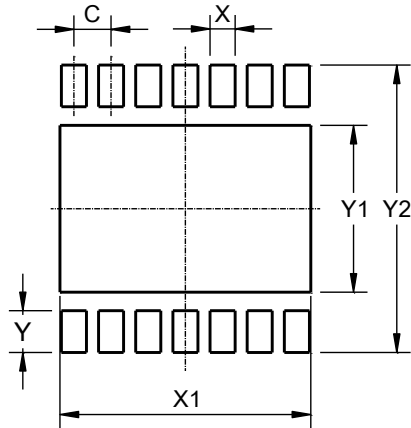


W-DFN3030-14 (Type A1)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	0	0.05	0.02
A3	0.203REF		
b	0.15	0.25	0.20
D	3.00BSC		
D2	2.55	2.65	2.60
e	0.40BSC		
E	3.00BSC		
E2	1.65	1.75	1.70
k	0.20	--	--
L	0.35	0.45	0.40
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

W-DFN3030-14 (Type A1)



Dimensions	Value (in mm)
C	0.40
X	0.27
X1	2.70
Y	0.45
Y1	1.80
Y2	3.10

**Mechanical Data**

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per J-STD-202 (e3)
- Weight: 0.017 grams (Approximate)

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