PRIMARY SIDE REGULATED SWITCHING MODE POWER SUPPLY CONTROLLER

Description

The AP3781 is a high performance AC/DC power supply controller for battery charger and adapter applications. The controller regulates the output voltage and current in the primary side by Pulse Frequency Modulation in Discontinuous Conduction Mode (DCM).

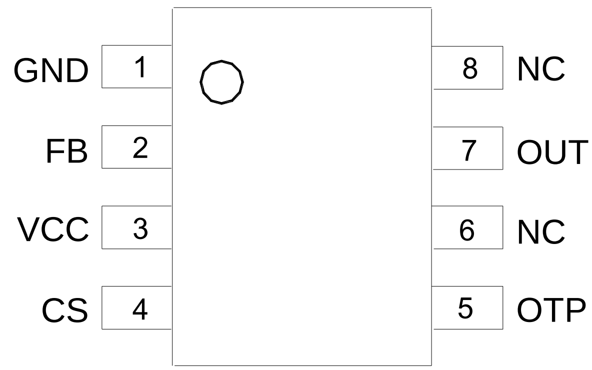
The AP3781 operates in Pulse Frequency Modulation (PFM) mode and peak current Amplitude Modulation (AM) mode to form a fine tune frequency curve within the whole power range. Therefore, AP3781 can achieve high average efficiency and improve audible noise.

The AP3781 provides comprehensive protections without additional circuitry. It contains V_{CC} over voltage protection, output over voltage protection, output under voltage protection, output short circuit protection, cycle-by-cycle current limit, open loop protection, external OTP and internal OTP, etc.

The AP3781 is packaged in SO-8.

Pin Assignments

(Top View)



SO-8

Features

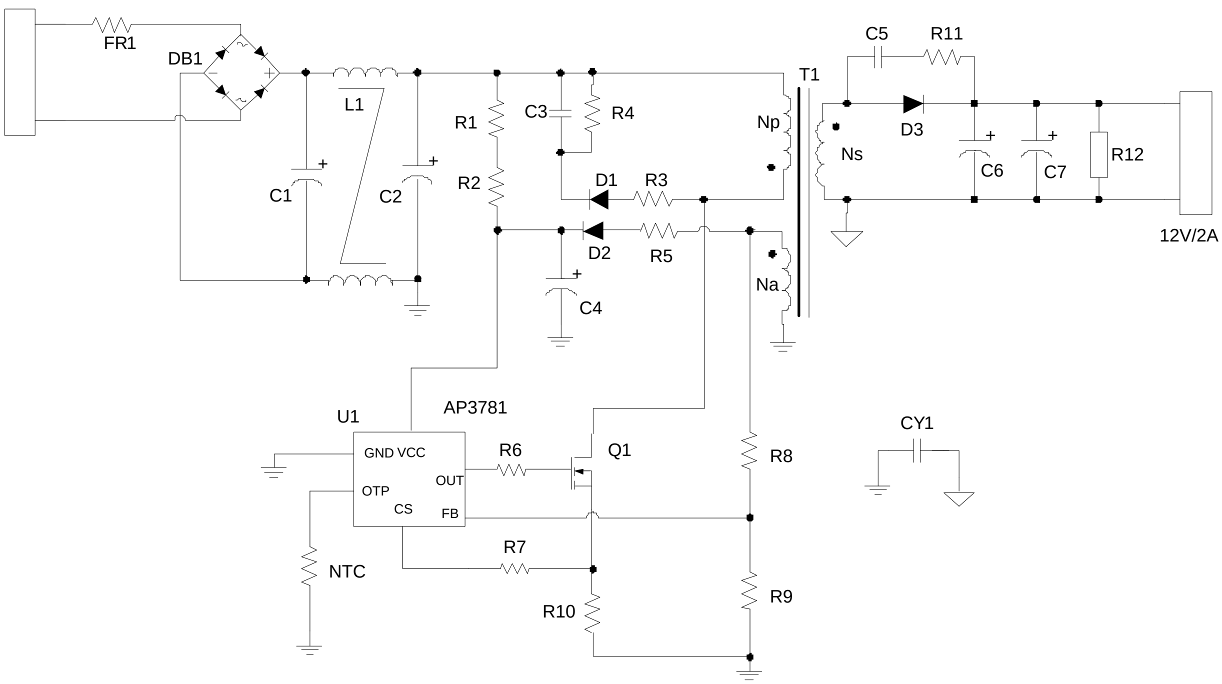
- Primary Side Control for Eliminating Opto-Coupler
- 75mW No-Load Input Power
- Flyback Topology in DCM Operation
- External Adjustable Over Temperature Protection
- Fixed Internal Cable Compensation: 3%
- External Cable Compensation: 3% to 8%
- Multiple Segment AM/PFM Control Mode to Improve Audio Noise and Efficiency
- Ultra Low Under Voltage Protection, Support Wide Operating Voltage for Power Tool Motor Drive
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.** **https://www.diodes.com/quality/product-definitions/**

Applications

- Routers
- Power Tools
- Set-Top Box (STB) Power Supply
- Smart Speakers
- Network Adaptors

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

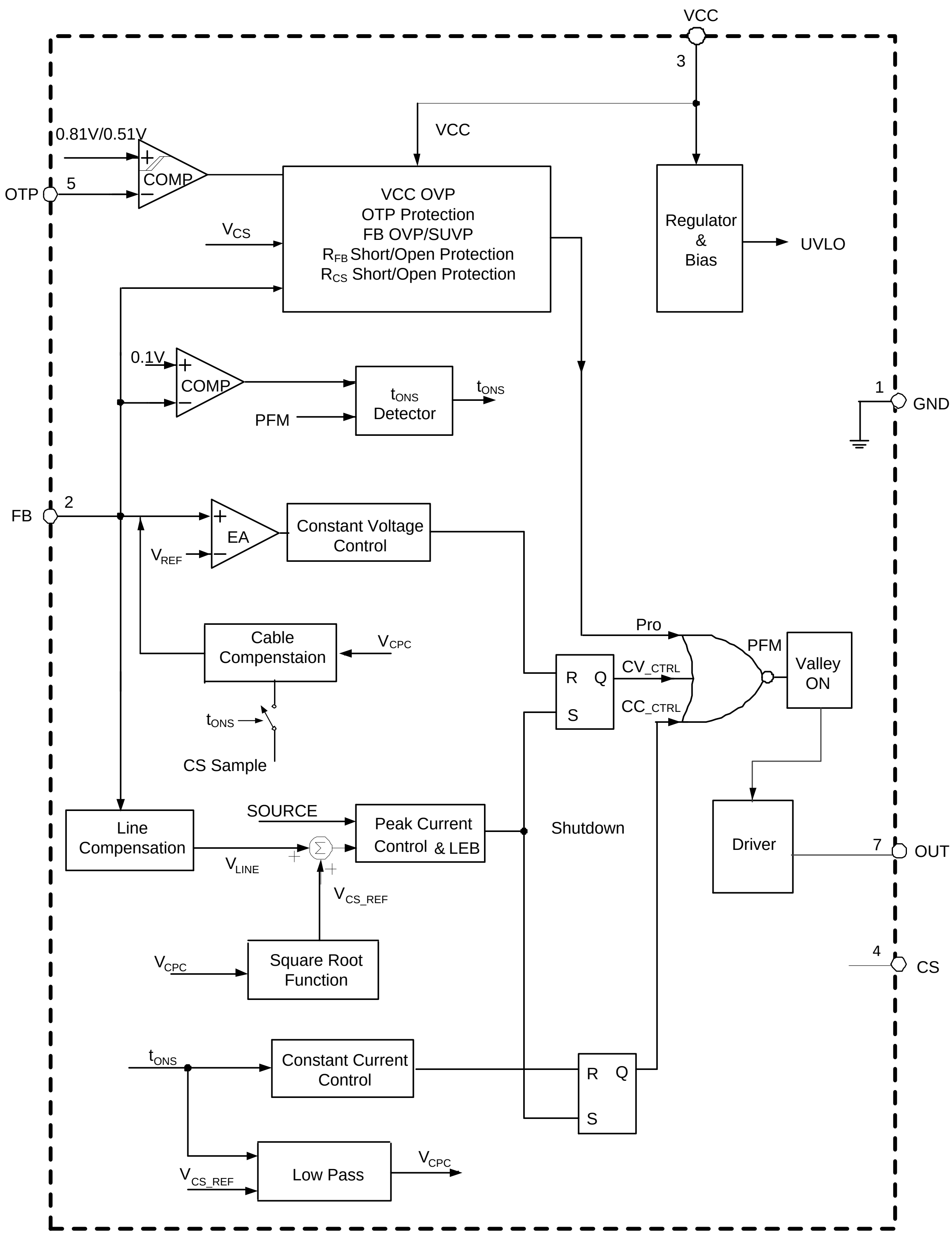
Typical Applications Circuit



Pin Descriptions

Pin Number	Pin Name	Function
1	GND	The ground of the controller
2	FB	The CV regulation is realized based on the voltage sampling of this pin
3	VCC	The VCC pin supplies the power for the IC
4	CS	The CS is the current sense pin of the IC. The IC will turn off the power MOSFET according to the voltage on the CS pin
5	OTP	Adjustable over temperature protection by external NTC resistor
6	NC	No Connection
7	OUT	Output pin to drive external MOSFET
8	NC	No Connection

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	-0.3 to 37	V
V_{CS}	Input Voltage	-0.3 to 8	V
V_{FB}	FB Input Voltage	-0.7 to 8	V
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{LEAD}	Lead Temperature (Soldering, 10s)	+300	°C
θ_{JC}	Thermal Resistance (Junction to Case) (Note 5)	16	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 5)	117	°C/W
—	ESD (Human Body Model)	2000	V
—	ESD (Charged Device Model)	1000	V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
5. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with $1inch^2$ cooling area.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	10	30	V
T_A	Ambient Temperature	-40	+85	°C

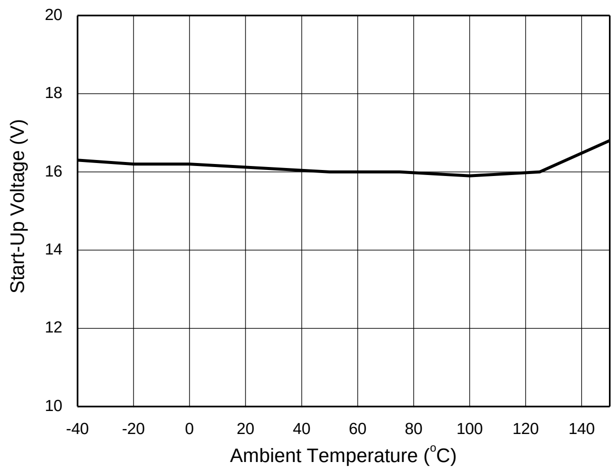
Electrical Characteristics (@V_{CC} =15V, T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STARTUP AND UVLO SECTION						
V_{TH_ST}	Startup Threshold	—	14.5	16	17.5	V
$V_{OPR(MIN)}$	Minimum Operating Voltage	—	6.1	6.8	7.5	V
STANDBY CURRENT SECTION						
I_{ST}	Startup Current	V_{CC}=V_{TH_ST}-1V before Startup	—	1	3	μA
I_{CC_OPR}	Operating Current	Static Current	410	510	610	μA
CURRENT SENSE SECTION						
V_{CS_H}	Peak Current Sense Threshold Voltage	40% to 100% CC Load	580	645	710	mV
R_{LINE}	Built-In Line Compensation Resistor	—	45	55	65	Ω
t_{LEB}	Leading Edge Blanking	—	330	420	510	ns
CONSTANT VOLTAGE SECTION						
V_{FB}	Feedback Threshold Voltage	Closed Loop Test of V_{OUT}	2.35	2.4	2.45	V
Ratio $_{SAMPLE\_H}$	Sample Ratio	40% to 100% CC Load	75	80	85	%
CONSTANT CURRENT SECTION						
t_{ONS}/t_{SW}	Secondary Winding Conduction Duty	Tested @ V_{FB} = 2V (Note 6)	—	0.5	—	—
FREQUENCY JITTER						
$\Delta V_{CS}/V_{CS}$	V_{CS} Modulation	10% Load to Full Load (Note 6)	—	3	—	%
CABLE COMPENSATION						
ΔV_{CABLE}	Cable Compensation Voltage	—	—	ADJ	—	%
DYNAMIC SECTION						
$t_{OFF(MAX)}$	Maximum Off Time	—	1.8	2	2.2	ms
DRIVING OUTPUT SECTION						
V_{GATE}	Gate Voltage	—	—	8	—	V
I_{SOURCE_PEAK}	Peak Driver Source Current	—	29	39	49	mA
$R_{DS(ON)}$	Sink Resistance	(Note 6)	7.0	8.2	9.4	Ω
PROTECTION SECTION						
$V_{FB(SOVP)}$	Over Voltage Protection at FB Pin	—	3.3	3.6	3.9	V
$V_{FB(SUVP)}$	Under Voltage Protection at FB Pin	—	150	200	250	mV
$t_{DELAY(SUVP)}$	Delay Time of SUVP	—	58	64	70	ms
$V_{CC(OVP)}$	Over Voltage Protection at VCC Pin	—	31.5	34	36.5	V
$t_{ONP(MAX)}$	Maximum Turn-on Time	—	13	19	25	μs
$V_{CS(MIN)}$	Minimum Peak Current Sense Voltage at t_{ONP} = 4.5μs	—	70	100	130	mV
$V_{FB\_NEG\_H}$	High Threshold for FB Negative Voltage Protection	—	27	36	45	mV
Internal T_{OTP}	Shutdown Temperature	(Note 6)	+135	+150	+165	°C
Internal T_{HYS}	Temperature Hysteresis	(Note 6)	+27	+30	+33	°C
V_{OTP}	External OTP Shutdown Threshold	—	480	510	540	mV
V_{OTP_REC}	External OTP Recovery Threshold	—	770	810	850	mV
I_{OTP}	External OTP Shutdown Current	—	74	80	86	μA

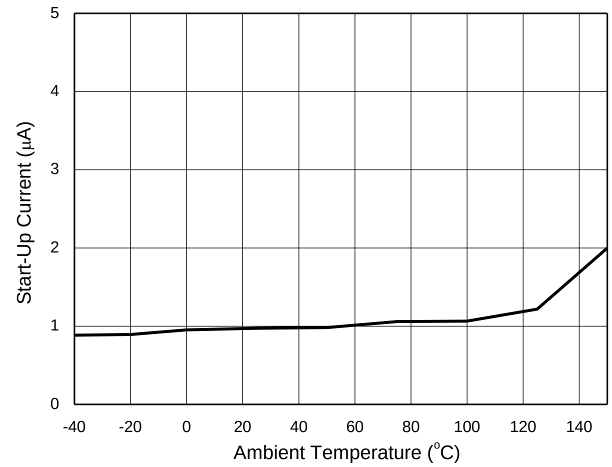
Note: 6. Guaranteed by design.

Performance Characteristics

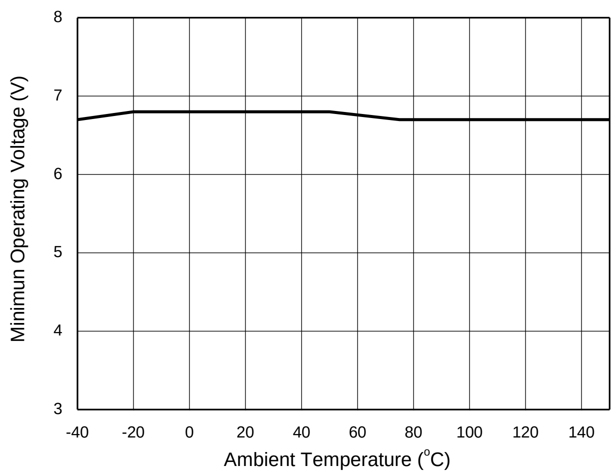
Start-Up Voltage vs. Ambient Temperature



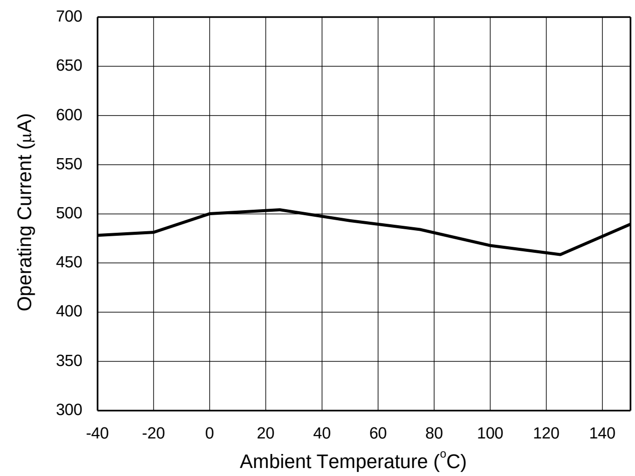
Start-Up Current vs. Ambient Temperature



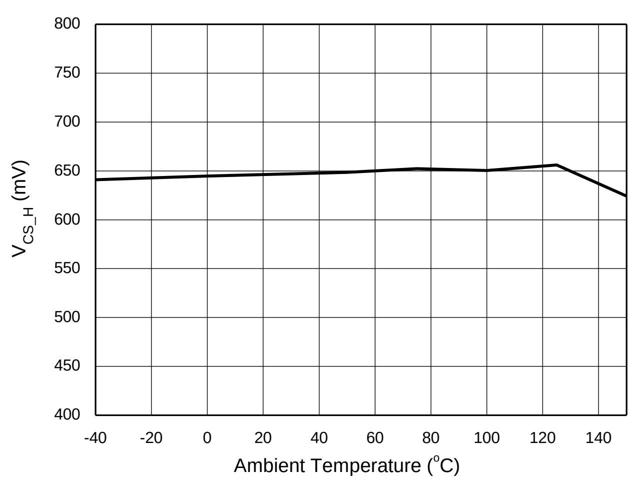
Minimal Operating Voltage vs. Ambient Temperature



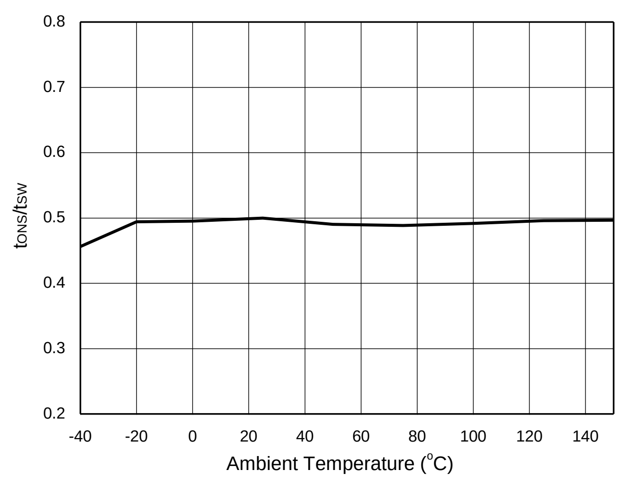
Operating Current vs. Ambient Temperature



V_{CS_H} vs. Ambient Temperature

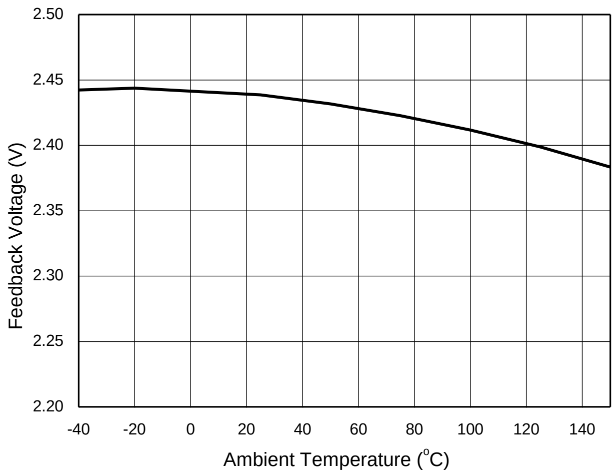


t_{ONS}/t_{SW} vs. Ambient Temperature

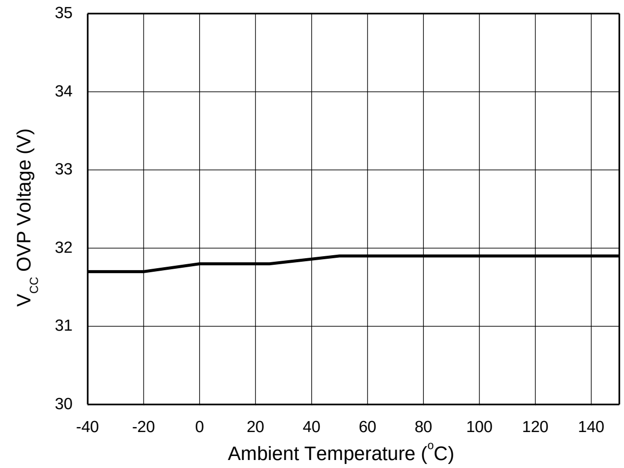


Performance Characteristics (continued)

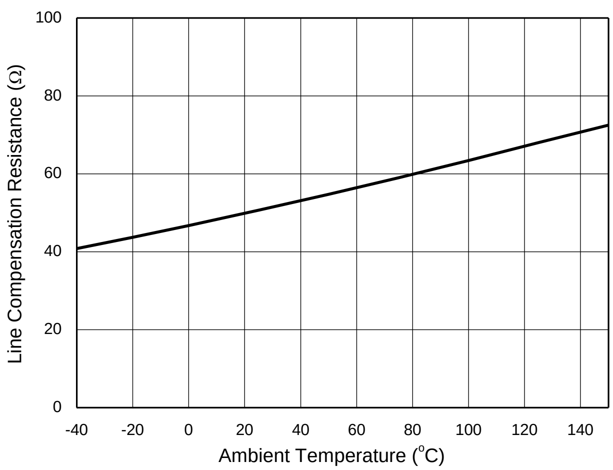
Feedback Voltage vs. Ambient Temperature



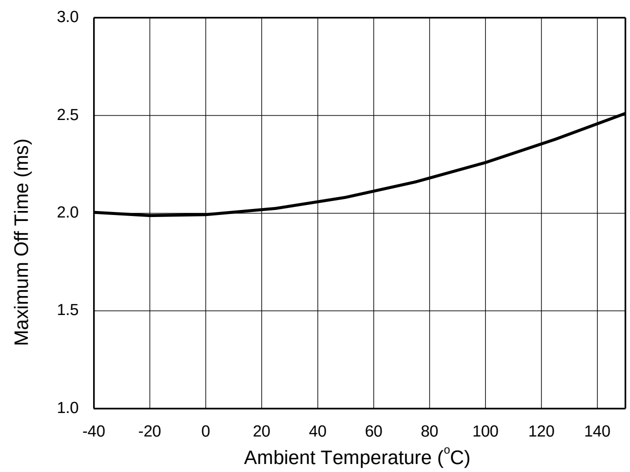
Vcc OVP Voltage vs. Ambient Temperature



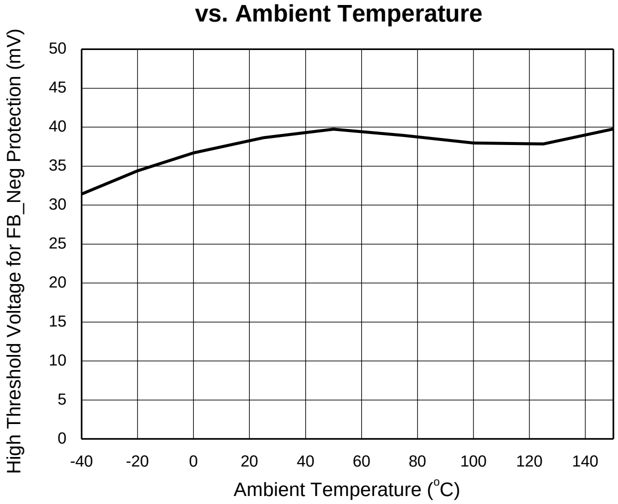
Line Compensation Resistance vs. Ambient Temperature



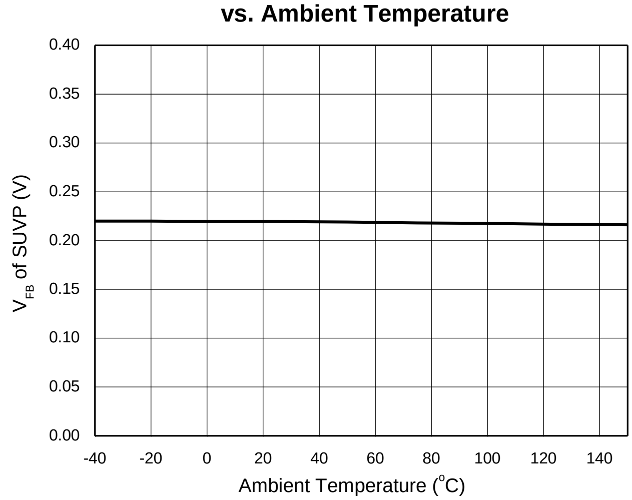
Maximum Off Time vs. Ambient Temperature



High Threshold Voltage for FB_Negative Protection vs. Ambient Temperature



Feedback Voltage of SUVP vs. Ambient Temperature



Operation Principle Description

1. The Conventional PSR Operating Waveforms

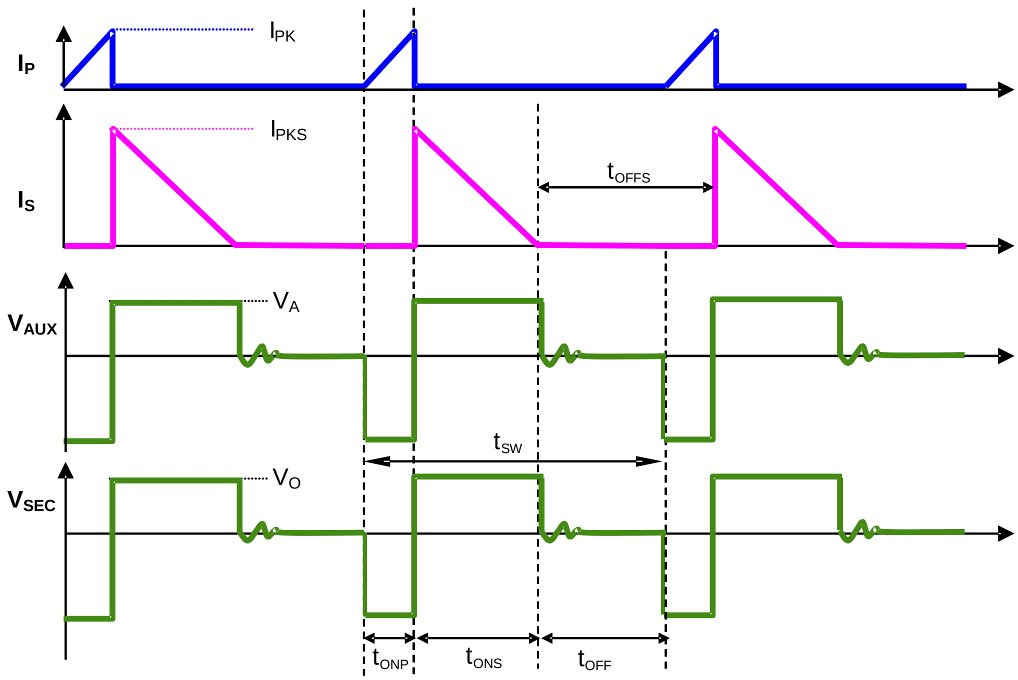


Figure 1. The Operation Waveform of Flyback PSR System

Figure 1 shows the typical waveforms which demonstrate the basic operating principle of AP3781 application. And the parameters are defined as following.

I_P---The primary side current
I_S ---The secondary side current
I_{PK}---Peak value of primary side current
I_{PKS}---Peak value of secondary side current
V_{SEC}---The transient voltage at secondary winding
V_O---The output voltage
V_{AUX}---The transient voltage at auxiliary winding
V_A--- The stable voltage at auxiliary winding when rectification diode is in conducting status, which equals the sum of VCC voltage and the forward voltage drop of auxiliary diode
t_{SW} ---The period of switching frequency
t_{ONP} ---The conduction time when primary side switch is "ON"
t_{ONS} ---The conduction time when secondary side diode is "ON"
t_{OFF} ---The dead time when neither primary side switch nor secondary side diode is "ON"
t_{OFFS} --- The time when secondary side diode is "OFF"

For primary-side regulation, the primary current ip(t) is sensed by a current sense resistor R_{CS} connected to CS pin. The current rises up linearly at a rate of:

$$\frac{dip(t)}{dt} = \frac{V_{IN}(t)}{L_M} \qquad (1)$$

As illustrated in Figure 1, when the current ip(t) rises up to I_{PK}, the primary MOSFET turns off. The constant peak current is given by:

$$I_{PK} = \frac{V_{CS}}{R_{CS}} \qquad (2)$$

Operation Principle Description (continued)

The energy stored in the magnetizing inductance L_M each cycle is therefore:

$$Eg = \frac{1}{2} \times L_M \cdot I_{PK}^2 \qquad (3)$$

So the power transferring from the input to the output is given by:

$$P = \frac{1}{2} \times L_M \times I_{PK}^2 \times f_{SW} \qquad (4)$$

Where, the f_{SW} is the switching frequency. When the peak current I_{PK} is constant, the output power depends on the switching frequency f_{SW}.

2. Constant Voltage Operation

The output voltage is proportional to the auxiliary winding voltage during t_{ONS} period indicated by formula 5, this auxiliary winding voltage is divided by resistors R_{FB1} and R_{FB2} (refer to Figure 5) before inputting to the FB pin. As Figure 2 illustrated, the AP3781 detects the FB voltage at the end of t_{SAMPLE} during t_{ONS} period, the detected voltage which reflects the output voltage is regulated to V_{FB} of 2.4V with the help of the constant voltage control block in AP3781. For system design, adjusting the ratio of R_{FB1} and R_{FB2} can achieve the target output voltage value.

$$V_{AUX} = \frac{N_{AUX}}{N_S} \times (Vo + Vd) \qquad (5)$$

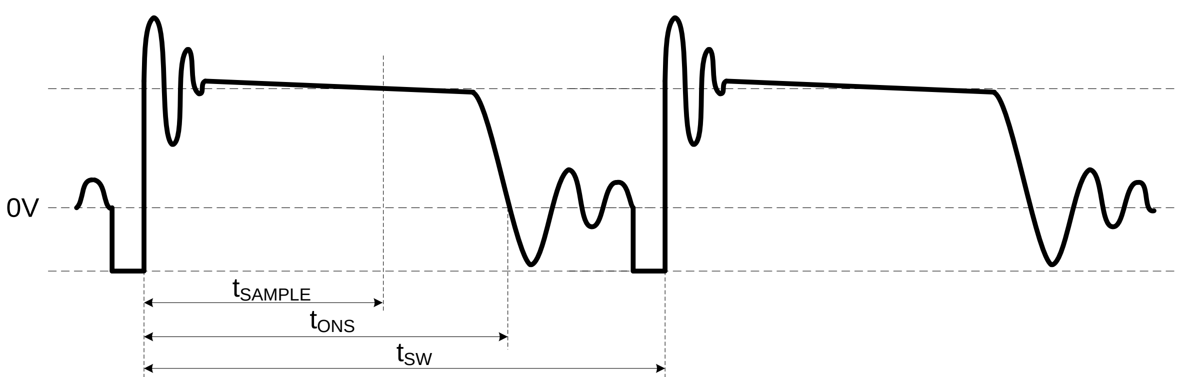


Figure 2. Auxiliary Voltage Waveform

3. Constant Current Control

In AP3781, formula 6 shows the related parameters that determine the output current. To get a constant output current, the V_{CS} and t_{ONS}/t_{SW} is fixed in AP3781 during CC mode. Meanwhile, a reliable control logic is integrated within AP3781 to ensure the system swift smoothly between CC mode and CV mode.

$$I_{OUT} = \frac{1}{2} * \frac{Np}{Ns} * I_{PK} * \frac{t_{ONS}}{t_{SW}} = \frac{1}{2} * \frac{Np}{Ns} * \frac{V_{CS}}{R_{CS}} * \frac{t_{ONS}}{t_{SW}} \qquad (6)$$

4. Multiple Segment Peak Current

In the original PFM PSR system, the switching frequency decreases with the decreasing output current, which will encounter audible noise issue when switching frequency decreases below 20kHz.

In order to avoid audible noise issue and a big drop in efficiency at light load, AP3781 uses a 3-segment primary peak current control method at CV mode, the current sense threshold voltage is piecewise defined, as shown in Figure 3, the low threshold $V_{CS\_H}/3.5$ is set under 2% CC load, the high threshold V_{CS_H} is set above 40% CC load, within the range from 2% to 40%, the threshold V_{CS_M} increases based on the load condition, the V_{CS_M} is carefully calculated inside AP3781 to make the system operate at a reasonable switching frequency which rises above 20kHz at a varying slope.

Operation Principle Description (continued)

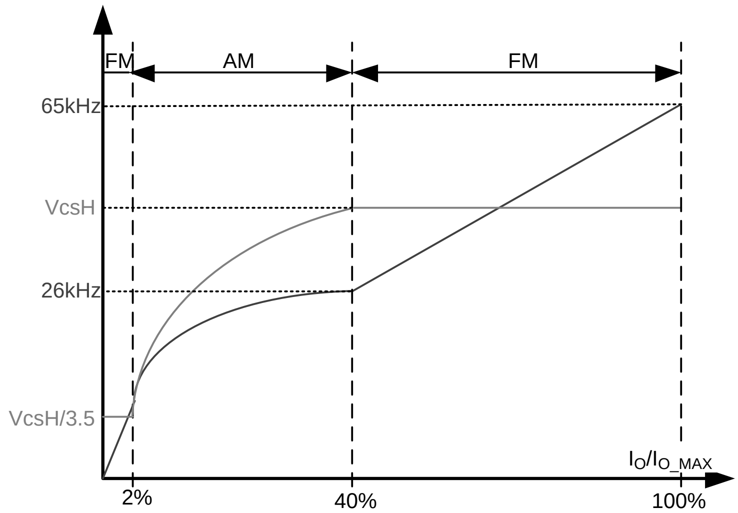


Figure 3. Segment Peak Current and Operating Frequency at CV Mode

5. Sample Time

As shown in Equation 5 and Figure 2, the detected auxiliary voltage reflects the output voltage. To be compatible with different system designs and avoid the turn-off ringing voltage influence on CV sampling, the t_{SAMPLE} is designed to be proportional of t_{ONS}. On the other hand, to alleviate the Vd effect on the accuracy of V_{OUT}, the sample ratio of t_{SAMPLE} to t_{ONS} varies according to load condition. The t_{SAMPLE} is usually 50% of t_{ONS} for the below 2% CC load conditions and 80% of t_{ONS} for the above 40% CC load conditions, within the range from 2% to 40% loading, the sample ratio rises linearly from 50% to 80%

6. Leading Edge Blanking

When the power switch is turned on, a turn-on spike voltage will occur on the V_{CS} sense resistor. To avoid false-termination of the switching pulse, a fixed 420ns leading-edge blanking time is built in. During this blanking period, the current sense comparator is disabled and the primary MOSFET cannot be turned off.

7. Valley Turn-On

When the off time (t_{OFF}) is shorter than 32µs, the AP3781 power system can work with valley turn-on. It can reduce the switching on power losses and achieve high overall efficiency. At the same time, because of valley turn-on the switching frequency has the random jitter feature, which will be of benefit to conductive EMI performance. The valley turn-on can also reduce the power switch turn on spike current and then achieve the better radiative EMI performance.

8. V_{CS} Jitter

Even though the valley turn on function produces the random frequency jitter feature, an active frequency jitter function is added in the AP3781. The active frequency dithering is realized by applying variation on V_{CS} reference (V_{CS_REF}). The V_{CS_REF} is changed every 2 cycles and the period of variation is 12 cycles, which is shown as Figure 4. The variation between V_{CS4} and V_{CS1} is +/-3% using the mean level as a reference.

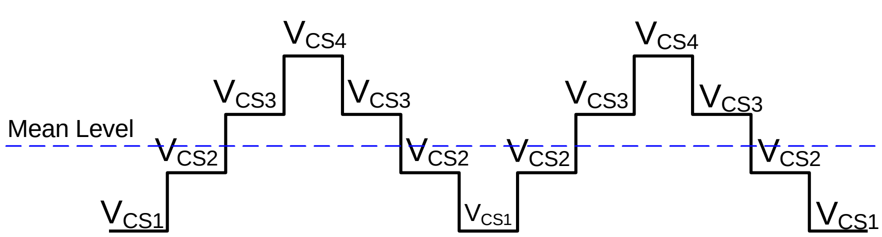


Figure 4. V_{CS} Jitter

Operation Principle Description (continued)

9. Adjustable Line Compensation

In real system, there exists a delay time, from the V_{CS} reaches the inner V_{CS} threshold to the actual switch turn off point. The delay time contains the propagation time of the inner comparator and the driver delay, and it does not change with line voltage. The delay time leads to different primary peak current under different line voltage, which results in different output current in CC mode.

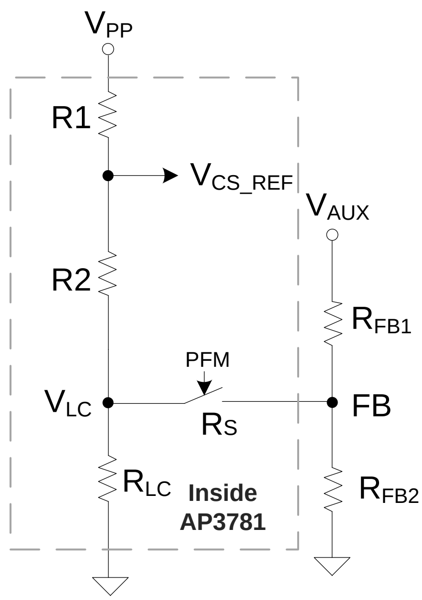


Figure 5. Line Compensation Control Circuit

In order to alleviate the difference under the universal input voltage, the AP3781 integrates the line compensation control circuit shown as Figure 5. During the primary on stage, an inner switcher R_S switches on, and the R_{LC} is much smaller compared with R_{FB2}, so the R_{FB2}'s effect on line compensation can be neglected, the proportional line voltage is detected through R_{FB1} and R_{LC} and is added to the V_{CS} threshold (V_{CS_REF}). The V_{LC} can be derived from the Formula 7:

$$V_{LC} = \frac{\frac{R_{FB1}}{3*R2}*V_{PP} - V_{AUX}}{1 + \frac{R_{FB1}}{3*R2} + \frac{R_{FB1}}{R_{LC}}} \qquad (7)$$

The final compensated V_{CS} is:

$$V_{CS\_REF} = \frac{1}{3}*V_{PP} + \frac{2}{3}*V_{LC} \qquad (8)$$

In the above formulas, V_{PP} is 1.8V at CC mode, R_{LC} is 55Ω, R2 is 60kΩ, R1 is two times of R2, V_{AUX} is the auxiliary winding voltage during primary-on period, and it is proportional to bus voltage. Based on the formula, we can make a conclusion that a smaller R_{FB1} results in deeper line compensation. If we know the delay time, t_{DELAY}, typically 150ns in the AP3781, we can calculate the R_{FB1} as a reference for the system design.

Operation Principle Description (continued)

10. External Cable Compensation

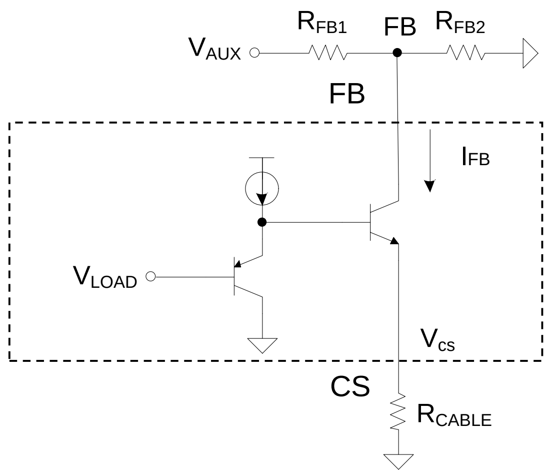


Figure 6. Cable Compensation

$V_{LOAD} = V_{CS}/16.8$, V_{CS} max 900mV. V_{LOAD} is an internal voltage changed with the load.

$I_{FB} = V_{LOAD}/R_{CABLE}$

$$\Delta V_{AUX} = R_{FB1} \cdot I_{FB} = \frac{R_{FB1}}{R_{CABLE}} \cdot V_{LOAD}$$

$$\Delta V_{CABLE} \approx \frac{N_S}{N_{AUX}} \cdot \Delta V_{AUX} = \frac{N_S}{N_{AUX}} \cdot \frac{R_{FB1}}{R_{CABLE}} \cdot V_{LOAD} \qquad (V_{LOAD} / R_{CABLE} / 16 < 8\mu A)$$

(External Cable Compensation)

$$\Delta V_{CABLE} \approx \frac{N_S}{N_{AUX}} \cdot \frac{R_{FB1}}{3.6k} \cdot V_{LOAD} \qquad (V_{LOAD} / R_{CABLE} / 16 > 8\mu A)$$

(Fixed Internal Cable Compensation)

11. Protection

The AP3781 provides versatile protections to prevent the system from damage under various fault conditions. Most protections will trigger auto-recovery mode in which the system will restart as soon as the V_{CC} drops to $V_{OPR(MIN)}$, when the fault conditions are removed, the system will recover to normal operation automatically.

V_{CC} OVP

A V_{CC} OVP threshold is set to protect the IC from damage. When the V_{CC} OVP protection is triggered, the IC will stop outputting drive signal immediately and the system will enter auto-recovery mode.

Secondary-Side Over Voltage Protection (SOVP)

As described above, the FB pin voltage during t_{ONS} reflects the output voltage proportionally, this voltage can be used to realize SOVP. The AP3781 set a higher threshold, $V_{FB(OVP)}$, to shut down the system if the sampled voltage reaches the threshold continuously for 3 switching cycles, the SOVP will be triggered and the system will enter auto-recovery mode.

Secondary-Side Under Voltage Protection (SUVP)

Like SOVP, the AP3781 also integrates the SUVP protection, if the detected voltage on FB pin is lower than $V_{FB(SUVP)}$ for 64ms, the SUVP will be triggered and the system will enter auto-recovery mode.

Operation Principle Description (continued)

Internal Over Temperature Protection (Internal OTP)

If the IC junction temperature exceeds the threshold T_{OTP}, the AP3781 shuts down immediately and enters the hold mode. If the junction temperature decreases by hysteresis temperature T_{HYS}, the AP3781 can recover to normal operation. If not, the power system keeps the hold mode.

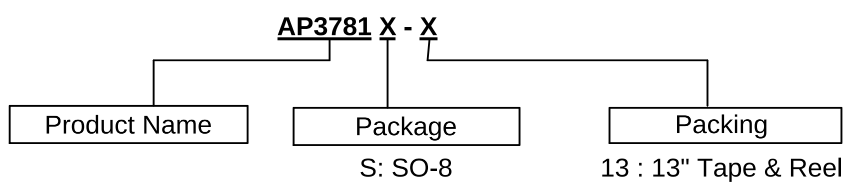
External Over Temperature Protection (External OTP)

The AP3781 provides external over-temperature protection (OTP) by connecting a Negative-Temperature-Coefficient (NTC) resistor from OTP pin to GND. Internally, a current source I_{OTP} is injected to the OTP pin, which generates a voltage proportional to the NTC resistance. At high ambient temperature, the NTC resistance gets lower and results in the OTP pin voltage decreasing. If the OTP pin voltage drops below an internally-set threshold V_{OTP}, then the OTP is triggered, and the AP3781 shuts down immediately and enters the fast auto-recovery mode. The power system will keep fast auto-recovery mode until the ambient temperature decreases and OTP pin voltage increases over the voltage V_{OTP_REC}, thus, the AP3781 can recover to normal operation.

Brown In/ Brown Out Protection

The AP3781 detects the bus voltage at each switching cycle through FB pin during t_{ONP} period, when the V_{CC} reaches V_{TH_ST} after power on, the AP3781 will output one switching pulse to check if the detected bus voltage on FB pin is higher than $V_{FB\_NEG\_H}$. If so, the system will start up normally, otherwise the AP3781 will stop outputting following pulses, then the V_{CC} will drop below $V_{OPR(MIN)}$ and the system will repeat the process described above until the detected FB voltage is higher than $V_{FB\_NEG\_H}$. When the power is off or there is a ditch in bus voltage, if the detected voltage is lower than $V_{FB\_NEG\_H}/3$ for 3 consecutive switching cycles, the IC will shut down and enter auto-recovery mode. This function is very useful when the bulk capacitor is open, or when the heavy load is suddenly released after power off.

Ordering Information

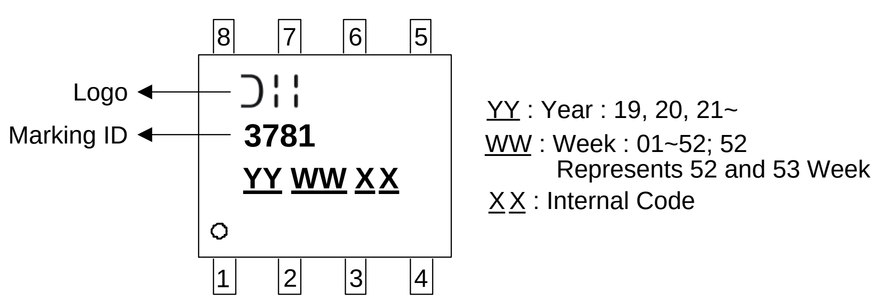


Package	Part Number	Marking ID	Packing
SO-8	AP3781S-13	3781	4000/Tape & Reel

Marking Information

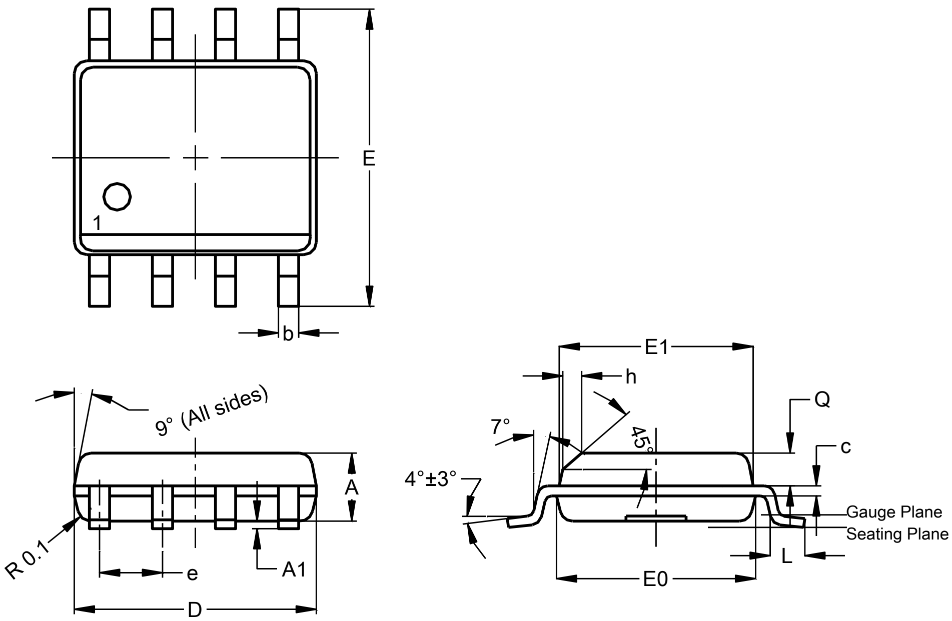
SO-8

(Top View)



Package Outline Dimensions

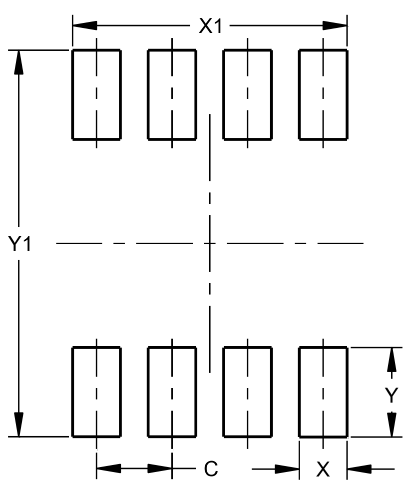
Please see http://www.diodes.com/package-outlines.html for the latest version.



SO-8			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	--	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50

Mechanical Data

- Moisture Sensitivity: MSL Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 e3
- Weight: 0.076 grams (Approximate)

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