Description

The AP39303 is a highly integrated power switcher with a built-in Quasi-Resonant (QR) PWM controller and a 700V high performance power MOSFET. AP39303 is specially designed for offline power supply that requires ultra-low standby power, high-power density and comprehensive protection. Coordinating with secondary side USBPD or quick charger controller to provide a Flyback charger solution.

At no load or light load, the IC will enter the burst mode to minimize standby power consumption. The minimum switching frequency (typical: 24kHz) is set to avoid the audible noise. When the load increases, the IC will enter QR mode with frequency foldback to improve system efficiency and EMI performance. The maximum switching frequency (typical: 120kHz) is set to clamp the QR frequency to reduce switching power loss. Furthermore, the frequency dithering function is built in to reduce EMI emission.

The AP39303 provides an inner high-voltage start-up function through HV pin which can reduce the standby loss. Moreover, The AP39303 integrates a VCC LDO circuitry, allowing the LDO to regulate the wide range V_{CC_IN} to an acceptable value. This makes the AP39303 to be a good choice in wide range output voltage application.

Internal piecewise linear line compensation ensures constant output power limit over entire universal line voltage range.

Comprehensive protection features are included, such as brown out protection, cycle-by-cycle current limit, VCC Over Voltage Protection (VOVP), Secondary-side Output OVP (SOVP) and UVP (SUVP), internal OTP, Over Load Protection (OLP) and pins' fault protection.

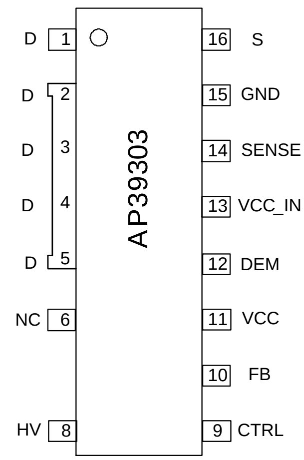
Combined with Diodes Incorporated's synchronous controller APR347, AP39303 system can achieve the higher power conversion efficiency and the better thermal performance.

Features

- Quasi-Resonant Operation under all Line and Load Condition
- Peak Current Mode Control @ DCM
- High-Voltage Startup
- Built-In 700V High Performance Power MOSFET
- Embedded VCC LDO to Guarantee Wide Range V_{CC_IN} Voltage
- Low VCC Charge Current Reduces Standby Power in Output Short Situation
- Adaptive Burst Mode Operation with Output Voltage
- Adaptive Output Power Limit with Output Voltage
- Non-Audible-Noise Quasi-Resonant Control
- Soft Start during Startup Process
- Frequency Fold Back for High Average Efficiency
- Secondary Winding Short Protection with FOCP
- Frequency Dithering for Reducing EMI
- V_{CC} Maintain Mode
- Useful Pin Fault Protection:
  SENSE Pin Floating
  FB/Opto-Coupler Open/Short
- Comprehensive System Protection Feature:
  Programmable External OTP
  Over Load Protection (OLP)
  Brown In/Out Protection
  Secondary Side OVP (SOVP) and UVP (SUVP)
- HSOP-16 (Type SM) Package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

Pin Assignments

(Top View)



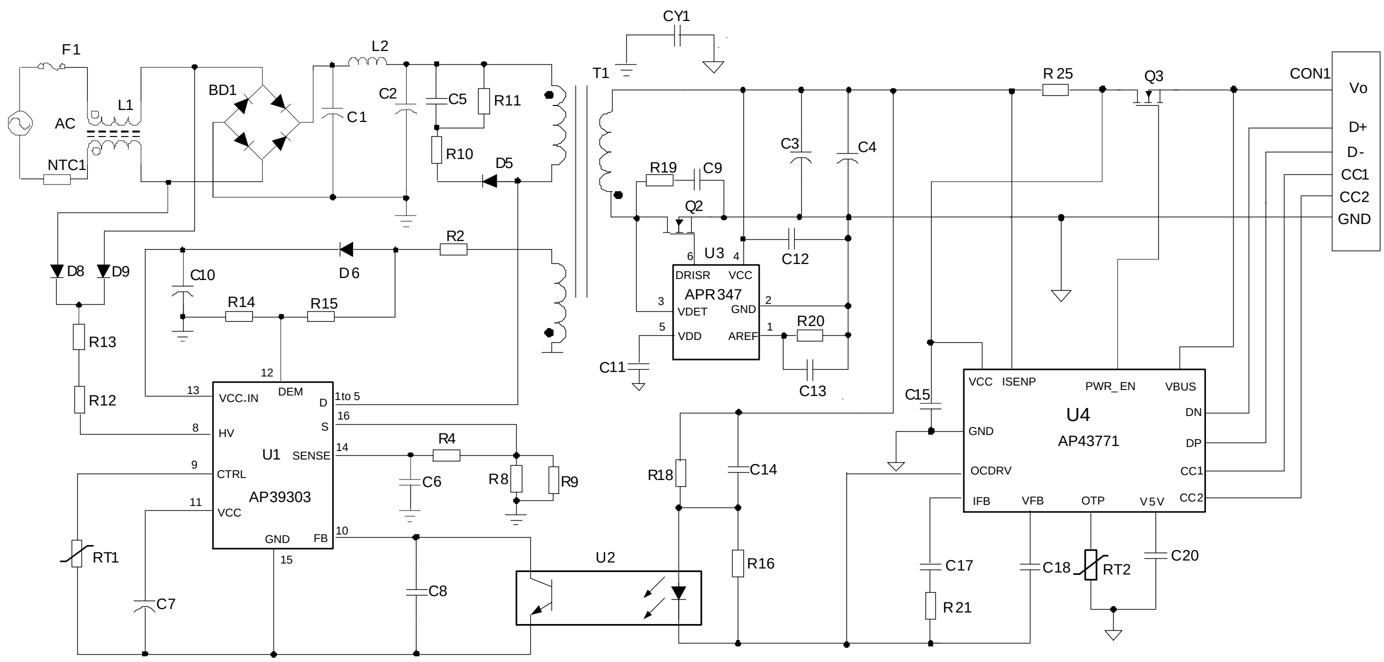
HSOP-16 (Type SM)

Applications

- Switching AC-DC Adapter/Charger
- ATX/BTX Auxiliary Power
- Set-Top Box (STB) Power Supply
- Open Frame Switching Power Supply

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

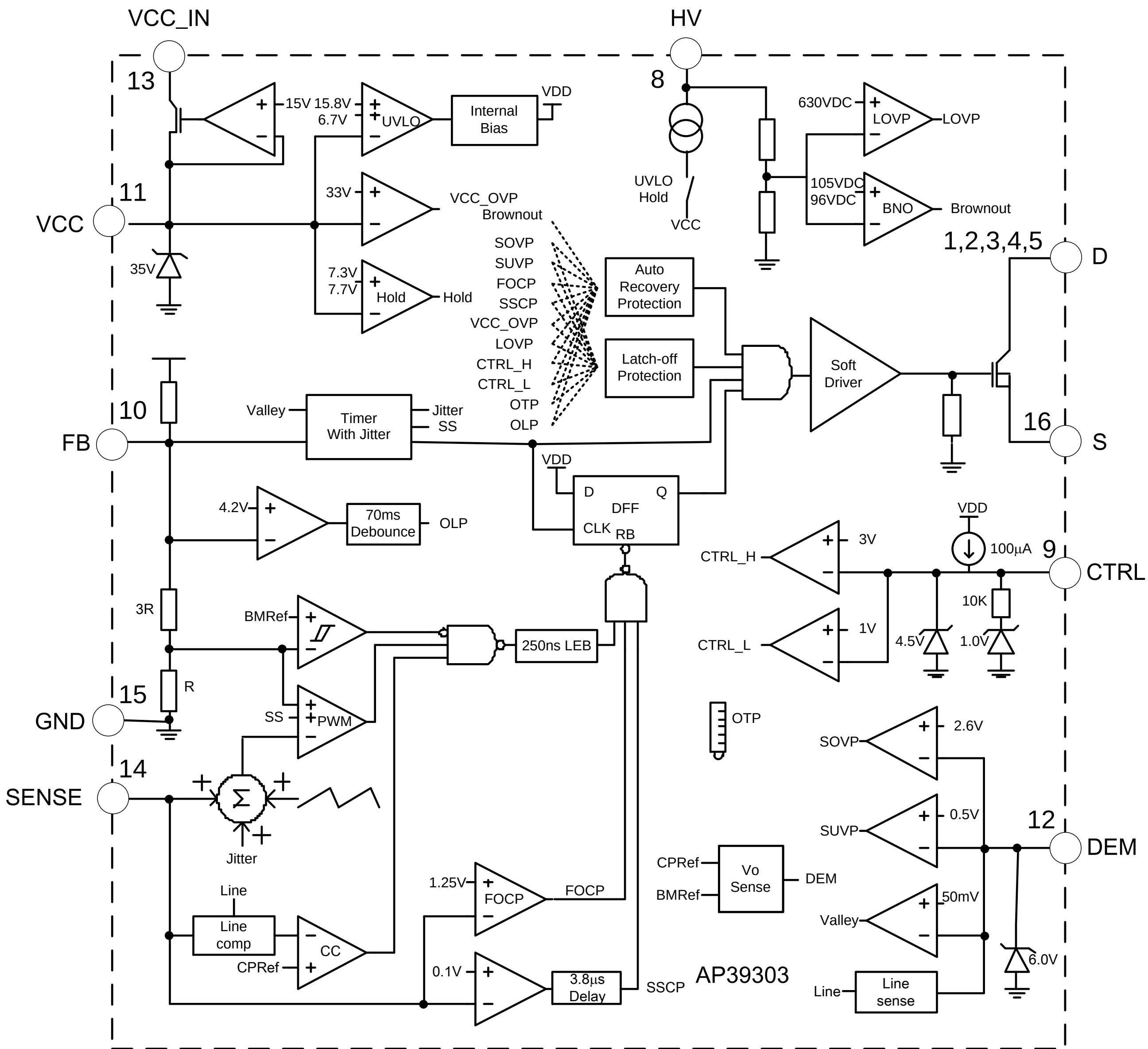
Typical Applications Circuit



Pin Descriptions

Pin Number	Pin Name	Function
1 to 5	D	The Drain of Internal Power MOSFET
6	NC	Suspended
8	HV	High Voltage Input. Sense Line Voltage and Provide Startup Current to V_{CC}
9	CTRL	Programmable External Protection
10	FB	Feedback. Directly Connected to the Opto-Coupler
11	VCC	Supply Voltage of Driver and Control Circuits
12	DEM	Valley Detection for QR Control. Sample V_{OUT} to Realize SOVP and SUVP Protection
13	VCC_IN	Wide Range Input Supply Voltage to Produce V_{CC}
14	SENSE	Sense the Primary Current
15	GND	Signal Ground
16	S	The Source of Internal Power MOSFET

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{HV}	HV Pin Input Voltage	700	V
V_D	Drain Pin Input Voltage	700	V
V_{CC_IN}	LDO Supply Voltage	120	V
V_{CC}	Power Supply Voltage	34	V
I_O	Gate Output Current	350	mA
V_{FB}, V_{SENSE}, V_{CTRL}, V_{DEM}	Input Voltage to FB, SENSE, CTRL, DEM	-0.3 to 7	V
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 5)	77	°C/W
P_D	Power Dissipation at T_A < +25°C	500	mW
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature Range	+150	°C
ESD	Human Body Model (Except HV Pin and VCC_IN Pin) (Note 6)	3,000	V
	Charged Device Model	600	V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

5. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch^2 cooling area.

6. HV devices are ESD sensitive (HBM: V_{HV} = 500V, V_{CC_IN} = 450V).

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	10	28	V
T_A	Ambient Temperature	-40	+85	°C

Electrical Characteristics (@T_A = -40°C to +85°C, V_{CC} = 18V, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage (VCC Pin)						
I_{ST}	Startup Current	—	—	1	15	µA
I_{CC}	Operating Supply Current	V_{FB} = 4V, C_L = 0nF (Note 8)	1.2	1.6	2.2	mA
$I_{CC\text{-}FAULT}$	Operating Current If Fault Occurs	V_{FB} = 4V, V_{SENSE} = 0V (Note 8)	0.25	0.4	0.55	mA
V_{ST}	Startup Voltage	—	14.3	15.8	16.3	V
V_M	V_{CC} Maintain	—	—	7.3	—	V
V_{UVLO}	Shutdown Voltage	—	6.1	6.7	7.1	V
$V_{CC\text{-}OVP}$	V_{CC} OVP	—	32	33	34	V
PWM Section/Oscillator Section						
$f_{OSC\text{-}MAX}$	Maximum Clamp Frequency	(Note 8)	—	120	—	kHz
$f_{OSC\text{-}MIN}$	Minimum Clamp Frequency	(Note 8)	20	24	28	kHz
$f_{OSC\text{-}JITTER}$	Valley Blanking Time Dithering	(Note 8)	—	±12	—	%
t_{DITHER}	Frequency Dithering Period	—	—	4	—	ms
Current Sense Section (SENSE Pin)						
$V_{SENSE\text{-}MAX}$	Current Limit Threshold Voltage	I_{DEM_SOURCE} = 200µA	0.89	0.96	1.04	V
$V_{TH\text{-}FOCP}$	FOCP Voltage	—	—	1.25	—	V
$t_{DELAY\text{-}FOCP}$	FOCP Debounce Time (Note 9)	—	—	7	—	Cycles
t_{LEB}	Leading Edge Blanking Time	—	150	250	350	ns
$V_{TH\text{-}SSCP}$	SSCP Voltage	—	—	100	—	mV
$t_{SOFT\text{-}ST}$	Soft-Start Time	—	3	4	8	ms
$t_{DELAY\text{-}SENSE}$	Sense Propagation Delay (Note 7)	—	—	100	—	ns
Feedback Input Section (FB Pin)						
$K_{FB\text{-}SENSE}$	The Ratio of Input Voltage to Current Sense Voltage (Note 7)	—	—	4	—	V/V
R_{FB}	Input Impedance	—	20	30	40	kΩ
$I_{FB\text{-}SOURCE}$	Source Current	V_{FB} = 0V	0.1	0.2	0.3	mA
G_{QR}	QR Mode Frequency Modulation Slope Versus V_{FB} (Note 7)	—	—	94	—	kHz/V
V_{BURST}	Threshold for Entering Burst Mode	V_{DEM}<0.75V	—	0.66	—	V
		0.75V<V_{DEM}<1.45V	—	0.8	—	V
		V_{DEM}>1.45V	—	0.933	—	V
$t_{ON\text{-}MAX}$	Maximum on Time	(Note 8)	16	18.5	21	µs
$t_{DELAY\text{-}OLP}$	Delay of Over Load Protection (Note 7)	—	—	70	—	ms
$V_{FB\text{-}OLP}$	Over Load Protection (Note 7)	—	—	4.2	—	V
Demagnetization Section (DEM Pin)						
$V_{TH\text{-}DEM}$	De-Magnetization Voltage (Note 7)	—	—	50	—	mV
$V_{CLP\text{-}L}$	Low Level for Clamping Voltage	I_{DEM} = 200µA (Source Current)	-50	-5	—	mV
$V_{CLP\text{-}H}$	High Level for Clamping Voltage	I_{DEM} = -1mA (Sink Current)	—	6	—	V
$V_{TH\text{-}SOVP\text{-}L}$	SOVP Threshold Voltage for Startup	—	1.0	1.1	1.2	V
$V_{TH\text{-}SOVP\text{-}H}$	SOVP Threshold Voltage for Steady State	—	2.5	2.6	2.7	V
$t_{DEB\text{-}SOVP}$	SOVP Debounce Time	—	—	7	—	Cycle

Notes: 7. Guaranteed by design.
8. Data measured in IC test mode.
9. Cycle-by-Cycle limit delay time contains OCP comparator delay time and driver delay time, Guaranteed by design.

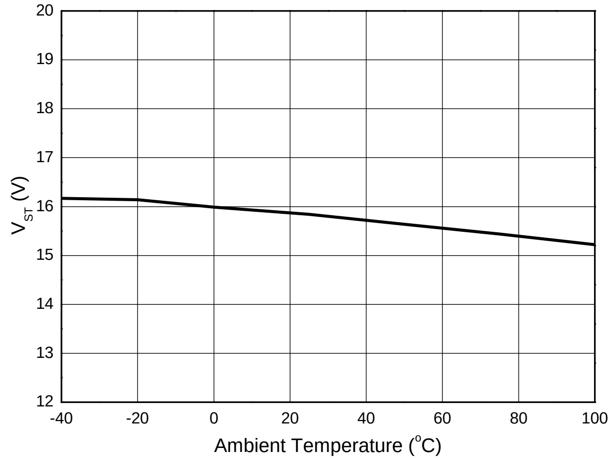
Electrical Characteristics (continued) (@T_A = -40°C to +85°C, V_{CC} = 18V, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Demagnetization Section (DEM Pin)						
$V_{TH\text{-}SUVP\text{-}L}$	SUVP Threshold Voltage for Hiccup	—	—	0.5	—	V
$t_{DEB\text{-}SUVP}$	SUVP Debounce Time	—	—	7	—	Cycle
$t_{BLANK\text{-}SUVP}$	SUVP Blank Time after Startup	—	15	20	25	ms
t_{SAMPLE}	Sample Delay Time (Note 7)	—	—	2	—	µs
LDO Section (VCC_IN Pin/VCC Pin)						
V_{CC}	LDO Regulated Voltage (Power Supply Voltage)	V_{CC} Open, V_{CC_IN} = 10V	9.0	9.8	10	V
		V_{CC} Open, V_{CC_IN} = 40V	14	15	16	V
I_{LDO}	Operating Current	V_{CC}=12V, V_{CC_IN} = 40V	6	8	11	mA
Protection Section (CTRL Pin)						
$I_{CTRL\text{-}SOURCE}$	Source Current	—	-110	-100	-90	µA
$V_{TH\text{-}CTRL\text{-}L}$	Low Threshold	—	0.97	1	1.03	V
$t_{CTRL\text{-}BLANK}$	Blank Time when V_{CTRL} is Low	—	—	20	—	ms
$V_{TH\text{-}CTRL\text{-}H}$	High Threshold Voltage	—	2.9	3	3.1	V
$V_{CTRL\text{-}CLP}$	Clamp Voltage (Note 11)	I_{CTRL}= -2mA	—	4.5	—	V
$t_{DELAY\text{-}HICC}$	Delay of Hiccup Protection (Note 7)	SUVP, SOVP, Line OVP, VCC OVP, FOCP, SSCP, CTRL Pin Protection	—	7	—	Cycles
HV Section (HV Pin)						
$I_{CHARGE\text{-}L}$	Charge Current	V_{CC} = 0V, V_{HV} = 100V	—	0.23	—	mA
$I_{CHARGE\text{-}H}$		V_{CC} = 6V, V_{HV} = 100V	—	2	—	mA
$I_{CHARGE\text{-}FAULT}$	Charge Current if Fault Occurs	V_{CC} = 6V, V_{HV} = 100V	—	65	—	µA
$V_{BR\text{-}IN}$	Brown In Voltage	—	100	105	110	V
$V_{BR\text{-}OUT}$	Brown Out Voltage	—	92	97	102	V
$t_{BR\text{-}IN}$	Delay of Brown In (Note 7)	—	—	100	—	µs
$t_{BR\text{-}OUT}$	Delay of Brown Out (Note 7)	—	—	50	—	ms
V_{LOVP}	Line OVP (Note 7)	—	—	630	—	V
V_{HV}	HV Pin Input Voltage (Note 10)	—	—	—	700	V
Internal OTP Section						
OTP	OTP Threshold (Note 7)	—	—	+150	—	°C
T_{HYS}	OTP Recovery Hysteresis (Note 7)	—	—	+125	—	°C
$t_{DEB\text{-}OTP}$	OTP Debounce Time	—	—	7	—	Cycle
Power MOSFET Section						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	—	700	—	—	V
$R_{DS(ON)}$	Drain-Source On State Resistance	—	—	1.26	2	Ω

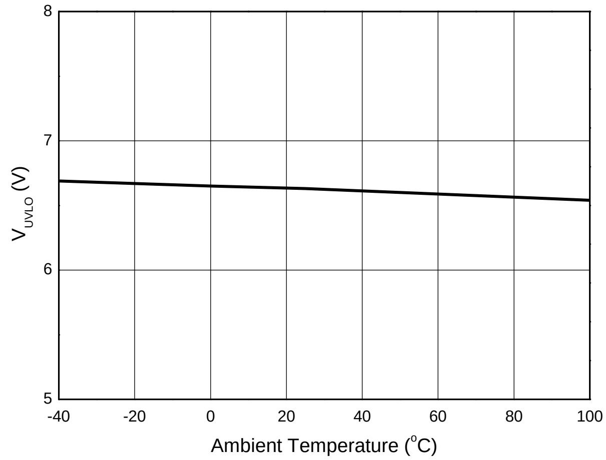
Notes: 7. Guaranteed by design.
8. Data measured in IC test mode.
9. Cycle-by-Cycle limit delay time contains OCP comparator delay time and driver delay time, Guaranteed by design.
10. The drain-source voltage is 80% of V_{DS} in the aging condition.
11. The sourcing current of CTRL pin must be limited below 5mA. Otherwise it may cause permanent damage to the device.

Performance Characteristics

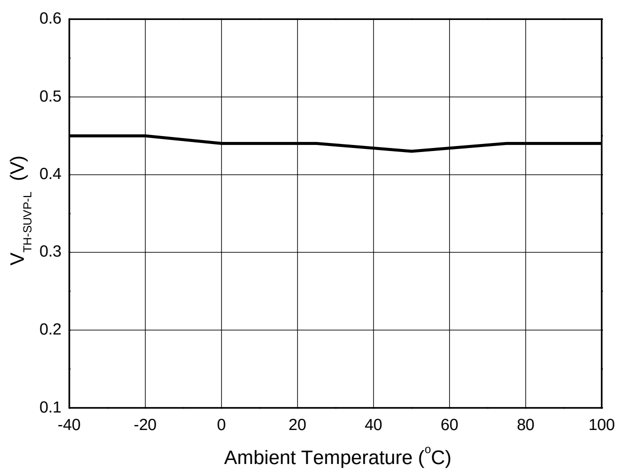
Startup Voltage vs. Ambient Temperature



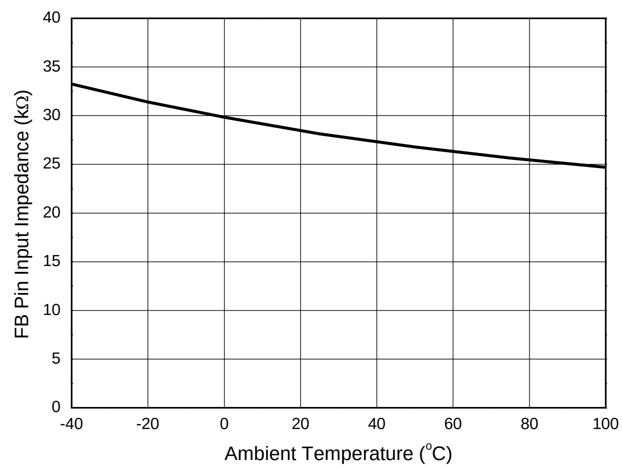
V_{UVLO} vs. Ambient Temperature



$V_{TH-SUVP-L}$ vs. Ambient Temperature

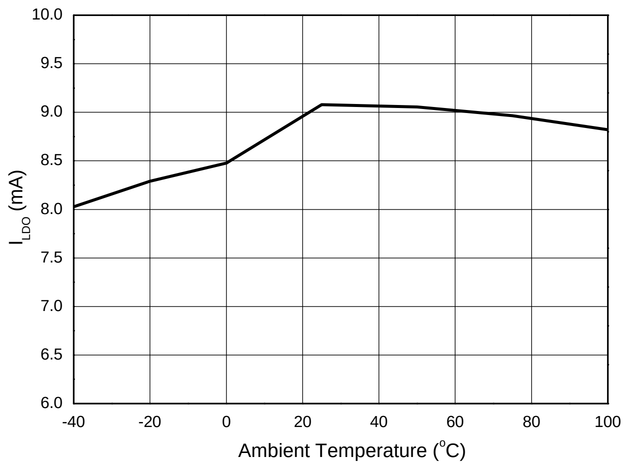


FB Pin Input Impedance vs. Ambient Temperature

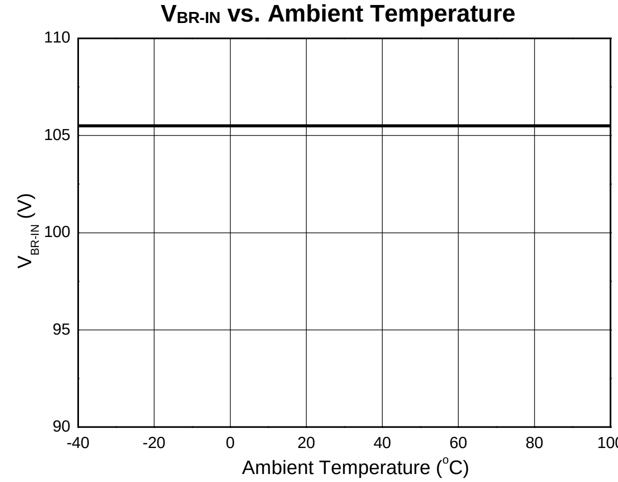


Performance Characteristics (continued)

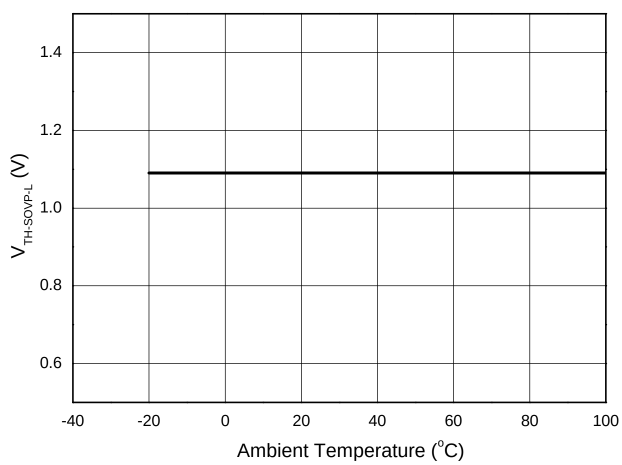
I_{LDO} vs. Ambient Temperature



V_{BR-IN} vs. Ambient Temperature



$V_{TH-SOVP-L}$ vs. Ambient Temperature



Operation Description

Quasi-Resonant (QR) Mode

Quasi-Resonant operation is regarded as a soft switching technology which always turns on the primary MOSFET at the valley status of Drain-to-Source voltage (V_{DS}). Compared to traditional hard switching, QR switching-on can reduce the switching power loss of MOSFET and achieve good EMI behavior without any additional BOM cost.

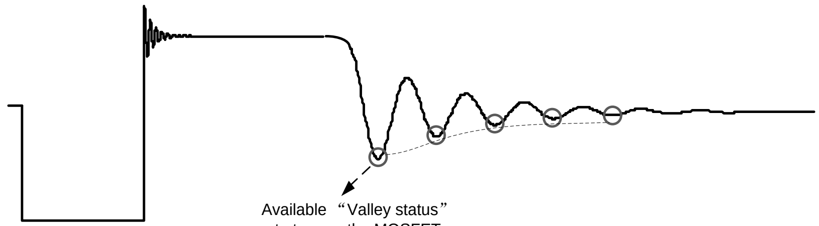


Figure 1

Figure 1 shows the primary MOSFET V_{DS} waveform. When the secondary-side current flows to zero, the primary inductance L_M and the effective MOSFET output capacitor C_{OSS} would be resonant. The valley is detected by DEM pin through a pair of voltage divider. At primary MOSFET turning off time, once the voltage on DEM pin is detected below 50mV, one "valley status" is counted. To prevent the false trigger of the V_{DS} ring caused by leakage inductance, the valley detection function is blanked within the t_{SAMPLE} (2μs, refer to Figure 6) when primary MOSFET turns off.

Each "valley status" of MOSFET V_{DS} will be detected and counted by DEM pin. According to the frequency control strategy of AP39303, one proper "valley status" will be selected to turn on the MOSFET.

Frequency Modulation Strategy

The AP39303 operates with QR mode, green mode and burst mode to achieve the high efficiency performance.

In general, the AP39303 power system operates with first "valley status" under low line and full load condition, in which the maximum primary peak current and transformer flux density occur. The power system designer is required to choose transformer size and switching frequency according to this worst case condition.

With output load decreasing from full load in the first "valley status", the switching frequency of AP39303 increases correspondingly. In order to avoid performance degrading at very high switching frequency operation, there is a fixed 120kHz maximum frequency limitation in AP39303. Since too high switching frequency will lead to the worse performance, the 120kHz frequency limitation is not preferred to reach in system design. Actually AP39303 has built-in reference in FB pin voltage to adjust "valley status" for green mode operation, as shown in Figure 2. When FB pin voltage decreases to a modulating reference, the first "valley status" is forced to shift to other available "valley status".

The AP39303 has the minimum switching frequency limit of 24kHz to avoid audible noise issue. When the switching frequency decrease to 24kHz with output load decreasing, the switching frequency will keep at 24kHz. When FB pin voltage is lower than V_{BURST}, the power system enters burst mode to reduce the power dissipation under very light load condition.

Operation Description (continued)

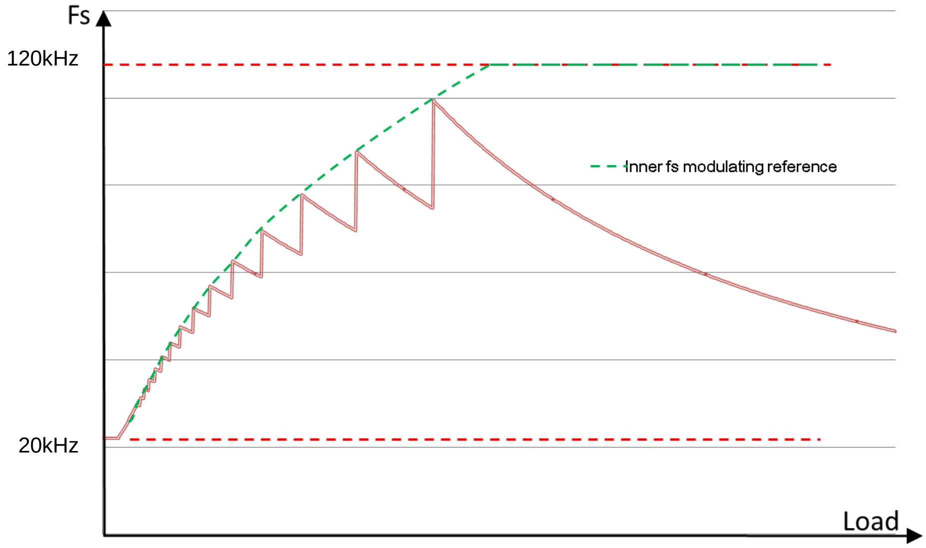


Figure 2

Active Frequency Dithering

To improve the EMI performance, the AP39303 integrates an active frequency dithering function. A consecutive frequency-dithering signal is injected to the SENSE pin after Leading-Edge Blanking (LEB) time. As shown in Figure 3, the frequency-dithering signal is repeating over and over again with a period of 4ms and amplitude of +/-V_{S_JITTER}. With the injection of frequency-dithering signal on SENSE pin, the switching frequency will have a periodical excursion to improve the EMI performance.

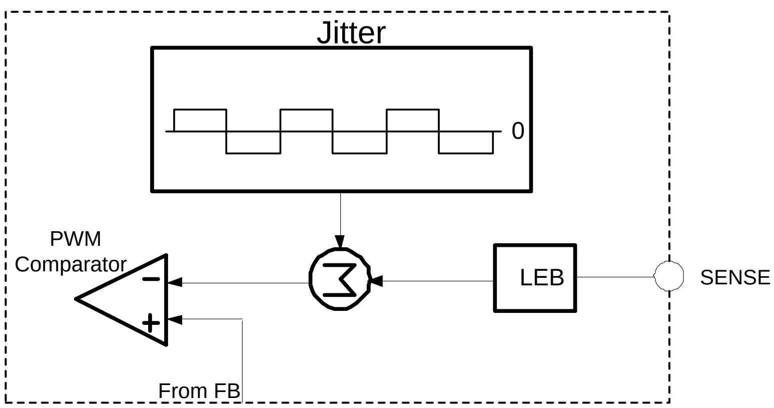


Figure 3

Current Mode PWM Control

The AP39303 operates as a current mode controller; the output switch is turned on by every oscillator cycle and turned off when the primary peak current reaches the threshold level established by the FB pin. The primary current signal is converted to a voltage signal on current sense resistor R_S. The relation between primary peak current (I_{PK}) and V_{FB} is:

$$I_{PK} = V_{FB} / 4R_S$$

Operation Description (continued)

Constant Over Current Protection

Cycle-by-cycle current limit is a popular method to achieve output over current protection. Actually, the turn-off delay of the MOSFET and the higher switching frequency always result in the higher OCP current at high line voltage. To obtain a constant OCP current value with universal input voltage, AP39303 adopts an effective line compensation circuitry. The function block is illustrated in Figure 4. The current I_{DEM} which reflects line voltage is scaled down and inversed to I_{L_OPP} within AP39303, this I_{L_OPP} flows through the inner compensation resistor R_{OPP} and an external filtering resistor R_F, and then the final line compensation voltage is formed as:

$$V_S + \frac{\text{Vindc} * \text{Naux}}{\text{Np} * \text{Rdem} * 21} * (R_{OPP} + R_F) = V_{REF1}$$

Where V_S is the sense voltage of R_S

As above formula indicates, changing the compensation voltage at different line voltage is a good way to balance the OCP current. In a real system, usually keep the R_{DEM} value fixed (220kΩ is recommended). To change the line compensation voltage, a good solution is to change R_F. Whenever the R_F is changed, adjust the C_F at the same time to offer an enough RC time to filter the spike on SENSE pin.

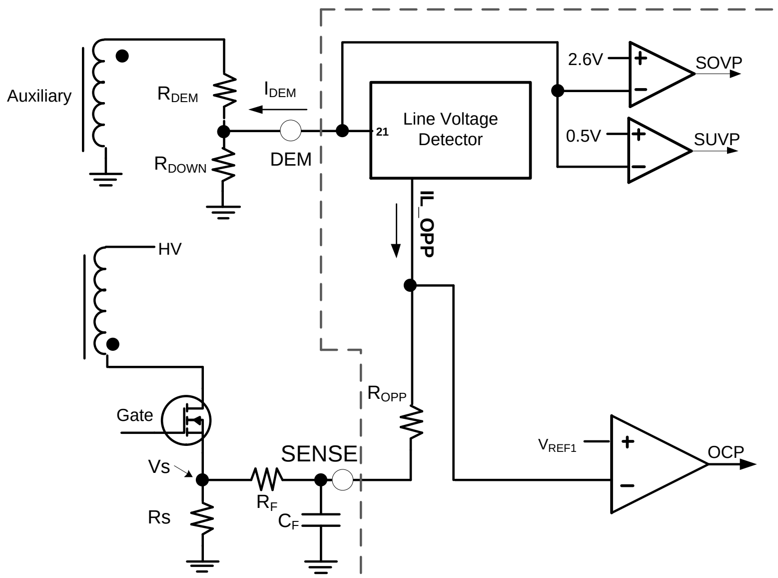


Figure 4

HV Start-Up Circuit

A built-in HV startup circuit in AP39303 can help to simplify the power system design for ultra-low standby application. For AP39303, there are two HV Start-Up charging current: the $I_{CHARGE-L}$ when V_{CC} is lower than 3V and the $I_{CHARGE-H}$ when the V_{CC} voltage rises above 3V, which can prevent the IC from overheat when V_{CC} short-to-GND fault happens. The HV startup circuit will stop working and have no additional power dissipation when V_{CC} voltage reaches the V_{ST}, then the AP39303 starts working and will supply energy to V_{CC} from auxiliary winding.

However, the charging process described above is only for the normal system startup condition. Once some system faults occur and the protection process is triggered, AP39303 will shut down and V_{CC} voltage will begin to decrease. The HV startup circuit starts working again when V_{CC} voltage decreases below $V_{CC-UVLO}$, and charges the V_{CC} capacitor with current of $I_{CHARGE-FAULT}$. This special design can reduce the input power dissipation when system fault happens, especially for output short condition. The HV Start-Up circuit working process is illustrated in Figure 5.

Operation Description (continued)

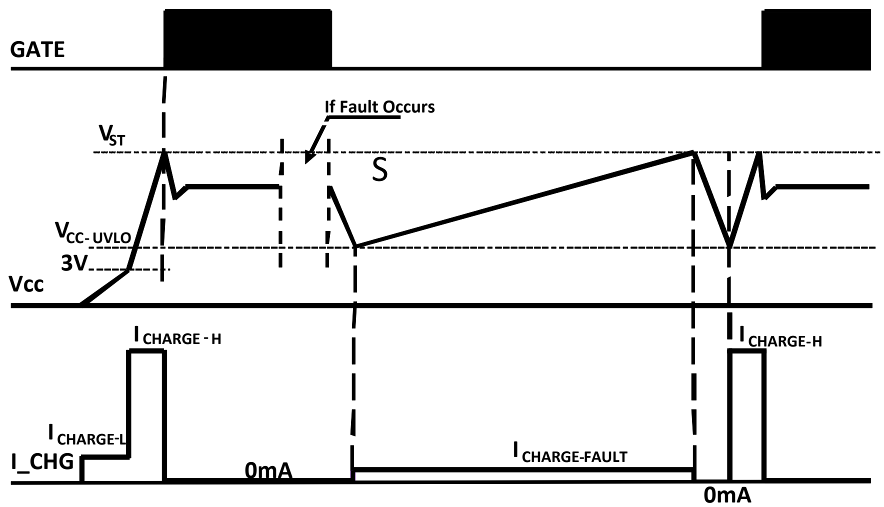


Figure 5

Built-In V_{CC} LDO

The AP39303 integrates a V_{CC} LDO circuitry, the LDO regulates the wide range V_{CC_IN} which is rectified from auxiliary winding to an acceptable value. It makes the AP39303 a good choice in wide range output voltage application.

Brown In/Out Protection

To avoid potential high-current stress at low line voltage, the AP39303 introduces a reliable brownout protection. The AC line voltage is detected through HV pin, a pair of high-voltage diodes are connected to the AC line which will rectify the AC input voltage to a double-frequency positive voltage referring to GND, a 20kΩ resistor is recommended to be added to improve the surge immunity. When the voltage across HV pin is higher than V_{BR-IN} for about 100µs of t_{BR-IN} and V_{CC} reaches V_{ST}, the system starts to work. If the HV pin voltage falls below V_{BR-OUT} and lasts for 50ms of t_{BR-OUT}, the system will shut down until the line voltage rises over its brown-in voltage again.

SOVP/SUVP Protection

The AP39303 provides output OVP and UVP protection function. The auxiliary winding voltage during secondary rectifier conducting period reflects the output voltage. A voltage divide network is connected to the auxiliary winding and DEM pin, the DEM pin will detect the equivalent output voltage with a delay of t_{SAMPLE} from the falling edge of GATE driver signal, as shown in Figure 6. The detected voltage will be compared to the SOVP and SUVP threshold voltage $V_{TH-SOVP}$ and $V_{TH-SUVP}$. If the SOVP or SUVP threshold is reached continuously by 7 switching cycles, the SOVP or SUVP protection will be triggered, the AP39303 will shut down and the system will restart when the V_{CC} voltage falls below the UVLO voltage.

To prevent from false-trigger of SUVP during start up process, a blank time of $t_{BLANK-SUVP}$ is set during which the SUVP protection function is ignored.

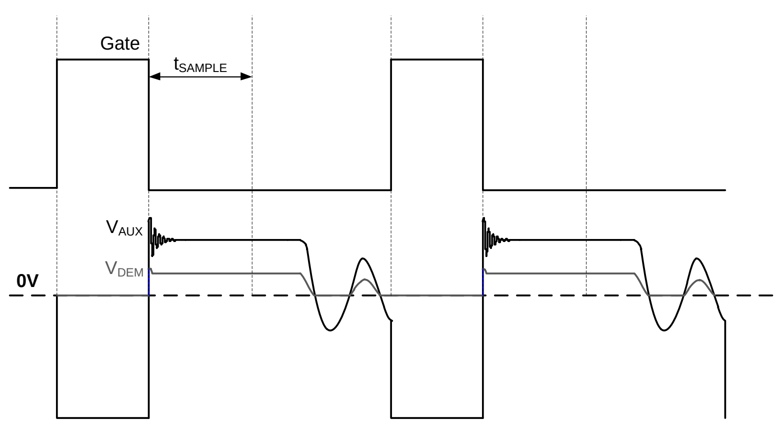


Figure 6

Operation Description (continued)

Externally Triggered Protection

The AP39303 reserves flexible protection mode for power design. The CTRL pin can achieve external programmable protection. A high threshold of $V_{TH\text{-}CTRL\text{-}H}$ is set for any over voltage protection, if the CTRL pin voltage is higher than the threshold for 7 switching cycles, the CTRL-High protection will be triggered. A low threshold of $V_{TH\text{-}CTRL\text{-}L}$ is usually used for external over temperature protection. To realize the external OTP, a proper NTC should be connected from the CTRL pin to the ground. An inner current of 100µA flows through the NTC from the CTRL pin. If the CTRL pin voltage is lower than the $V_{TH\text{-}CTRL\text{-}L}$ for 32ms duration at least, the CTRL-Low protection will be triggered. Whenever the protection is triggered, the system will stop the output drive signal and will restart after the V_{CC} voltage falling below the UVLO voltage.

System Protection

LOVP, FOCP, SSCP, VCC OVP, OTP

The AP39303 provides versatile protection to ensure the reliability of the power system. LOVP achieves line voltage overvoltage protection, if the detected AC line voltage is higher than V_{LOVP} for 7 switching cycles, the LOVP protection will be triggered. FOCP protection is an ultra-fast short-current protection which is helpful to avoid catastrophic damage of the system when the secondary rectifier is short. The primary peak current will be monitored by SENSE pin through a primary sense resistor, whenever the sampled voltage reaches the threshold of $V_{TH\text{-}FOCP}$ for 7 switching cycles continuously, the FOCP protection will be activated to shut down the switching pulse. SSCP might be triggered at ultra-low DC bus voltage condition or other failure condition that short the SENSE pin to ground. The SSCP module senses the voltage across the primary sense resistor with a delay of 3µs after the rising edge of primary GATE signal, this sensed signal is compared with $V_{TH\text{-}SSCP}$. If it is lower than $V_{TH\text{-}SSCP}$ for 7 switching cycles, the SSCP protection will be triggered and the drive signal will be disabled. All these protections described above will restart the system when the V_{CC} voltage falls below UVLO. Although the external OTP can be easily implemented through CTRL pin, the AP39303 still reserves the inner OTP with a hysteresis for any necessary use.

V_{CC} Maintain Mode

During light-load or transient-load condition, V_{FB} will drop and be lower than V_{BURST}, thus the PWM drive signal will be stopped, and there is no energy for transferring to the output. Therefore, the IC V_{CC} supply voltage may decrease to the UVLO threshold voltage and system may enter the unexpected restart mode. To avoid this, the AP39303 holds a so-called V_{CC} maintain mode which can supply energy to V_{CC}.

When V_{CC} decreases to a setting threshold as V_M, the V_{CC} maintain mode will be awaked and a charging current of $I_{CHARGE\text{-}H}$ will flow to the V_{CC} pin. With V_{CC} maintain mode, the V_{CC} is not easy to touch the shutdown threshold during the startup process and transient load condition. This will also simplify the system design. The minimum V_{CC} voltage is suggested to be designed a little higher than V_{CC} maintain threshold thus can achieve the best balance between the power loss and step load performance.

Leading-Edge Blanking Time

A narrow spike on the leading edge of the current waveform can usually be observed when the power MOSFET is turned on. A 250ns leading-edge blank is built-in to prevent the false-trigger caused by the turn-on spike. During this period, the current limit comparator and the PWM comparator are disabled and the gate driver cannot be switched off.

At the time of turning-off the MOSFET, a negative undershoot (maybe larger than -0.3V) can occur on the SENSE pin. So it is strongly recommended to add a small RC filter or at least connect a resistor “R” on this pin to protect the IC (Shown as Figure 7).

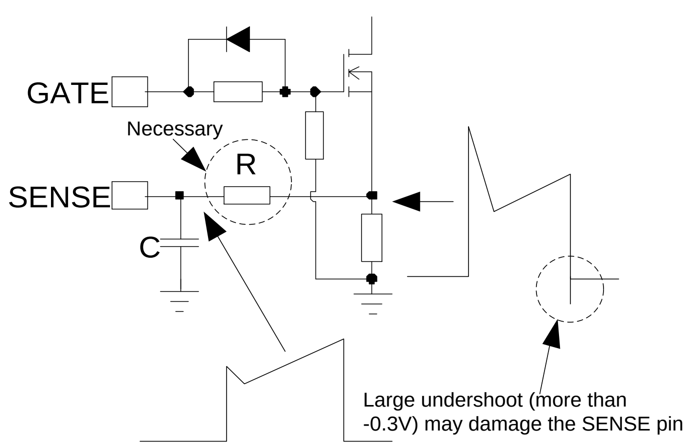
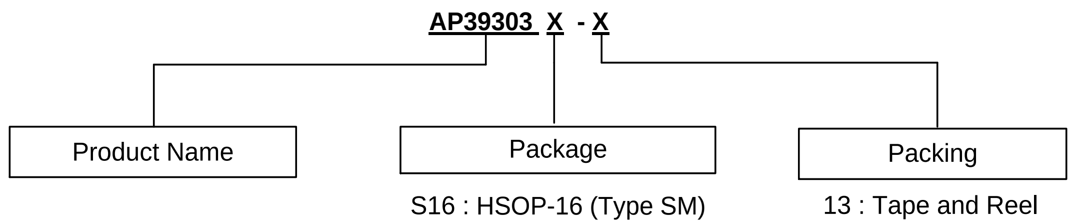


Figure 7

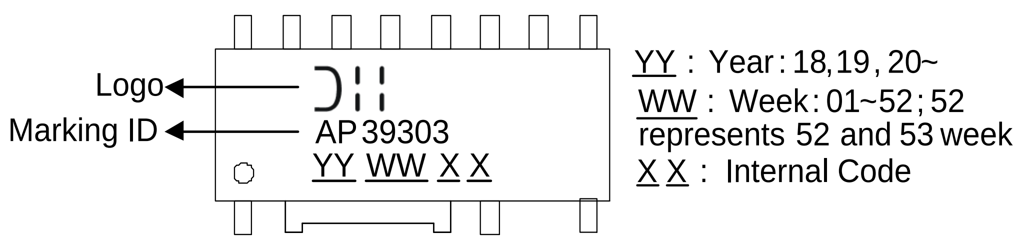
Ordering Information



Part Number	Package	Marking ID	13''Tape and Reel	
			Quantity	Part Number Suffix
AP39303S16-13	HSOP-16 (Type SM)	AP39303	4000/Tape and Reel	-13

Marking Information

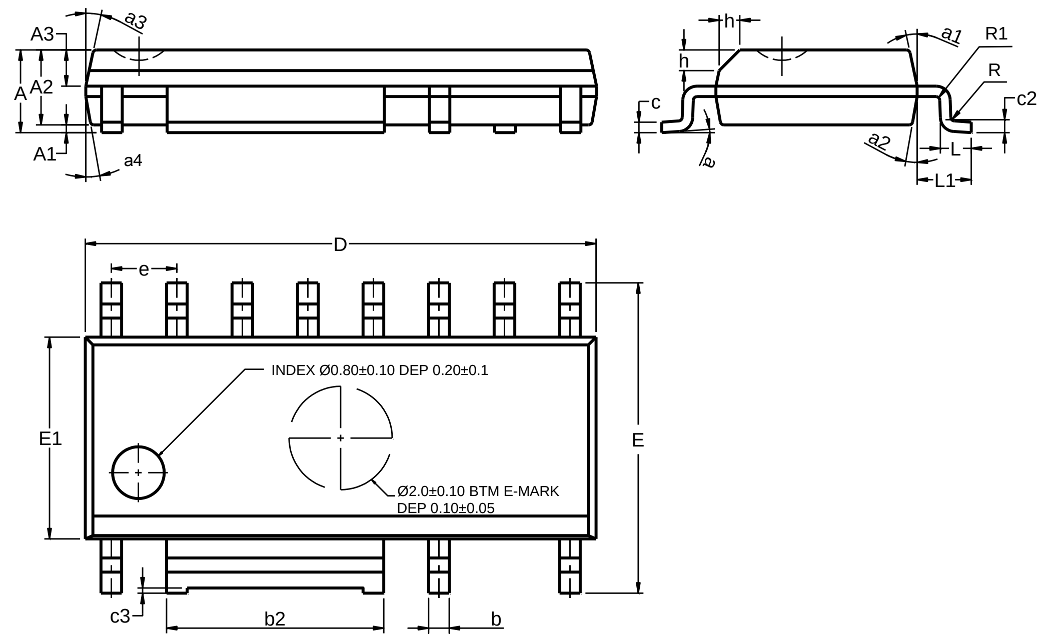
(Top View)



Package Outline Dimensions (All dimensions in mm)

Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: HSOP-16 (Type SM)



HSOP-16 (Type SM)			
Dim	**Min**	**Max**	**Typ**
A	1.35	1.75	1.60
A1	0.10	0.25	0.15
A2	1.25	1.65	1.45
A3	0.55	0.75	0.65
b	0.36	0.51	--
b2	4.17	4.32	--
c	0.17	0.25	--
c2	0.25BSC		
c3	0.00	0.15	--
D	9.80	10.00	9.90
E	5.80	6.20	6.00
E1	3.80	4.00	3.90
e	1.27BSC		
h	0.30	0.50	0.40
L	0.45	0.80	0.60
L1	1.04REF		
R	0.07	--	--
R1	0.07	--	--
a	0°	8°	--
a1	10°	14°	12°
a2	8°	12°	10°
a3	10°	14°	12°
a4	8°	12°	10°
All Dimensions in mm			

Mechanical Data

- Moisture Sensitivity: MSL Level 3 per JESD22-A113
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 (e3)
- Weight: 0.168 grams (Approximate)

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