

## Description

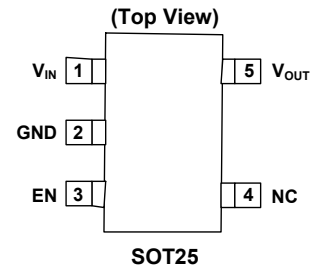
The AP7315Q is a low dropout regulator with high output voltage accuracy, low  $R_{DS(ON)}$ , high PSRR, low output noise, and low quiescent current. This regulator is based on a CMOS process.

The AP7315Q is available with fixed output voltage variants with an enable input to turn it on and off. It is available with output discharge (AP7315DQ) and without (AP7315Q) output discharge function.

With its low power consumption and line and load transient responses, the AP7315Q is well suited for noise sensitive automotive applications.

The AP7315Q is qualified to AEC-Q100 Grade 1 in SOT25 and is Automotive Compliant, supporting PPAPs.

## Pin Assignments



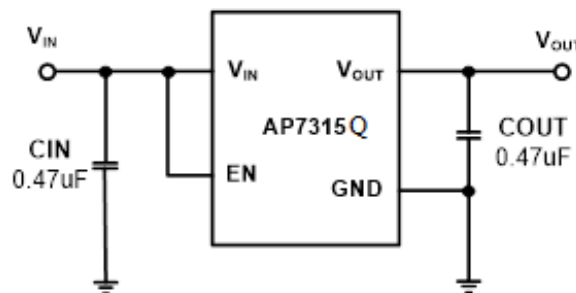
## Features

- Wide V<sub>IN</sub> Range: 1.7V to 5.25V
- -40°C to +125°C Temperature Range
- Guarantee Output Current, 150mA
- V<sub>OUT</sub> Accuracy ±1%
- Ripple Rejection 75dB at 1kHz
- Low Output Noise, 60µVrms from 10Hz to 100kHz
- Quiescent Current as Low as 35µA
- V<sub>OUT</sub> Fixed 1.1V to 3.3V
- Moisture Sensitivity: Level 1 Per J-STD-020
- Terminals: Finish - Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 ③
- Weight: 0.016 grams (Approximate)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen- and Antimony-Free, Green Device (Note 3)**
- **The AP7315Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**

<https://www.diodes.com/quality/product-definitions/>

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds .

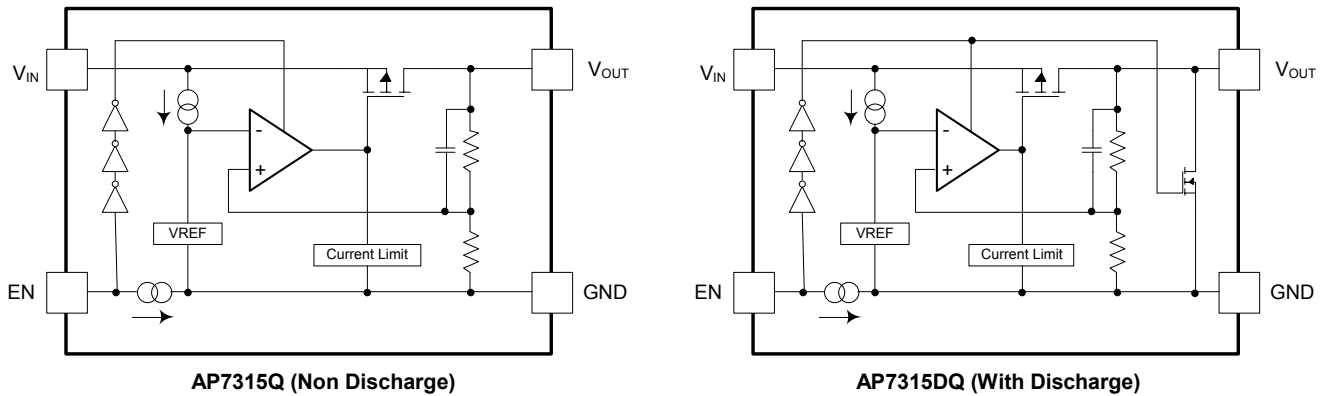
## Typical Applications Circuit



**Pin Descriptions**

Pin Number	Pin Name	Function
1	V <sub>IN</sub>	Power Input Pin
2	GND	Ground
3	EN	Enable Pin This pin should be driven either high or low and must not be floating. Driving this pin high enables the regulator, and pulling it low puts the regulator into shutdown mode.
4	NC	No Connection
5	V <sub>OUT</sub>	Power Output Pin

**Functional Block Diagram**



**Absolute Maximum Ratings** (Note 4) (@ T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body Mode ESD Protection	>2	KV
ESD CDM	Charge Device Model	±500	V
V <sub>IN</sub>	Input Voltage	6.0	V
V <sub>EN</sub>	Input Voltage EN	6.0	V
V <sub>OUT</sub>	Output Voltage	-0.3 to V <sub>IN</sub> +0.3	V
I <sub>OUT</sub>	Output Current	300	mA
P <sub>D</sub>	Power Dissipation	400	mW
T <sub>J</sub>	Operating Junction Temperature	-40 to +150	°C
T <sub>STG</sub>	Storage Temperature	-55 to +150	°C

Note: 4. a) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.  
 b) Ratings apply to ambient temperature at +25°C. The JEDEC High-K board design used to derive this data is a 2in. × 2in. multilayer board with 1oz. internal power and ground planes and 2oz. copper traces on the top and bottom of the board.

**Recommended Operating Conditions** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
$V_{IN}$	Input Voltage Range	1.7	5.25	V
$I_{OUT}$	Output Current	0	150	mA
$T_J$	Operating Junction Temperature	-40	+125	$^\circ\text{C}$
$T_A$	Operating Ambient Temperature (Note 5)	-40	+125	$^\circ\text{C}$

Note: 5. Ambient temperature range is subject to the junction temperature not exceeding  $125^\circ\text{C}$ .

**Electrical Characteristics**

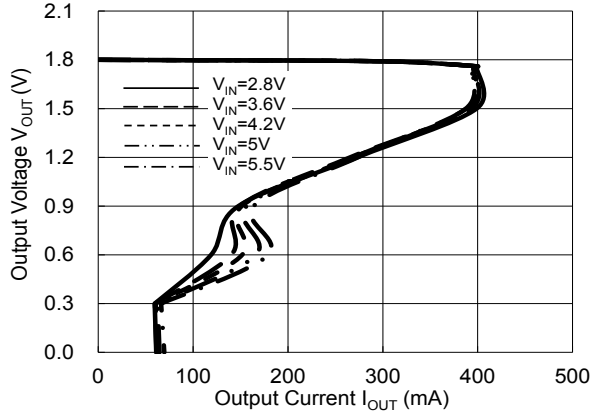
(@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.  $V_{EN} = V_{IN} = V_{OUT} + 1.0\text{V}$ ,  $C_{IN} = C_{OUT} = 0.47\mu\text{F}$ ,  $I_{OUT} = 1.0\text{mA}$ )

Parameter	Conditions	Min	Typ	Max	Units	
Output Voltage Accuracy (Note 6)	$V_{OUT} \geq 2.0\text{V}$ , $V_{IN} = V_{OUT} + 1\text{V}$ , $T_A = +25^\circ\text{C}$	$V_{OUT} \times 0.99$	$V_{OUT}$	$V_{OUT} \times 1.01$	V	
	$V_{OUT} < 2.0\text{V}$ , $V_{IN} = V_{OUT} + 1\text{V}$ , $T_A = +25^\circ\text{C}$	$V_{OUT} - 20\text{mV}$	$V_{OUT}$	$V_{OUT} + 20\text{mV}$	V	
Line Regulation ( $dV_{OUT}/dV_{IN}/V_{OUT}$ )	$V_{IN} = (V_{OUT - Nom} + 1.0\text{V})$ to $5.25\text{V}$ , $I_{OUT} = 1.0\text{mA}$	—	0.02	0.1	%/V	
Load Regulation ( $dV_{OUT}/V_{OUT}/dI_{OUT}$ )	$V_{IN} = V_{OUT - Nom} + 1.0\text{V}$ , $I_{OUT} = 1\text{mA}$ to $150\text{mA}$	—	0.5	1.0	%/A	
Quiescent Current (Note 7)	$I_{OUT} = 0\text{mA}$	20	35	60	$\mu\text{A}$	
	$I_{OUT} = 150\text{mA}$	30	60	100		
$I_{STANDBY}$	$V_{EN} = 0\text{V}$ (Disabled)	—	0.01	1.0	$\mu\text{A}$	
Output Current	—	150	—	—	mA	
Fold-back Short Current (Note 8)	$V_{OUT}$ Short to Ground	—	55	—	mA	
PSRR (Note 9)	$V_{IN} = (V_{OUT} + 1\text{V})V_{DC} + 0.2V_{p-pAC}$ , $V_{OUT} \geq 1.8\text{V}$ , $I_{OUT} = 30\text{mA}$	—	75	—	dB	
Output Noise Voltage (Notes 9, 10)	$BW = 10\text{Hz}$ to $100\text{kHz}$ , $I_{OUT} = 30\text{mA}$	—	60	—	$\mu\text{Vrms}$	
Dropout Voltage (Note 11)	$I_{OUT} = 150\text{mA}$	$1.1\text{V} \leq V_{OUT} < 1.5\text{V}$	—	0.50	0.64	V
		$1.5\text{V} \leq V_{OUT} < 1.7\text{V}$	—	0.38	0.49	
		$1.7\text{V} \leq V_{OUT} < 2.0\text{V}$	—	0.34	0.44	
		$2.0\text{V} \leq V_{OUT} < 2.5\text{V}$	—	0.28	0.38	
		$2.5\text{V} \leq V_{OUT} < 2.8\text{V}$	—	0.22	0.32	
		$2.8\text{V} \leq V_{OUT} \leq 3.3\text{V}$	—	0.21	0.29	
Output Voltage Temperature Coefficient	$I_{OUT} = 30\text{mA}$ , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	—	$\pm 30$	—	ppm/ $^\circ\text{C}$	
EN Input Low Voltage	—	0	—	0.5	V	
EN Input High Voltage	—	1.3	—	5.25	V	
EN Input Leakage	$V_{EN} = 0$ , $V_{IN} = 5.0\text{V}$ or $V_{EN} = 5.0\text{V}$ , $V_{IN} = 0\text{V}$	-1.0	—	+1.0	$\mu\text{A}$	
On Resistance of N-channel for Auto-Discharge (Note 12)	$V_{IN} = 4.0\text{V}$ , $V_{EN} = 0\text{V}$ (Disabled)	—	30	—	$\Omega$	
Thermal Resistance (Note 13) Junction to Ambient ( $\Theta_{JA}$ )	—	—	179	—	$^\circ\text{C/W}$	
Junction to Case ( $\Theta_{JC}$ )	—	—	52	—		

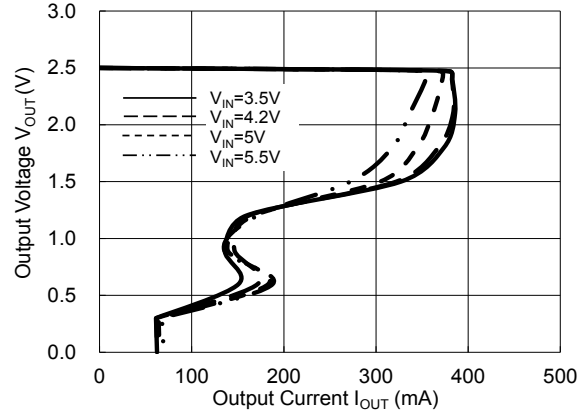
- Notes:
- Potential multiple grades based on following output voltage accuracy.
  - Quiescent current is defined here is the difference in current between the input and the output.
  - Short circuit current is measured with  $V_{OUT}$  pulled to GND.
  - This specification is guaranteed by design.
  - To make sure lowest environment noise minimizes the influence on noise measurement.
  - Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value
  - AP7315Q has 2 options for output, built-in discharge and non-discharge.
  - Thermal impedances measured on PCB of type and size with which top layer and bottom layer metal coverage

**Typical Characteristics**

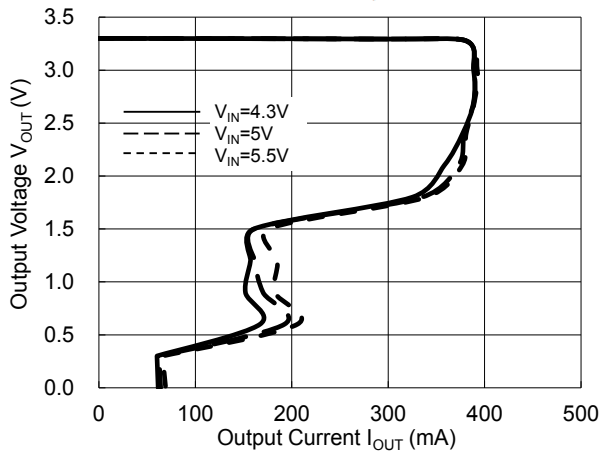
**Output Voltage vs. Output Current**  
AP7315Q-18



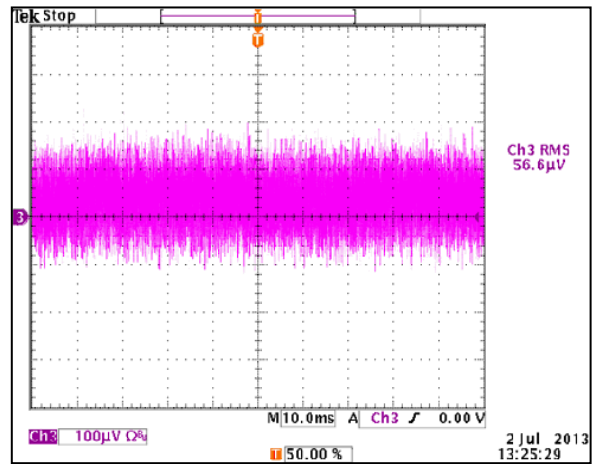
**Output Voltage vs. Output Current**  
AP7315Q-25



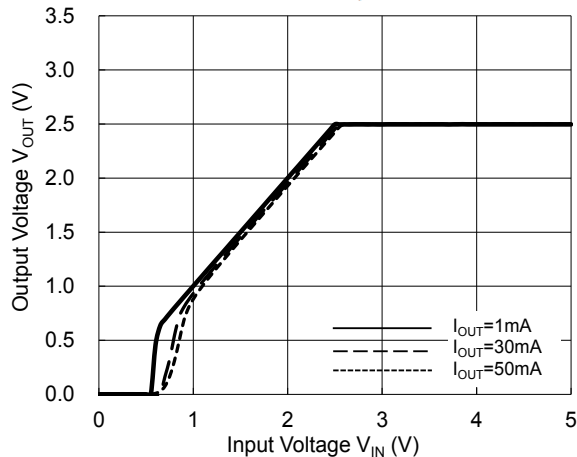
**Output Voltage vs. Output Current**  
AP7315Q-33



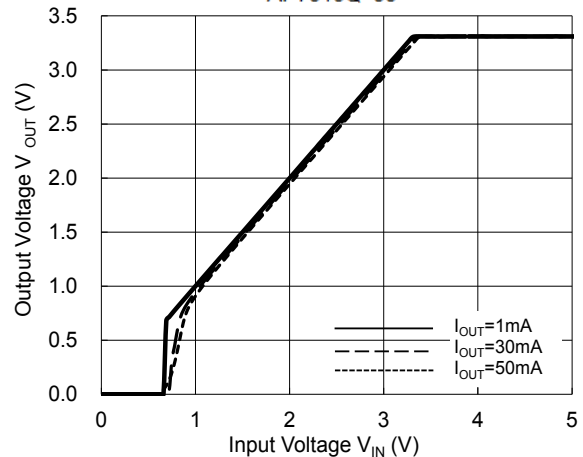
**Output Noise (AP7315Q-33)**



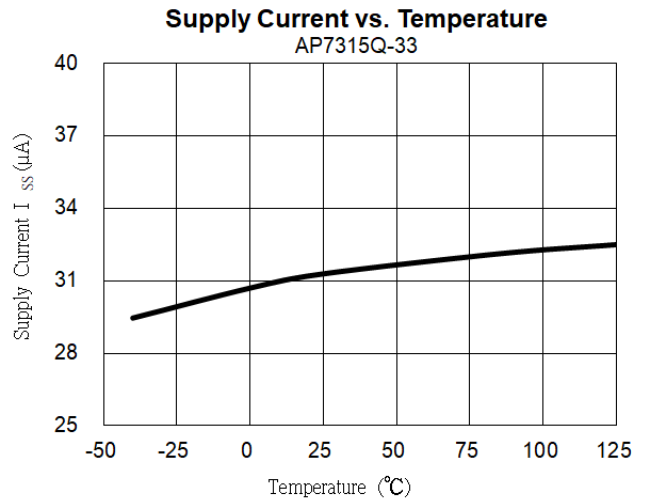
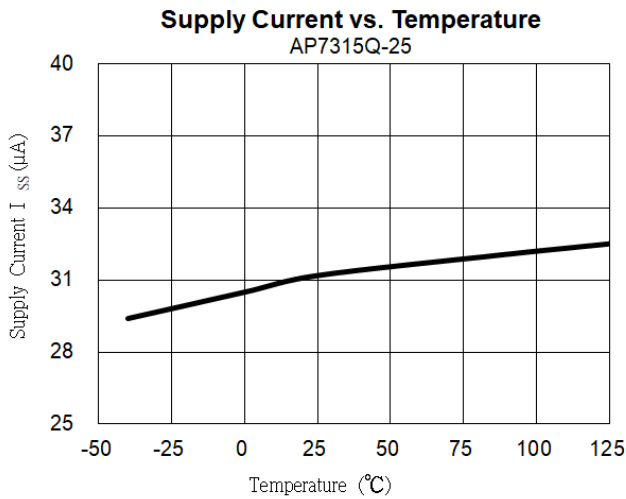
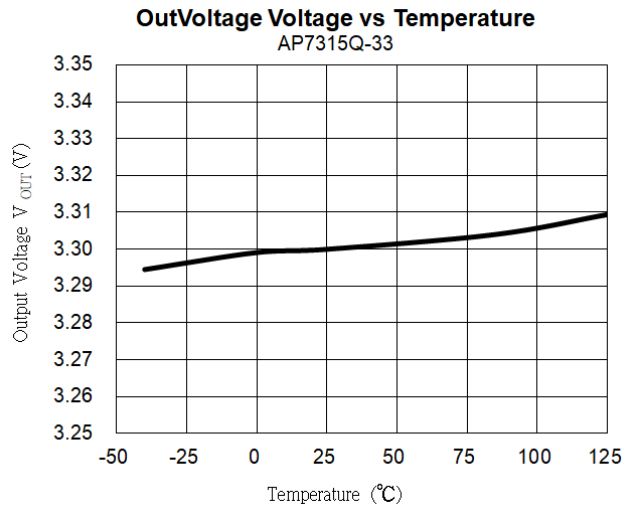
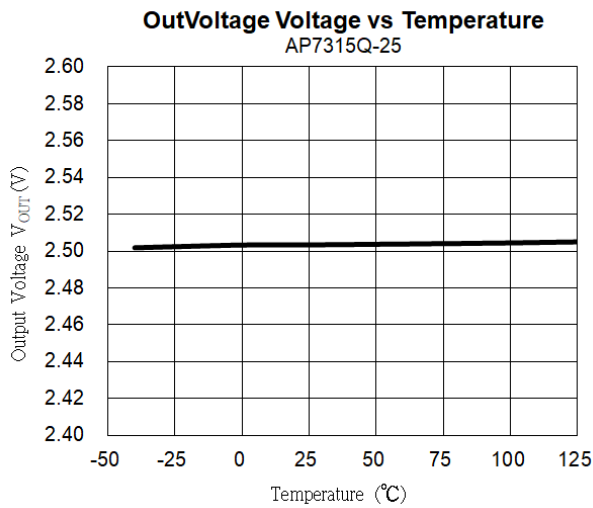
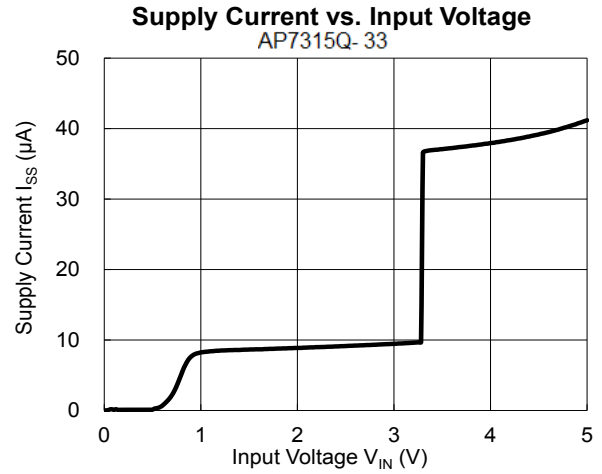
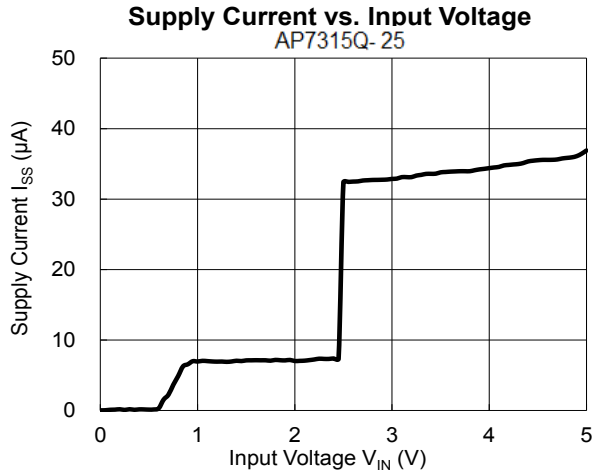
**Output Voltage vs. Input Voltage**  
AP7315Q-25



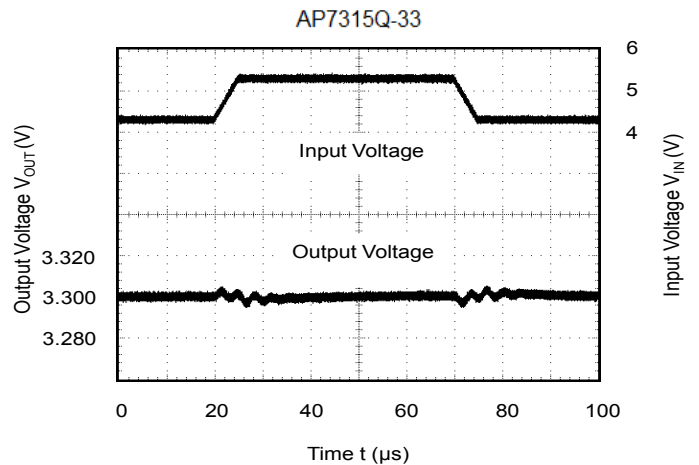
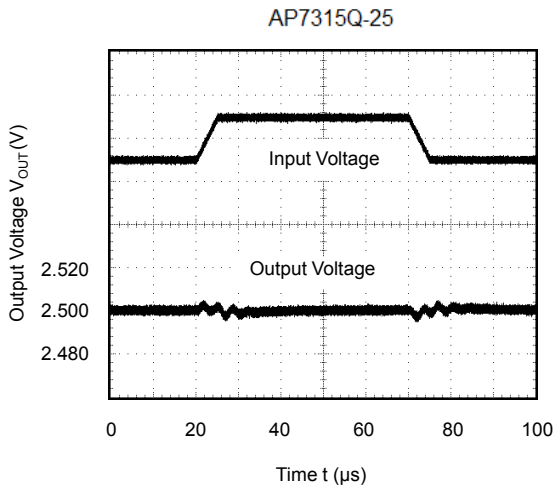
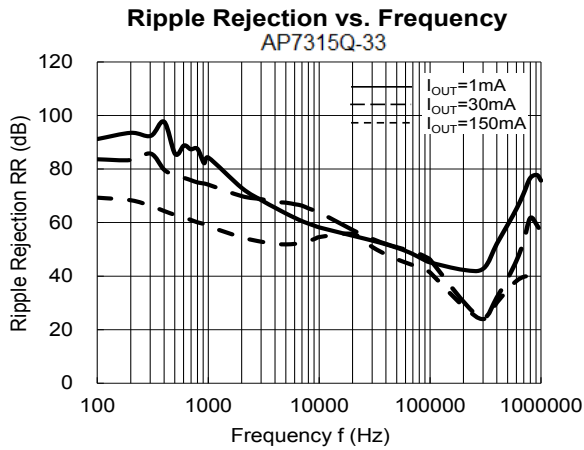
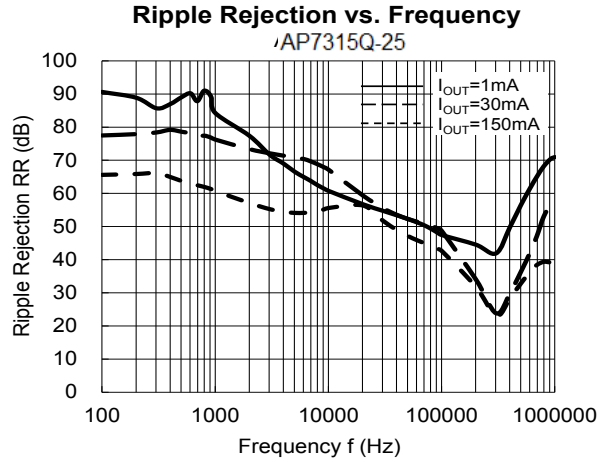
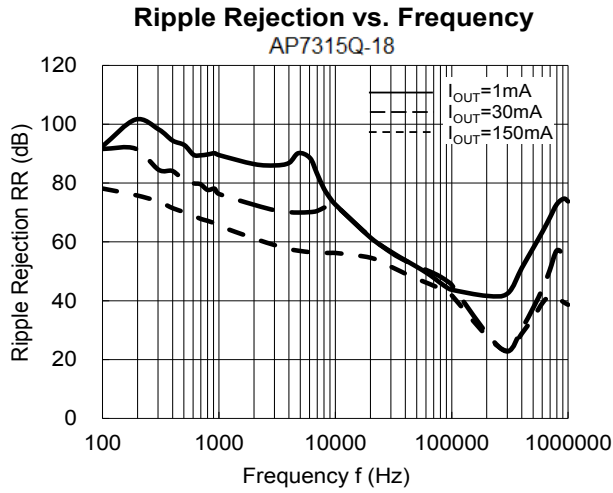
**Output Voltage vs. Input Voltage**  
AP7315Q-33



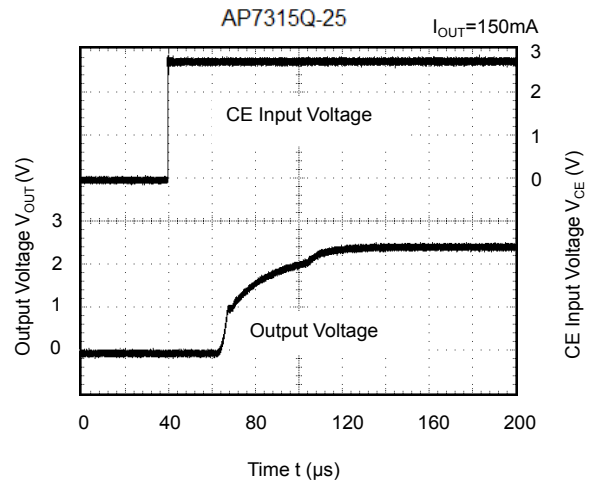
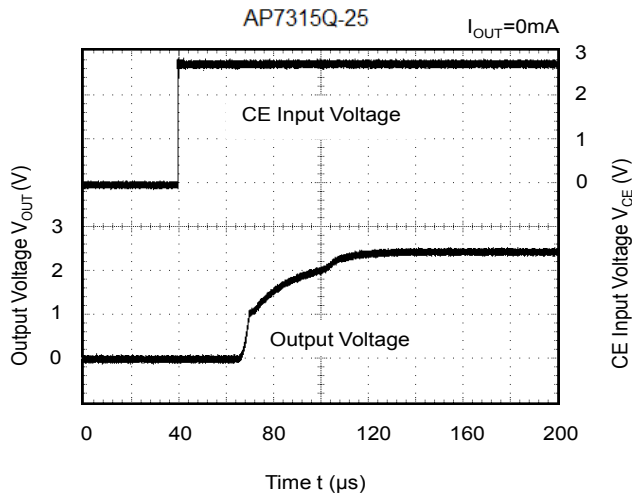
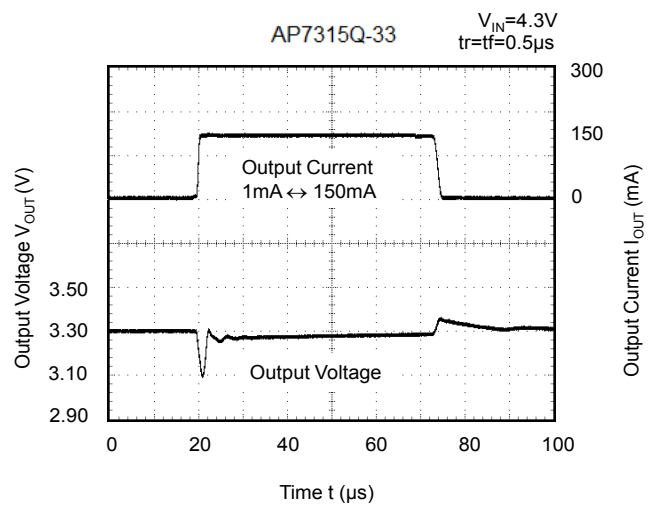
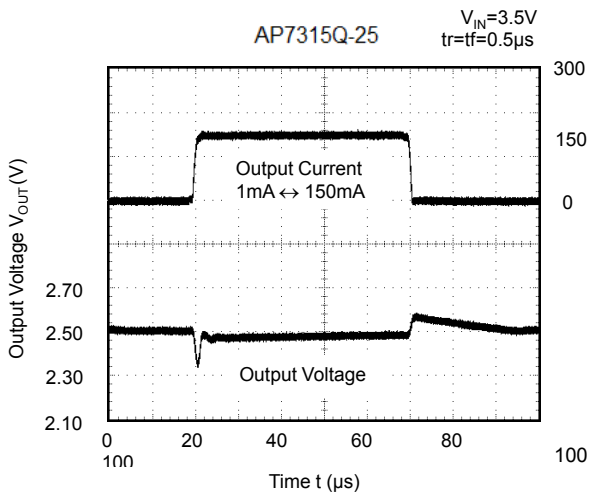
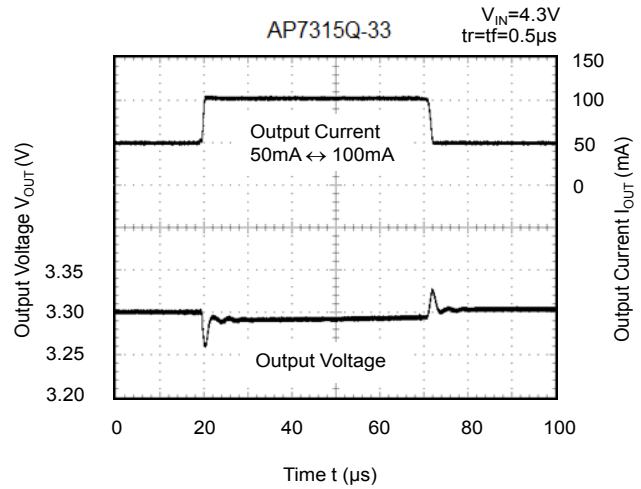
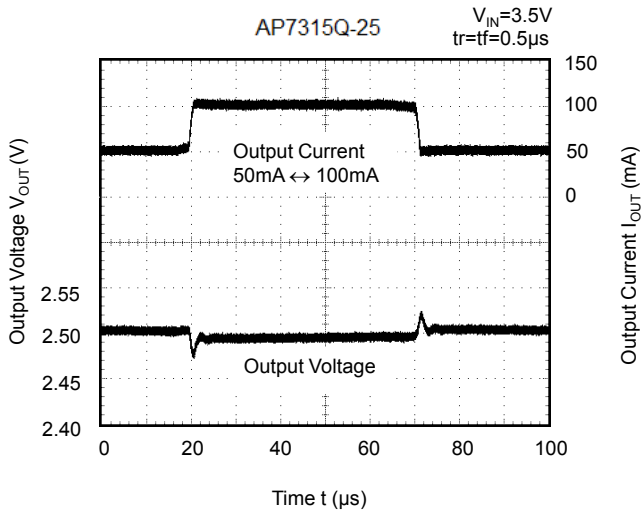
**Typical Characteristics** (continued)



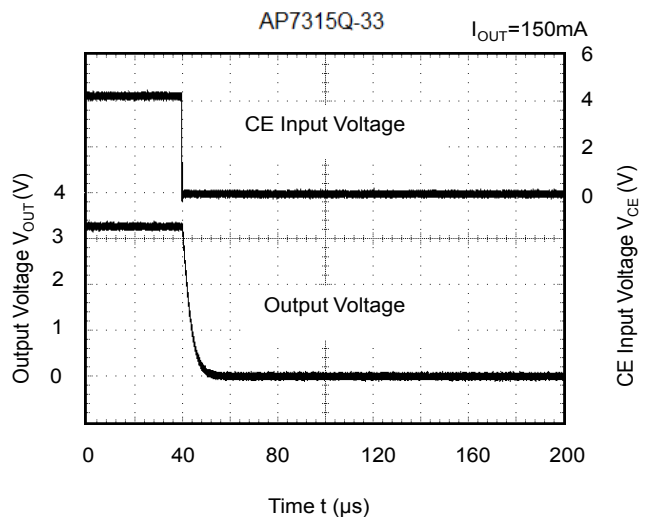
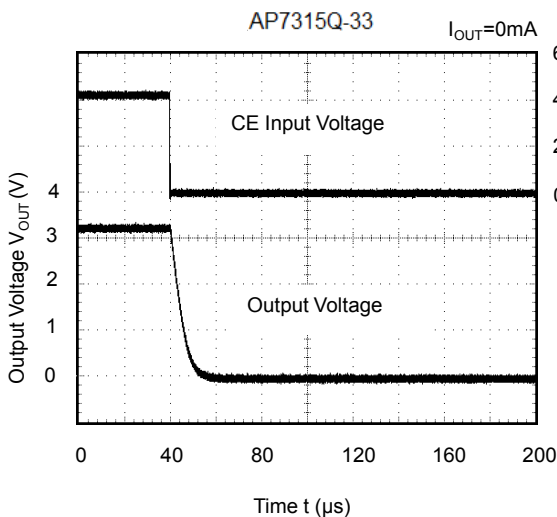
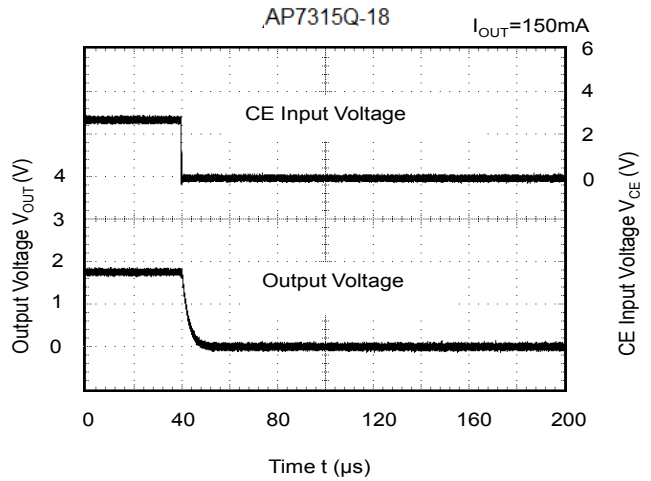
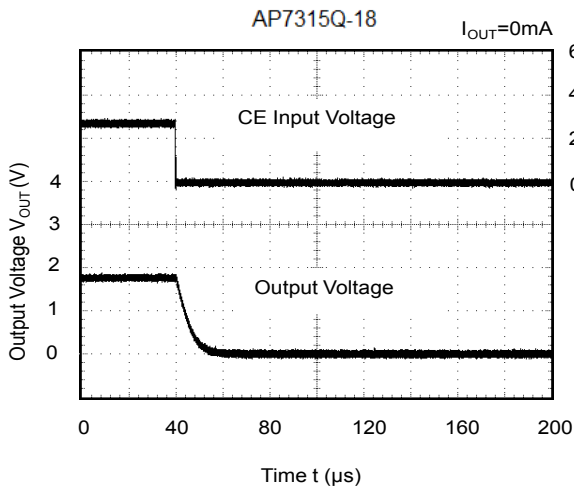
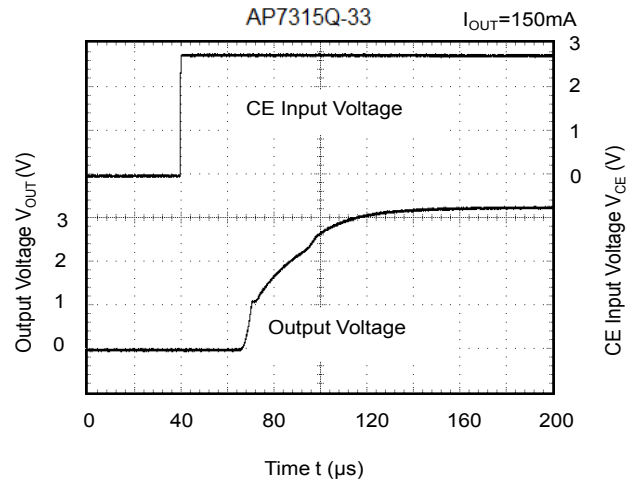
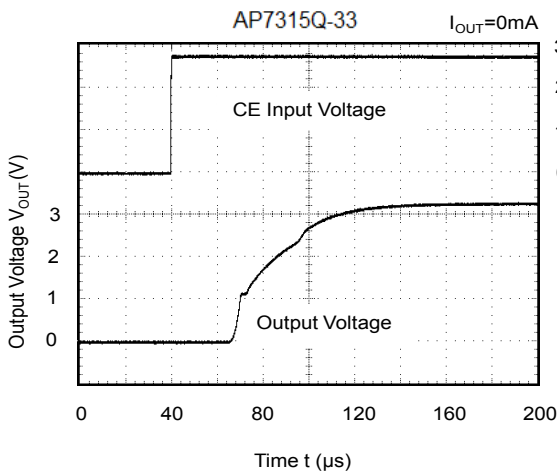
**Typical Characteristics (cont.)**



**Typical Characteristics (cont.)**



**Typical Characteristics** (cont.)





**Application Information**

**Output Capacitor**

An output capacitor ( $C_{OUT}$ ) is required to improve transient response and maintain stability. The AP7315Q is stable with very small ceramic output capacitors. The ESR (equivalent series resistance) and capacitance drives the selection. If the application has large load variations, it is recommended to utilize low-ESR bulk capacitors. It is recommended to place ceramic capacitors as close as possible to the load and the ground pin. Care should be taken to reduce the impedance in the layout.

**Input Capacitor**

To prevent the input voltage from dropping during load steps, it is recommended to utilize an input capacitor ( $C_{IN}$ ). A minimum  $0.47\mu F$  ceramic capacitor is recommended between  $V_{IN}$  and GND pins to decouple input power supply glitch. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both  $V_{IN}$  and GND pins.

**Enable Control**

The AP7315Q is turned on by setting the EN pin high and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to the  $V_{IN}$  pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section.

**Short Circuit Protection**

When  $V_{OUT}$  pin is short-circuit-to-GND, short-circuit protection is triggered and clamp the output current to approximately 60mA. This feature protects the regulator from over-current and damage due to overheating.

**Layout Considerations**

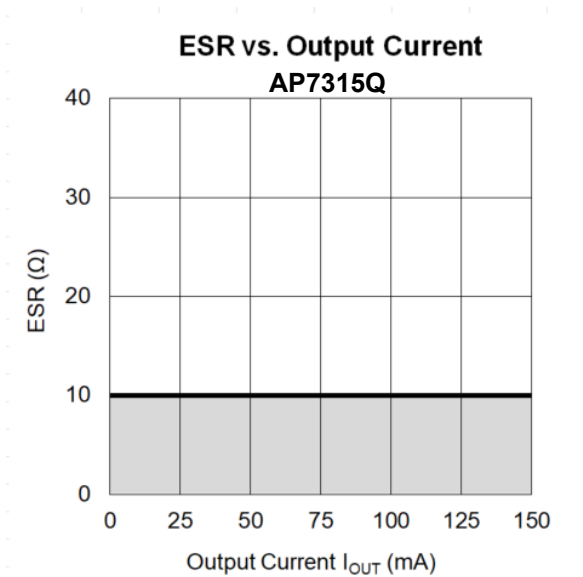
For good ground loop and stability, the input and output capacitors should be located close to the  $V_{IN}$ ,  $V_{OUT}$ , and GND pins of the device. The regulator GND pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance. Wide trace should be used for large current paths from  $V_{IN}$  to  $V_{OUT}$ , and load circuit.

**ESR vs. Output Current**

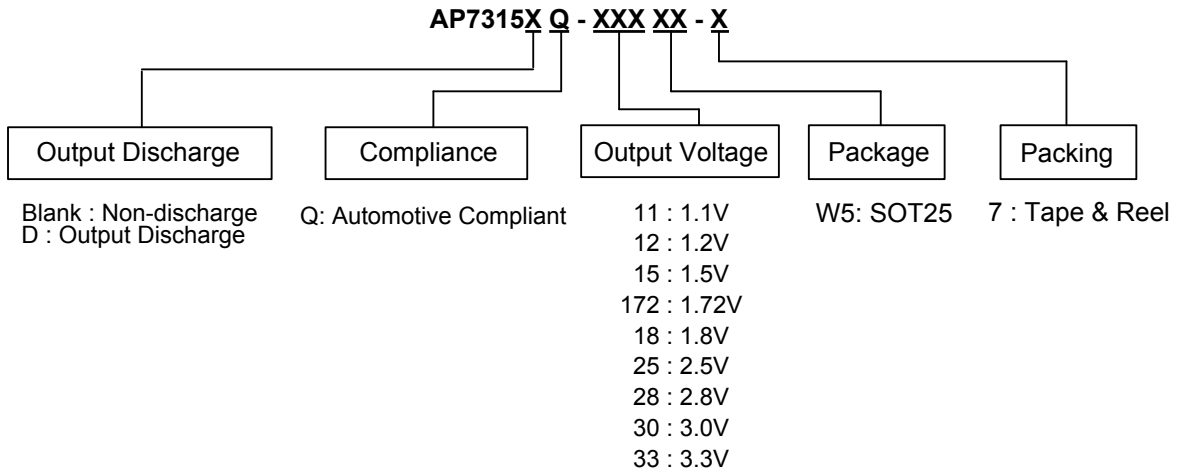
A ceramic type output capacitor is recommended for this series; however, other output capacitors with low ESR may also be used. The relations between  $I_{OUT}$  (Output Current) and ESR of an output capacitor are shown below. The stable region is marked as the hatched area in the graph.

Measurement Conditions:

Frequency Band: 10Hz to 2MHz, Temperature:  $-40^{\circ}C$  to  $+125^{\circ}C$



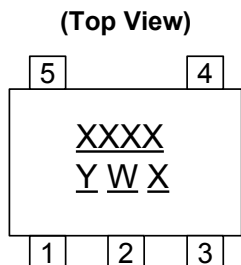
**Ordering Information**



Part Number (Note 15)	Compliance (Note 16)	Package Code	Packaging (Note 14)	7" Tape and Reel	
				Quantity	Part Number Suffix
AP7315Q-XXXW5-7	Automotive Compliant	W5	SOT25	3000/Tape & Reel	-7
AP7315DQ-XXXW5-7	Automotive Compliant	W5	SOT25	3000/Tape & Reel	-7

Note: 14. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.  
 15. Other output voltage variants may be available in 100mV steps. For more information, please contact your local Diodes Sales representative.  
 16. AP7315Q and AP7315DQ are qualified to AEC-Q100 grade 1 and are classified as Automotive Compliant supporting PPAP documentation. Automotive Compliant and standard products are electrically and thermally the same, except where specified.  
 For more information, please refer to [http://www.diodes.com/quality/product\\_compliance\\_definitions/](http://www.diodes.com/quality/product_compliance_definitions/).  
 See AP7315 datasheet for commercial qualified versions.

**Marking Information**



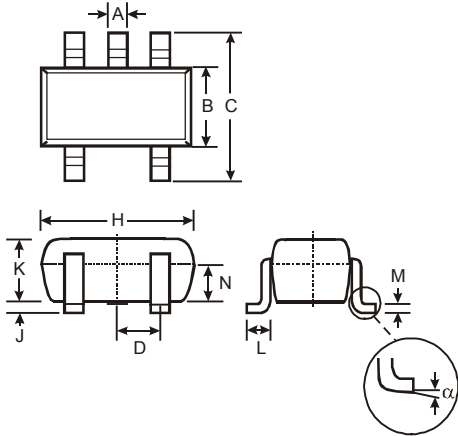
**XXXX** : Identification Code  
**Y** : Year 0 to 9  
**W** : Week : A to Z : 1 to 26 week;  
 a to z : 27 to 52 week; z represents  
 52 and 53 week  
**X** : Internal Code

Part Number	Package	Identification Code
AP7315Q-11W5-7	SOT25	15AQ
AP7315Q-12W5-7	SOT25	15BQ
AP7315Q-15W5-7	SOT25	15DQ
AP7315Q-172W5-7	SOT25	15XQ
AP7315Q-18W5-7	SOT25	15EQ
AP7315Q-25W5-7	SOT25	15JQ
AP7315Q-28W5-7	SOT25	15MQ
AP7315Q-30W5-7	SOT25	15RQ
AP7315Q-33W5-7	SOT25	15UQ
AP7315DQ-11W5-7	SOT25	5DAQ
AP7315DQ-12W5-7	SOT25	5DBQ
AP7315DQ-15W5-7	SOT25	5DDQ
AP7315DQ-172W5-7	SOT25	5DYQ
AP7315DQ-18W5-7	SOT25	5DEQ
AP7315DQ-25W5-7	SOT25	5DJQ
AP7315DQ-28W5-7	SOT25	5DMQ
AP7315DQ-30W5-7	SOT25	5DSQ
AP7315DQ-33W5-7	SOT25	5DVQ

**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SOT25**

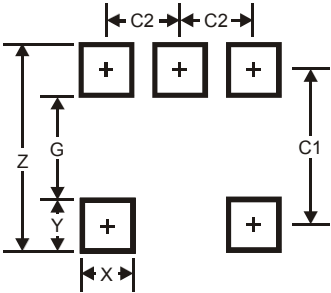


SOT25			
Dim	Min	Max	Typ
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	-	-	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
N	0.70	0.80	0.75
α	0°	8°	-
<b>All Dimensions in mm</b>			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**SOT25**



Dimensions	Value
Z	3.20
G	1.60
X	0.55
Y	0.80
C1	2.40
C2	0.95

**IMPORTANT NOTICE**

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