

## Description

The DIODES™ AP7343Q is a low dropout regulator with high output voltage accuracy, low  $R_{DS(ON)}$ , high PSRR, low output noise and low quiescent current. This regulator is based on a CMOS process.

The AP7343Q includes a voltage reference, error amplifier, current limit circuit, and an enable input to turn it on and off. With the integrated resistor network, fixed output voltage versions can be delivered.

With its low power consumption and line and load transient responses, the AP7343Q is well suited for noise sensitive automotive applications.

The AP7343Q is packaged in SOT25 and W-DFN2020-6 (SWP) (Type A1) packages, which allow for the smallest footprint and dense PCB layout.

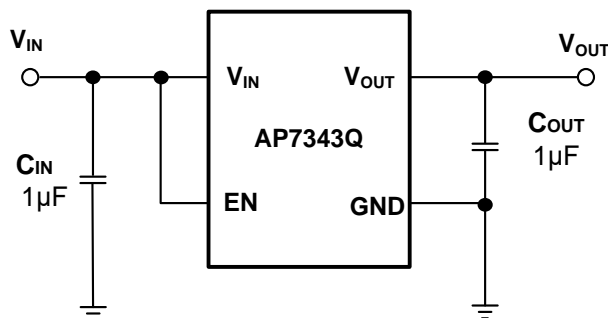
## Features

- Low  $V_{IN}$  and Wide  $V_{IN}$  Range: 1.7V to 5.25V
- -40°C to +125°C Temperature Range
- Guaranteed Output Current: 300mA
- $V_{OUT}$  Accuracy  $\pm 1\%$
- Ripple Rejection 75dB at 1kHz
- Low Output Noise, 60 $\mu$ Vrms from 10Hz to 100kHz
- Quiescent Current as Low as 35 $\mu$ A
- $V_{OUT}$  Fixed 0.9V to 3.6V
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP7343Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**

<https://www.diodes.com/quality/product-definitions/>

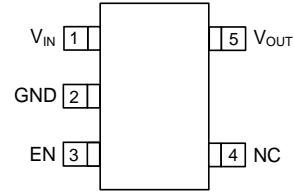
- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Typical Applications Circuit



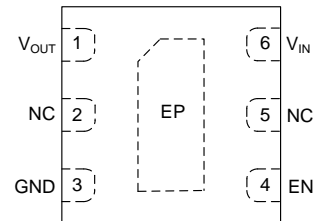
## Pin Assignments

(Top View)



SOT25

(Top View)



W-DFN2020-6 (SWP) (Type A1)

Future Product

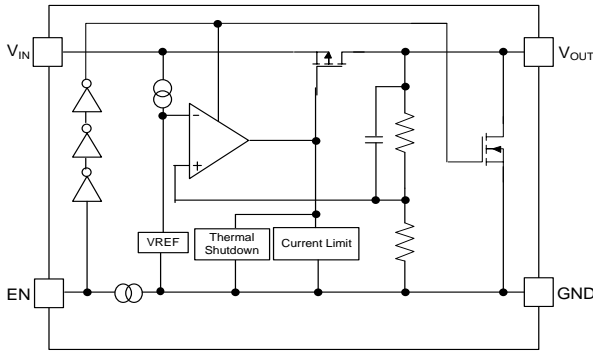
## Applications

- Infotainment power supplies
- Automotive RF supplies
- Cameras
- Automotive POL in ADAS
- Automotive wireless communications

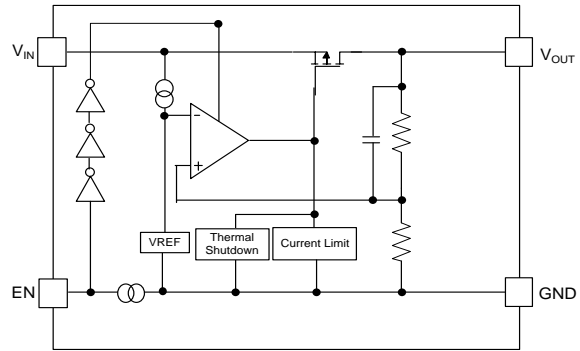
### Pin Descriptions

Pin Number		Pin Name	Function
SOT25	W-DFN2020-6 (SWP) (Type A1)		
1	6	V <sub>IN</sub>	Power Input Pin
2	3	GND	Ground
3	4	EN	Enable Pin This pin must be driven either high or low and must not be floating. Driving this pin high enables the regulator, and pulling it low puts the regulator into shutdown mode.
4	2, 5	NC	No Connect Not connected internally; recommended to connect to GND to maximize PCB copper for thermal dissipation.
5	1	V <sub>OUT</sub>	Power Output Pin
—	EP	Expose Pad	In PCB layout, prefer to use large copper area to cover this pad for better thermal dissipation, then connect this area to GND or leave it open. However, do not use it as GND electrode function alone

### Functional Block Diagram



DIODES™ AP7343DQ (With Discharge)



AP7343Q (Without Discharge)

### Absolute Maximum Ratings (Note 4) (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body Mode ESD Protection	> 2	kV
ESD CDM	Charge Device Model	±500	V
V <sub>IN</sub>	Input Voltage	6.0	V
V <sub>EN</sub>	Input Voltage for EN Pin	6.0	V
V <sub>OUT</sub>	Output Voltage	-0.3 to V <sub>IN</sub> + 0.3	V
I <sub>OUT</sub>	Output Current	400	mA
P <sub>D</sub>	Power Dissipation	SOT25	400
		W-DFN2020-6 (SWP) (Type A1) (Wettable)	TBD
T <sub>J</sub>	Operating Junction Temperature	-40 to +150	°C
T <sub>STG</sub>	Storage Temperature	-55 to +150	°C

Note: 4. a). Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.  
b). Ratings apply to ambient temperature at +25°C. The JEDEC High-K board design used to derive this data was a 2inch x 2inch multilayer board with 1oz internal power and ground planes and 2oz copper traces on the top and bottom of the board.

**Recommended Operating Conditions** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

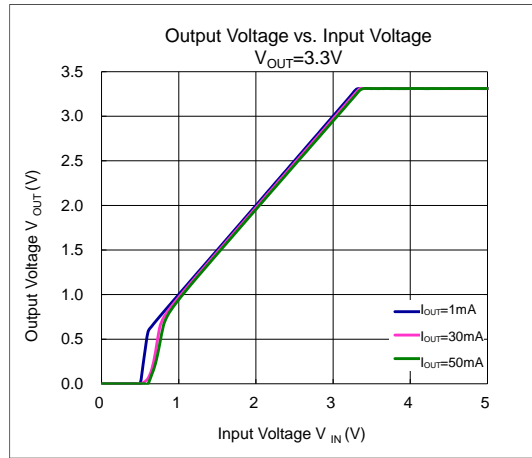
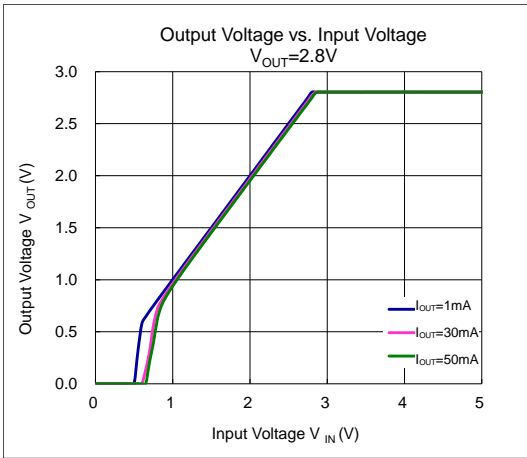
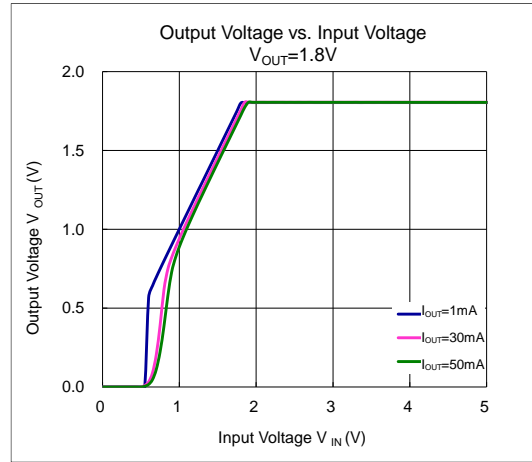
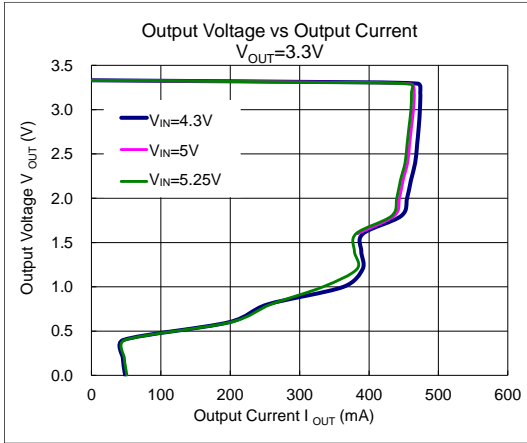
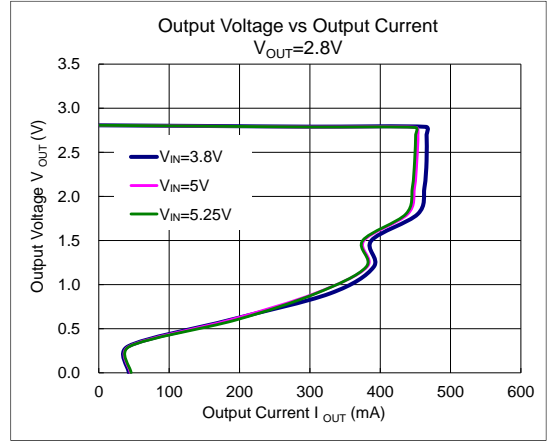
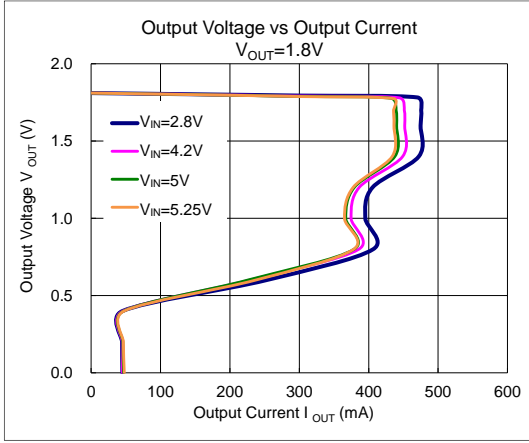
Symbol	Parameter	Min	Max	Unit
$V_{IN}$	Input Voltage	1.7	5.25	V
$I_{OUT}$	Output Current	0	300	mA
$T_J$	Operating Junction Temperature	-40	+125	$^\circ\text{C}$
$T_A$	Operating Ambient Temperature	-40	+125	$^\circ\text{C}$

**Electrical Characteristics** (@ $T_A = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT} + 1.0\text{V}$ ,  $C_{IN} = C_{OUT} = 1.0\mu\text{F}$ ,  $I_{OUT} = 1.0\text{mA}$ , unless otherwise specified.)

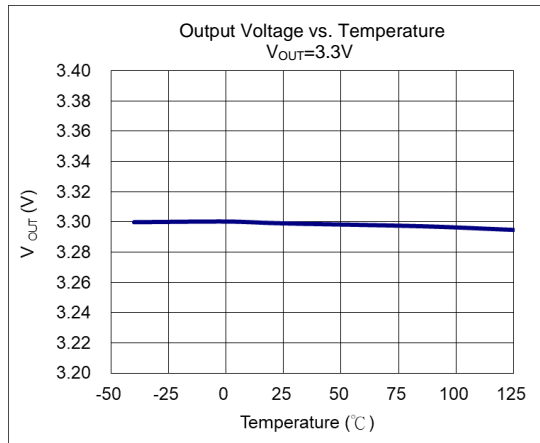
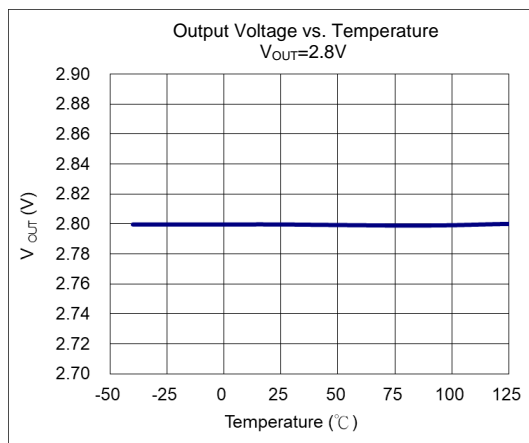
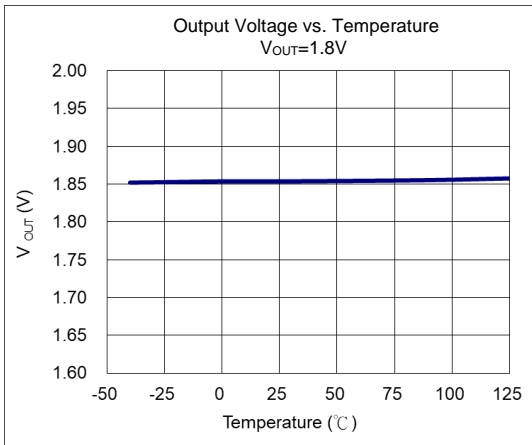
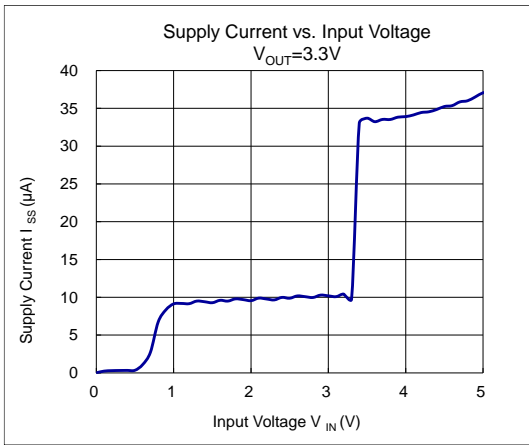
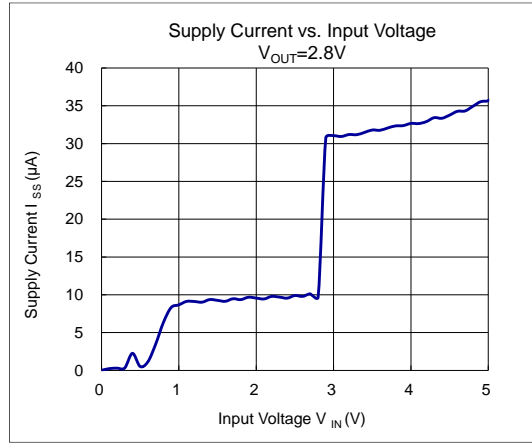
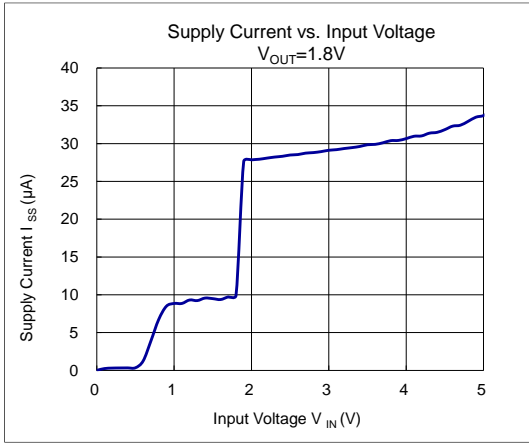
Parameter	Condition	Min	Typ	Max	Unit	
Input Voltage	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.7	—	5.25	V	
Output Voltage Accuracy (Note 5)	$V_{OUT}(T) \geq 2.0\text{V}$ , $V_{IN} = V_{OUT}(T) + 1\text{V}$   $T_A = +25^\circ\text{C}$	$V_{OUT}(T) \times 0.99$	$V_{OUT}(T)$	$V_{OUT}(T) \times 1.01$	V	
	$V_{OUT}(T) < 2.0\text{V}$ , $V_{IN} = V_{OUT}(T) + 1\text{V}$   $T_A = +25^\circ\text{C}$	$V_{OUT}(T) - 20\text{mV}$	$V_{OUT}(T)$	$V_{OUT}(T) + 20\text{mV}$		
Line Regulation ( $dV_{OUT}/dV_{IN}/V_{OUT}$ )	$V_{IN} = (V_{OUT-Nom} + 1.0\text{V})$ to $5.25\text{V}$ , $I_{OUT} = 1.0\text{mA}$	—	0.02	0.1	%/V	
Load Regulation	$V_{IN} = V_{OUT-Nom} + 1.0\text{V}$ , $I_{OUT} = 1\text{mA}$ to $300\text{mA}$	—	15	30	mV	
Quiescent Current (Note 6)	$I_{OUT} = 0\text{mA}$	—	35	60	$\mu\text{A}$	
$I_{STANDBY}$	$V_{EN} = 0\text{V}$ (Disabled)	—	0.01	1.0	$\mu\text{A}$	
Output Current	—	300	—	—	mA	
Fold-back Short Current (Note 7)	$V_{OUT}$ Short to Ground	—	55	—	mA	
PSRR (Note 8)	$V_{IN} = (V_{OUT} + 1\text{V}) V_{DC} + 0.2\text{Vp-pAC}$ $V_{OUT} \geq 1.8\text{V}$ , $I_{OUT} = 30\text{mA}$   $f = 1\text{kHz}$	—	75	—	dB	
Output Noise Voltage (Notes 8 & 9)	$BW = 10\text{Hz}$ to $100\text{kHz}$ , $I_{OUT} = 30\text{mA}$	—	60	—	$\mu\text{Vrms}$	
Dropout Voltage (Note 10)	$I_{OUT} = 300\text{mA}$ (SOT25)	$V_{OUT} = 0.9\text{V}$	—	0.51	0.82	V
		$1.0\text{V} < V_{OUT} \leq 1.2\text{V}$	—	0.46	0.72	
		$1.2\text{V} < V_{OUT} \leq 1.4\text{V}$	—	0.39	0.60	
		$1.4\text{V} < V_{OUT} \leq 1.7\text{V}$	—	0.35	0.46	
		$1.7\text{V} < V_{OUT} \leq 2.1\text{V}$	—	0.30	0.41	
		$2.1\text{V} < V_{OUT} \leq 2.5\text{V}$	—	0.26	0.36	
		$2.5\text{V} < V_{OUT} \leq 3.0\text{V}$	—	0.25	0.32	
Output Voltage Temperature Coefficient	$I_{OUT} = 30\text{mA}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	—	$\pm 30$	—	ppm/ $^\circ\text{C}$	
Thermal Shutdown Threshold (TSHDN)	—	—	+150	—	$^\circ\text{C}$	
Thermal Shutdown Hysteresis (THYS)	—	—	+20	—	$^\circ\text{C}$	
EN Input Low Voltage	—	0	—	0.5	V	
EN Input High Voltage	—	1.3	—	5.25	V	
EN Input Leakage	$V_{EN} = 0\text{V}$ , $V_{IN} = 5.0\text{V}$ or $V_{EN} = 5.0\text{V}$ , $V_{IN} = 0\text{V}$	-1.0	—	+1.0	$\mu\text{A}$	
On Resistance of N-Channel for Auto-Discharge (Note 11)	$V_{IN} = 4.0\text{V}$ , $V_{EN} = 0\text{V}$ (Disabled)	—	30	—	$\Omega$	
Thermal Resistance Junction to Ambient ( $\theta_{JA}$ )	SOT25	—	179	—	$^\circ\text{C/W}$	
	W-DFN2020-6 (SWP) (Type A1) (Wettable)	—	TBD	—		
Thermal Resistance Junction to Case ( $\theta_{JC}$ )	SOT25	—	52	—	$^\circ\text{C/W}$	
	W-DFN2020-6 (SWP) (Type A1) (Wettable)	—	TBD	—		

- Notes:
- Potential multiple grades based on following output voltage accuracy.
  - Quiescent current defined here is the difference in current between the input and the output.
  - Short circuit current is measured with  $V_{OUT}$  pulled to GND.
  - This specification is guaranteed by design.
  - To make sure lowest environment noise minimizes the influence on noise measurement.
  - Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.
  - AP7343Q has two options for output, built-in discharge and non-discharge.

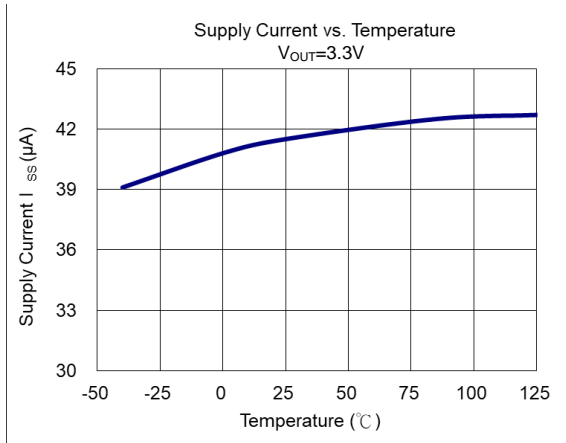
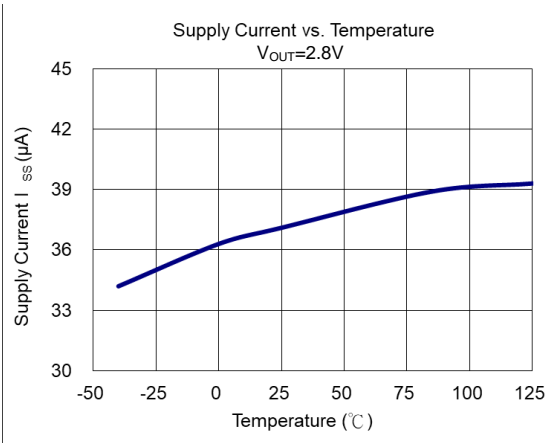
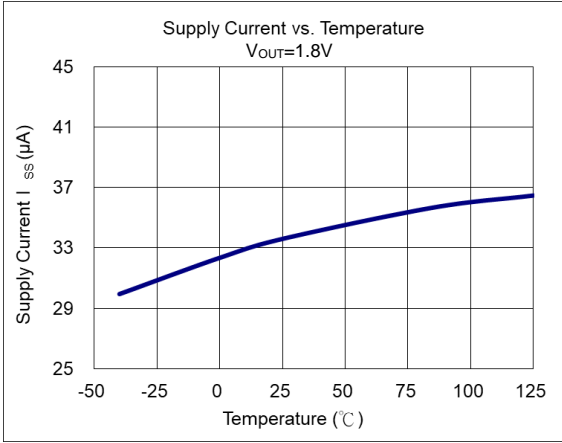
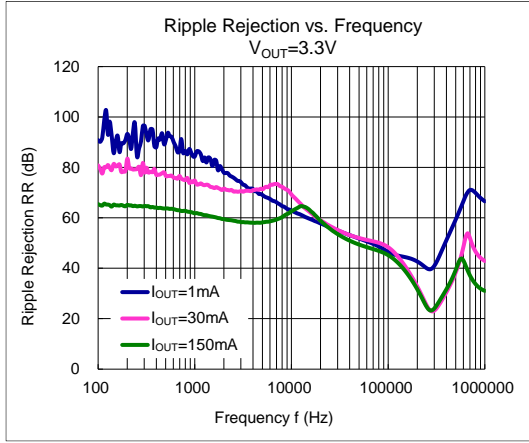
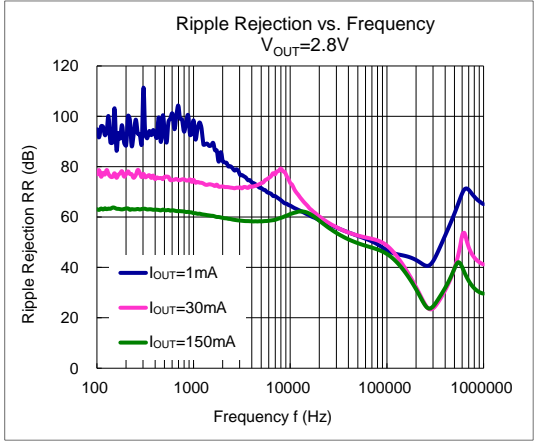
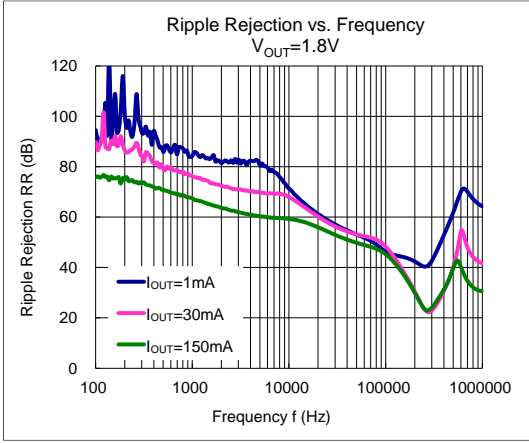
**Typical Characteristics**



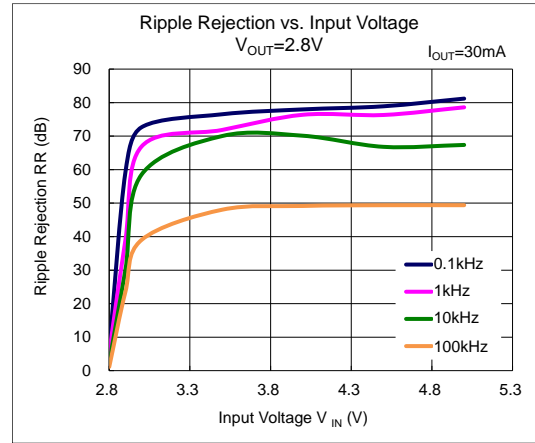
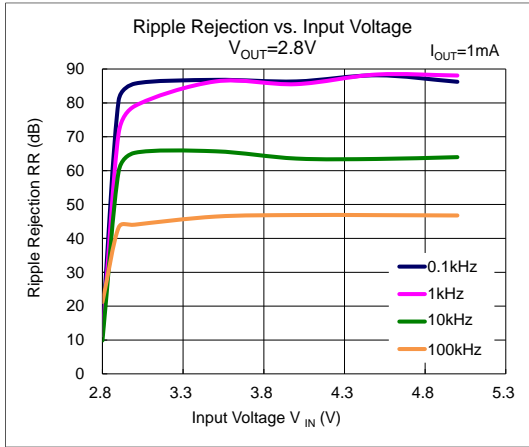
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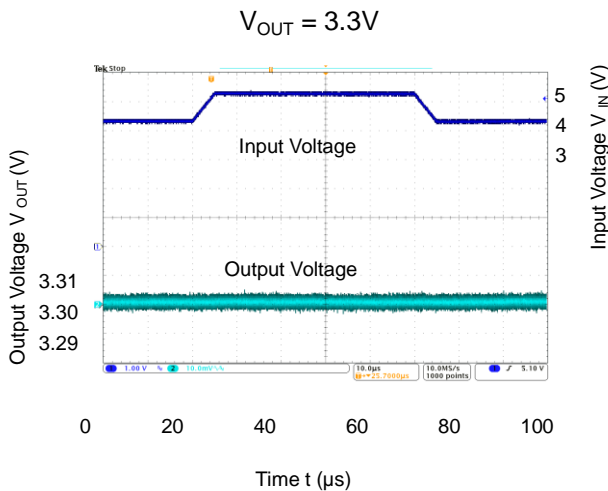
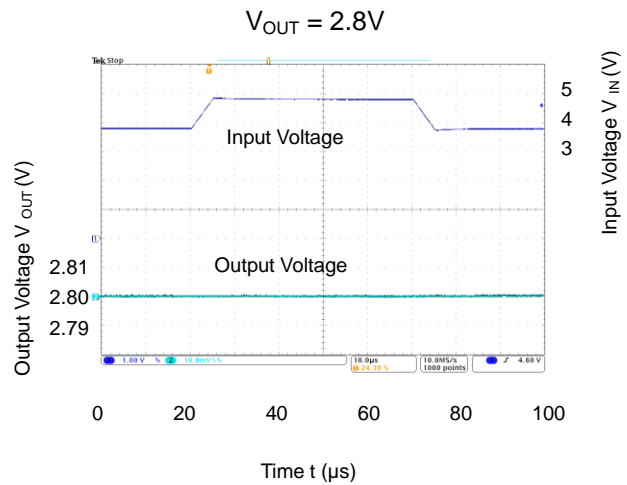
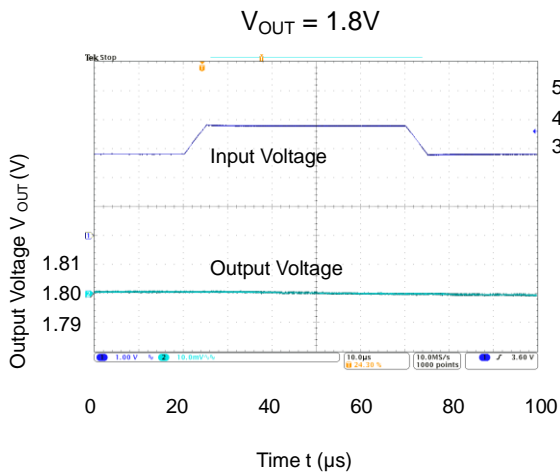
**Typical Characteristics** (continued)



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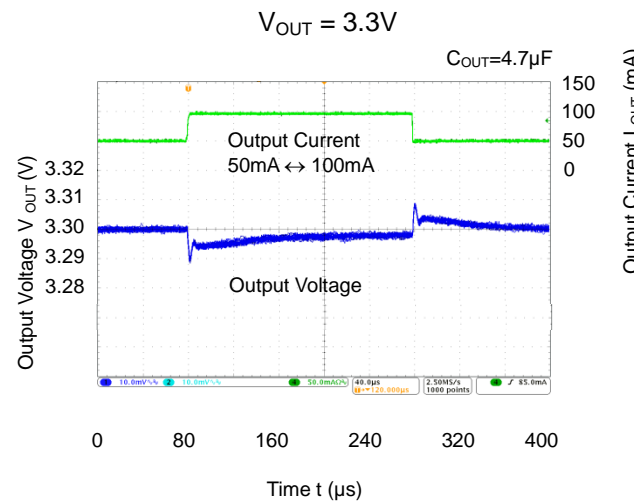
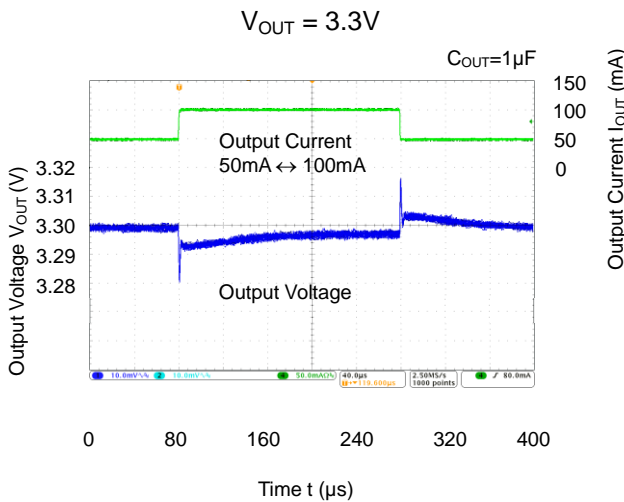
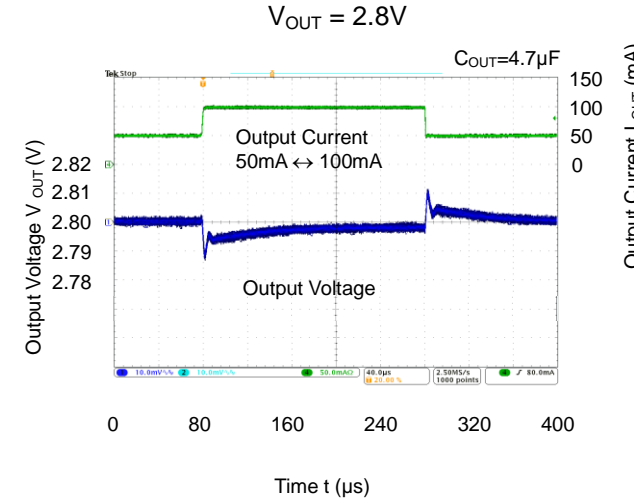
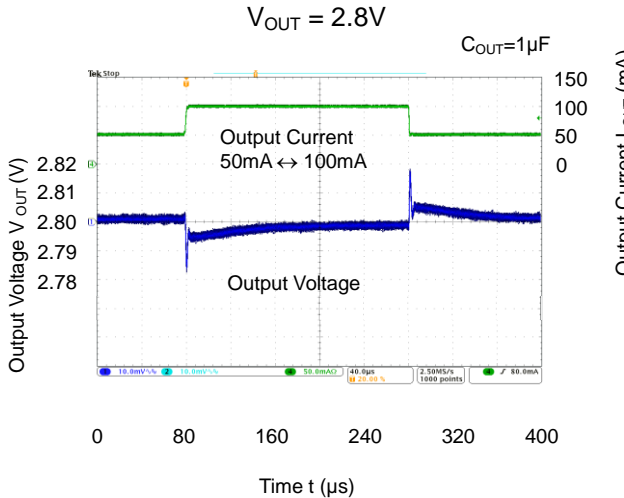
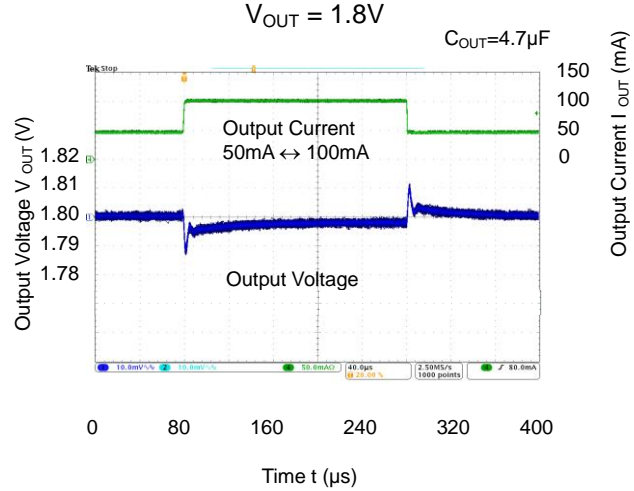
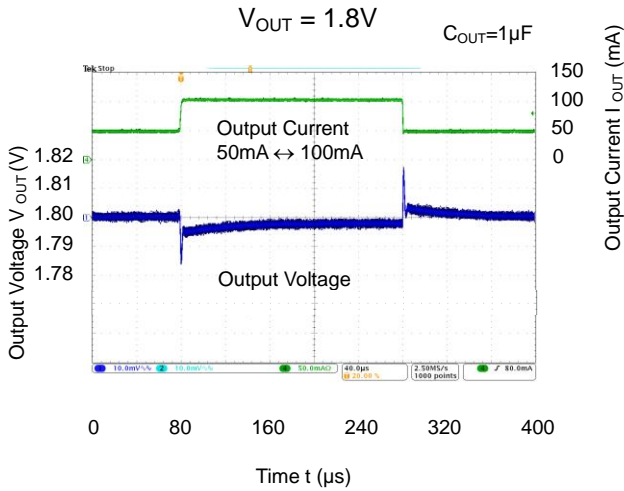


Line Transient Response Waveforms ( $I_{OUT} = 30mA$ ,  $t_R = t_F = 5\mu s$ ,  $C_{IN} = None$ ,  $C_{OUT1} = C_{OUT2} = 1\mu F$ ,  $T_A = +25^\circ C$ )



**Typical Characteristics** (continued)

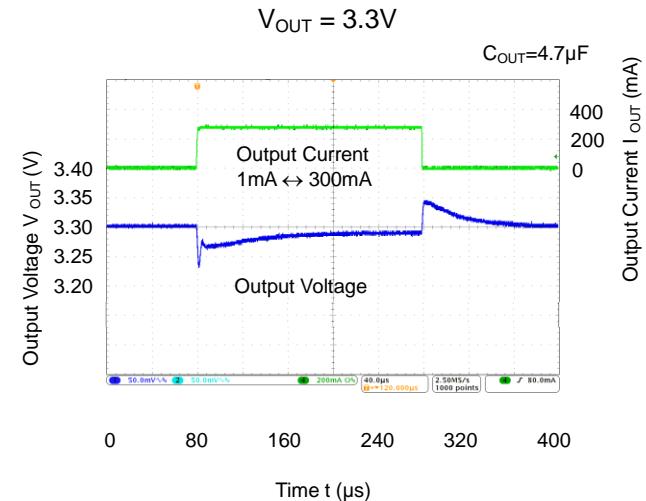
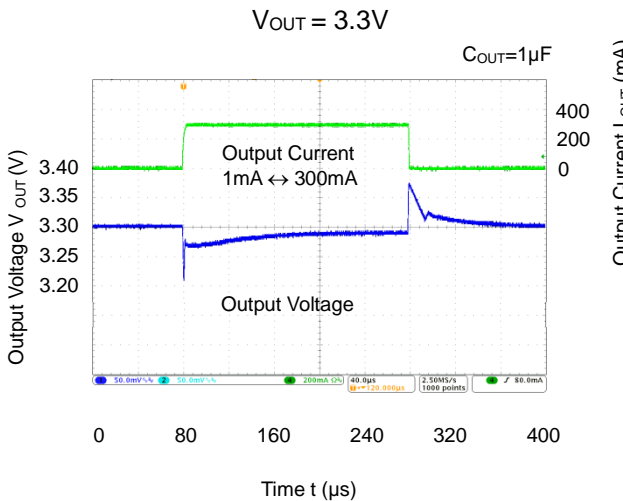
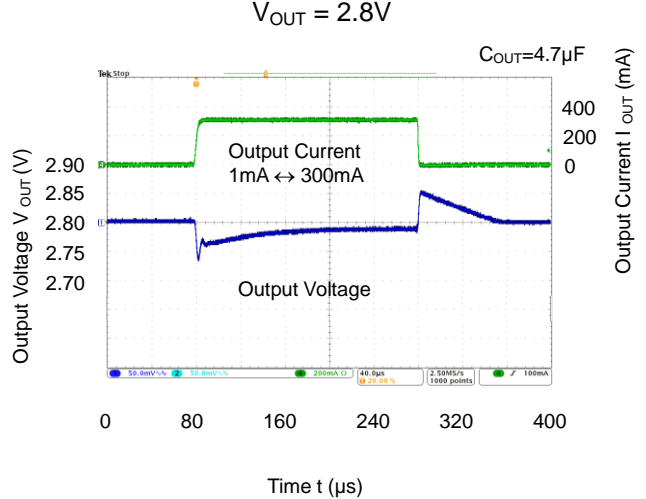
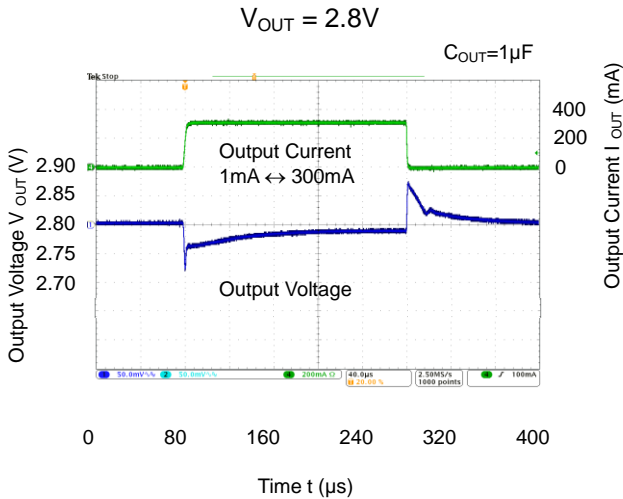
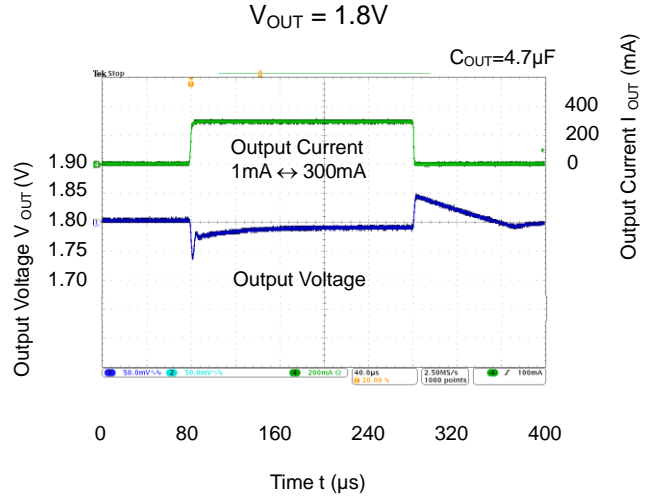
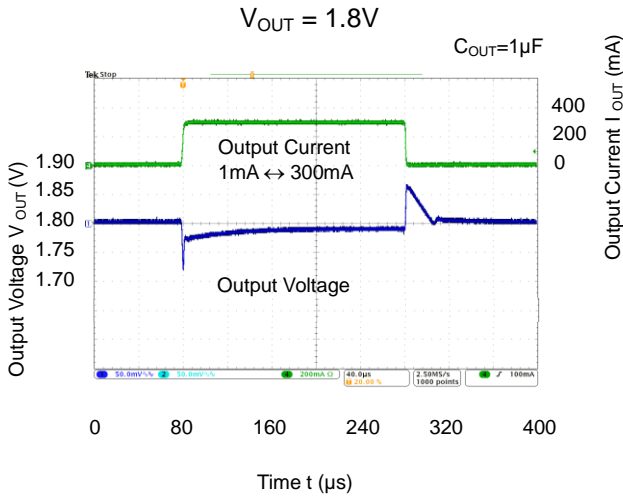
Load Transient Response Waveforms ( $V_{IN} = V_{OUT} + 1V$ ,  $C_{IN} = 1\mu F$ ,  $T_A = +25^\circ C$ )





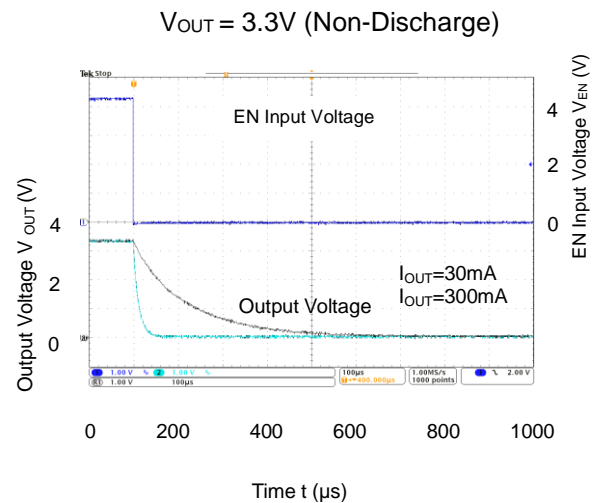
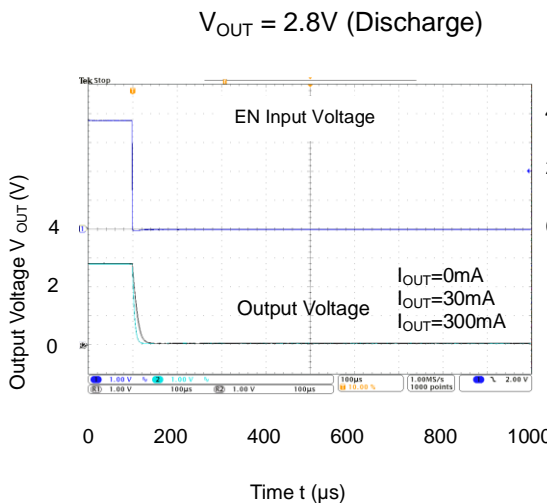
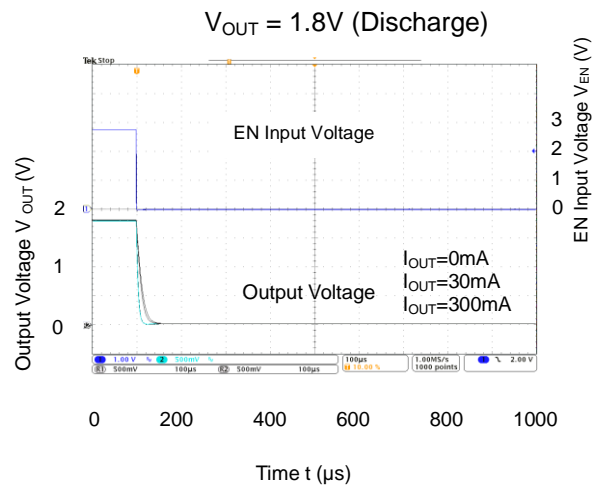
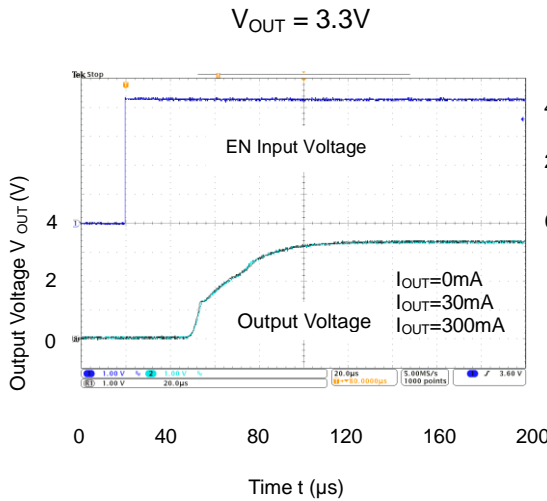
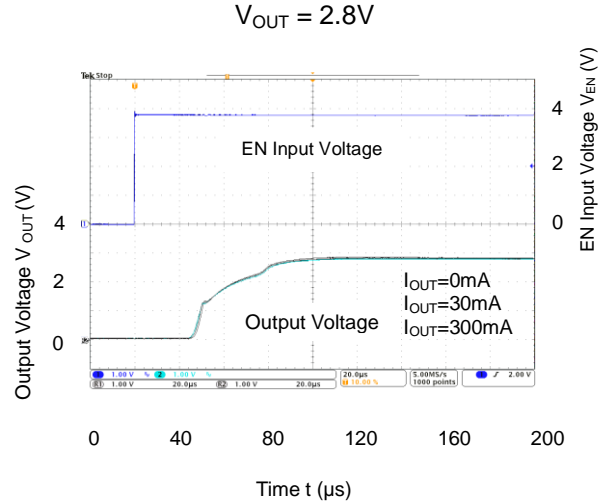
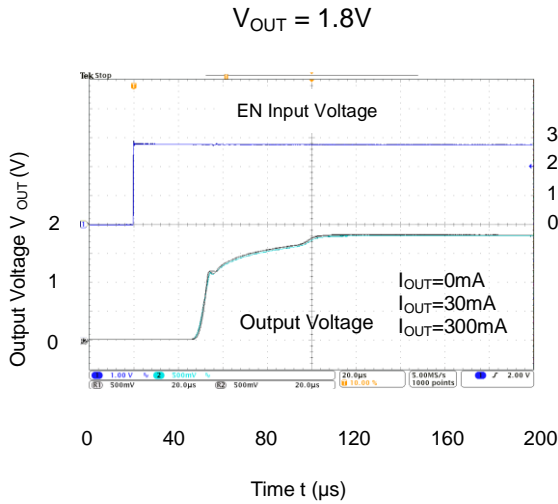
**Typical Characteristics** (continued)

Load Transient Response Waveforms ( $V_{IN} = V_{OUT} + 1V$ ,  $C_{IN} = 1\mu F$ ,  $T_A = +25^\circ C$ )



**Typical Characteristics** (continued)

Turn On & Off Waveforms ( $V_{IN} = V_{OUT} + 1V$ ,  $C_{IN} = 1\mu F$ ,  $C_{OUT} = 1\mu F$ ,  $T_A = +25^\circ C$ )



## Application Information

### Output Capacitor

An output capacitor ( $C_{OUT}$ ) is required to improve transient response and maintain stability. The AP7343Q is stable with very-small ceramic-output capacitors. The ESR (equivalent series resistance) and capacitance drive the selection. If the application has large load variations, it is recommended to utilize low-ESR bulk capacitors. It is recommended to place ceramic capacitors as close as possible to the load, and the ground pin and care should be taken to reduce the impedance in the layout.

### Input Capacitor

To prevent the input voltage from dropping during load steps, it is recommended to utilize an input capacitor ( $C_{IN}$ ). A minimum 0.47 $\mu$ F ceramic capacitor is recommended between  $V_{IN}$  and GND pins to decouple input power supply glitch. This input capacitor must be located as close as possible to the device to ensure input stability and reduce noise. For PCB layout, a wide copper trace is required for both  $V_{IN}$  and GND pins.

### Enable Control

The AP7343Q is turned on by setting the EN pin high and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to  $V_{IN}$  pin to keep the regulator output on at all times. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the *Electrical Characteristics* section.

### Short Circuit Protection

When  $V_{OUT}$  pin is short-circuited to GND, short-circuit protection is triggered and clamps the output current to approximately 60mA. This feature protects the regulator from overcurrent and damage due to overheating.

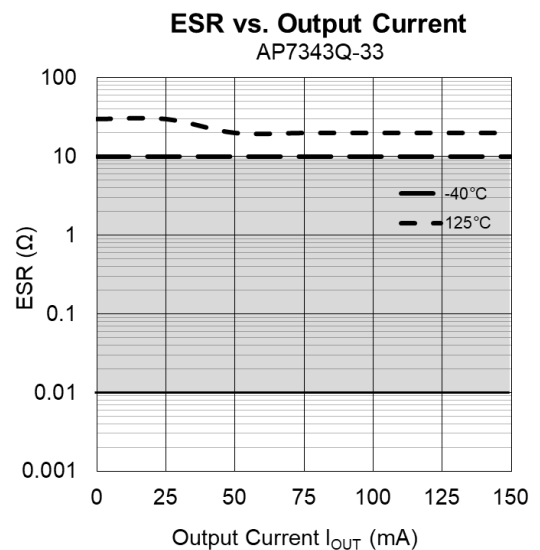
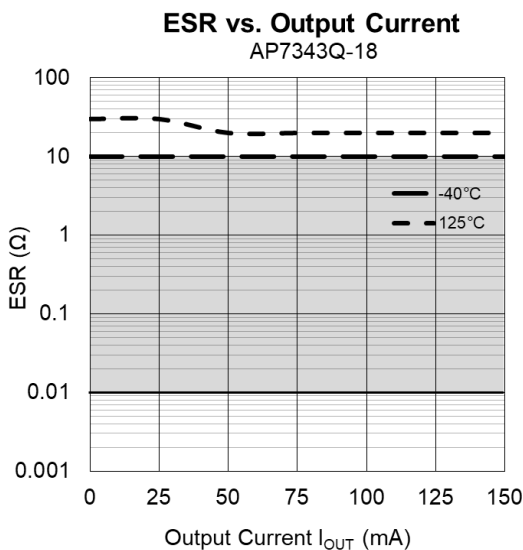
### Layout Considerations

For good ground loop and stability, the input and output capacitors should be located close to the input, output, and ground pins of the device. The regulator ground pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance. Wide trace should be used for large current paths from  $V_{IN}$  to  $V_{OUT}$  and load circuit.

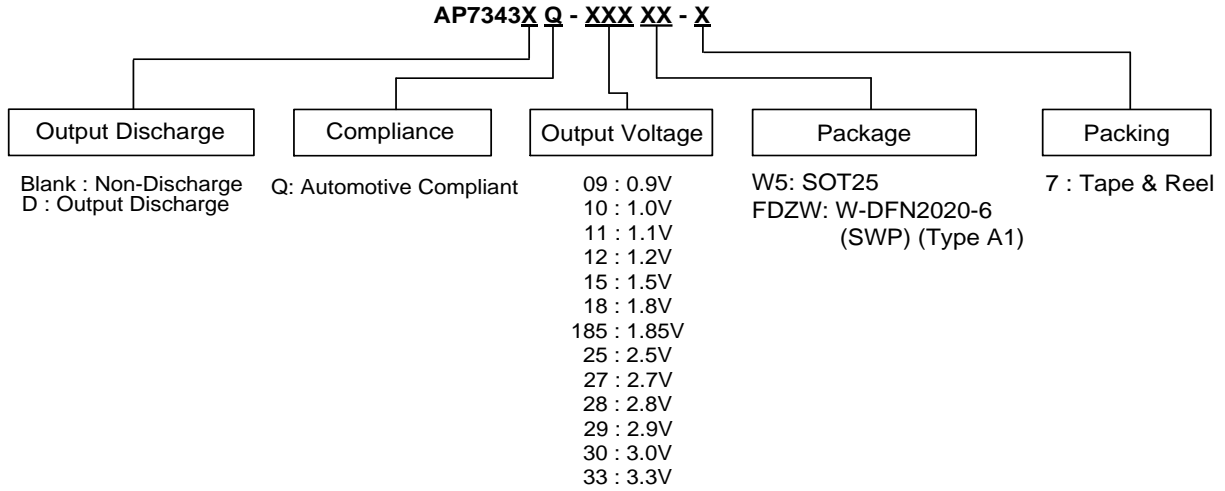
## ESR vs. Output Current

Ceramic type output capacitor is recommended for this series; however, the other output capacitors with low ESR also can be used. The relations between  $I_{OUT}$  (output current) and ESR of an output capacitor are shown below. The stable region is marked as the hatched area in the graph.

Measurement conditions: Frequency Band: 10Hz to 2MHz, Temperature: -40°C to +125°C.



**Ordering Information** (Notes 12, 13 & 14)



Part Number	Part Number Suffix	Package Code	Package	Packing	
				Qty.	Carrier
AP7343Q-XXXW5-7	-7	W5	SOT25	3000	7" Tape & Reel
AP7343DQ-XXXW5-7	-7	W5	SOT25	3000	7" Tape & Reel
AP7343Q-XXXFDZW-7(*)	-7	FDZW	W-DFN2020-6 (SWP) (Type A1)	3000	7" Tape & Reel
AP7343DQ-XXXFDZW-7(*)	-7	FDZW	W-DFN2020-6 (SWP) (Type A1)	3000	7" Tape & Reel

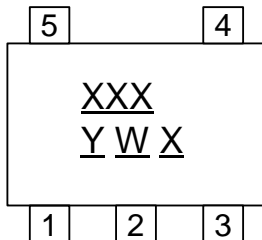
\* Future Product

- Notes:
- 12. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.
  - 13. Other output voltage variants may be available in 100mV steps. For more information, please contact your local Diodes Incorporated sales representative.
  - 14. AP7343Q and AP7343DQ are qualified to AEC-Q100 grade 1 and are classified as "Automotive Compliant" supporting PPAP documentation. Automotive compliant and standard products are electrically and thermally the same, except where specified. For more information, please refer to <https://www.diodes.com/quality/product-definitions/>.

## Marking Information

(1) SOT25

(Top View)



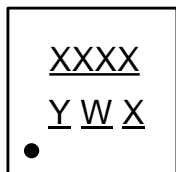
XXX : Identification Code  
Y : Year 0 to 9 (ex: 2 = 2022)  
W : Week : A to Z : Week 1 to 26;  
a to z : Week 27 to 52; z represents  
Week 52 and 53  
X : Internal Code

Part Number	Package	Identification Code
AP7343Q-09W5-7	SOT25	7BQ
AP7343Q-10W5-7	SOT25	7CQ
AP7343Q-11W5-7	SOT25	7EQ
AP7343Q-12W5-7	SOT25	7FQ
AP7343Q-15W5-7	SOT25	7HQ
AP7343Q-18W5-7	SOT25	7JQ
AP7343Q-185W5-7	SOT25	7KQ
AP7343Q-25W5-7	SOT25	7NQ
AP7343Q-27W5-7	SOT25	7XQ
AP7343Q-28W5-7	SOT25	7PQ
AP7343Q-29W5-7	SOT25	8AQ
AP7343Q-30W5-7	SOT25	7TQ
AP7343Q-33W5-7	SOT25	7WQ
AP7343DQ-09W5-7	SOT25	8BQ
AP7343DQ-10W5-7	SOT25	8CQ
AP7343DQ-11W5-7	SOT25	8EQ
AP7343DQ-12W5-7	SOT25	8FQ
AP7343DQ-15W5-7	SOT25	8KQ
AP7343DQ-18W5-7	SOT25	8PQ
AP7343DQ-25W5-7	SOT25	8XQ
AP7343DQ-27W5-7	SOT25	8ZQ
AP7343DQ-28W5-7	SOT25	6JQ
AP7343DQ-29W5-7	SOT25	6MQ
AP7343DQ-30W5-7	SOT25	6PQ
AP7343DQ-33W5-7	SOT25	6TQ

### Marking Information (continued)

(2) W-DFN2020-6 (SWP) (Type A1)

(Top View)



XXXX : Identification Code

Y : Year : 0 to 9 (ex: 2 = 2022)

W : Week : A to Z : Week 1 to 26;

a to z : Week 27 to 52; z represents Week 52 and 53

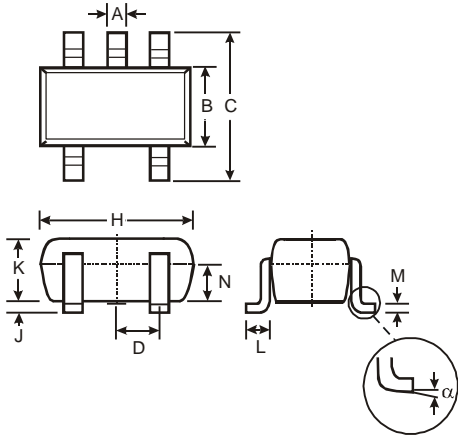
X : Internal Code

Part Number	Package	Identification Code
AP7343Q-09FDZW-7	W-DFN2020-6 (SWP) (Type A1)	7BQ
AP7343Q-10FDZW-7	W-DFN2020-6 (SWP) (Type A1)	7CQ
AP7343Q-11FDZW-7	W-DFN2020-6 (SWP) (Type A1)	7EQ
AP7343Q-12FDZW-7	W-DFN2020-6 (SWP) (Type A1)	7FQ
AP7343Q-15FDZW-7	W-DFN2020-6 (SWP) (Type A1)	7HQ
AP7343Q-18FDZW-7	W-DFN2020-6 (SWP) (Type A1)	7JQ
AP7343Q-185FDZW-7	W-DFN2020-6 (SWP) (Type A1)	7KQ
AP7343Q-25FDZW-7	W-DFN2020-6 (SWP) (Type A1)	7NQ
AP7343Q-27FDZW-7	W-DFN2020-6 (SWP) (Type A1)	7XQ
AP7343Q-28FDZW-7	W-DFN2020-6 (SWP) (Type A1)	7PQ
AP7343Q-29FDZW-7	W-DFN2020-6 (SWP) (Type A1)	8AQ
AP7343Q-30FDZW-7	W-DFN2020-6 (SWP) (Type A1)	7TQ
AP7343Q-33FDZW-7	W-DFN2020-6 (SWP) (Type A1)	7WQ
AP7343DQ-09FDZW-7	W-DFN2020-6 (SWP) (Type A1)	8BQ
AP7343DQ-10FDZW-7	W-DFN2020-6 (SWP) (Type A1)	8CQ
AP7343DQ-11FDZW-7	W-DFN2020-6 (SWP) (Type A1)	8EQ
AP7343DQ-12FDZW-7	W-DFN2020-6 (SWP) (Type A1)	8FQ
AP7343DQ-15FDZW-7	W-DFN2020-6 (SWP) (Type A1)	8KQ
AP7343DQ-18FDZW-7	W-DFN2020-6 (SWP) (Type A1)	8PQ
AP7343DQ-25FDZW-7	W-DFN2020-6 (SWP) (Type A1)	8XQ
AP7343DQ-27FDZW-7	W-DFN2020-6 (SWP) (Type A1)	8ZQ
AP7343DQ-28FDZW-7	W-DFN2020-6 (SWP) (Type A1)	6JQ
AP7343DQ-29FDZW-7	W-DFN2020-6 (SWP) (Type A1)	6MQ
AP7343DQ-30FDZW-7	W-DFN2020-6 (SWP) (Type A1)	6PQ
AP7343DQ-33FDZW-7	W-DFN2020-6 (SWP) (Type A1)	6TQ

**Package Outline Dimensions**

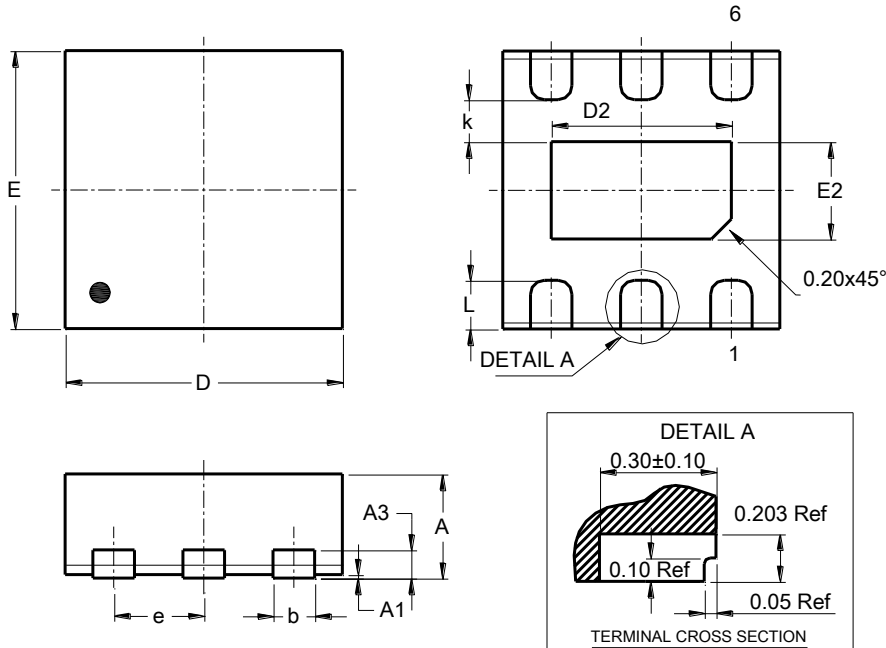
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) SOT25



SOT25			
Dim	Min	Max	Typ
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	-	-	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
N	0.70	0.80	0.75
α	0°	8°	-
All Dimensions in mm			

(2) W-DFN2020-6 (SWP) (Type A1)

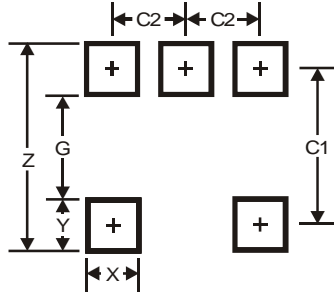


W-DFN2020-6 (SWP) (Type A1)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.25	0.35	0.30
D	2.00 BSC		
D2	1.35	1.45	1.40
E	2.00 BSC		
E2	0.55	0.65	0.60
e	0.65 BSC		
k	0.20	—	—
L	0.20	0.40	0.30
All Dimensions in mm			

## Suggested Pad Layout

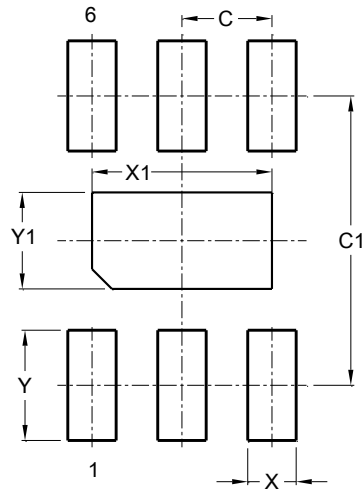
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) SOT25



Dimensions	Value (in mm)
Z	3.20
G	1.60
X	0.55
Y	0.80
C1	2.40
C2	0.95

(2) W-DFN2020-6 (SWP) (Type A1)



Dimensions	Value (in mm)
C	0.650
C1	2.100
X	0.350
X1	1.400
Y	0.800
Y1	0.600

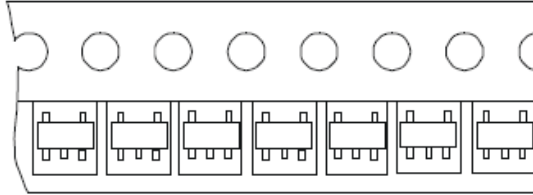
## Mechanical Data

- Moisture Sensitivity: Level 1 Per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 ③
- Weight:
  - SOT25: 0.016 grams (Approximate)
  - W-DFN2020-6 (SWP) (Type A1): 0.010 grams (Approximate)

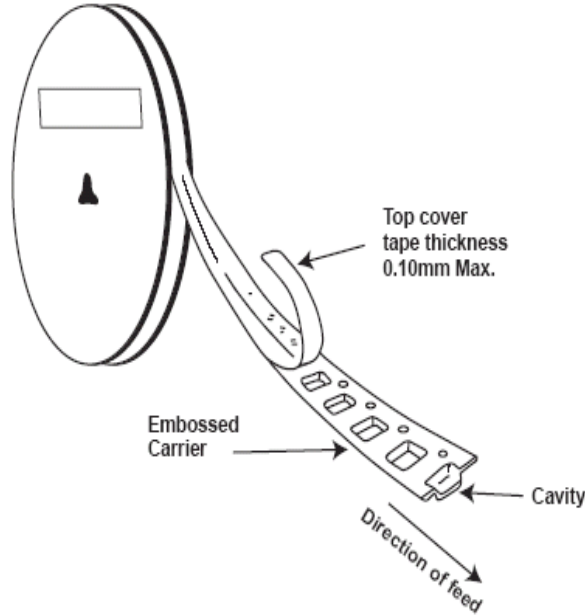
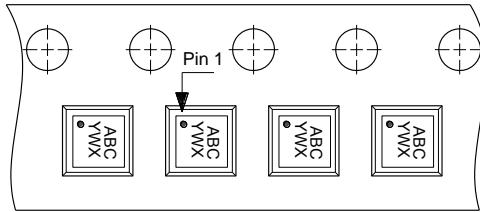


**Tape Orientation**

For AP7343Q-XXXW5-7 & AP7343DQ-XXXW5-7



For AP7343DQ-XXXFDZW-7



Note: 15. The taping orientation of the other package type can be found on our website at <https://www.diodes.com/assets/Packaging-Support-Docs/ap02007.pdf>.

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