

## Description

The AP7345D is a Dual low dropout regulator with high output voltage accuracy, low  $R_{DS(ON)}$ , high PSRR, low output noise and low quiescent current. This regulator is based on a CMOS process.

Each of regulators includes a voltage reference, error amplifier, current limit circuit and an enable input to turn on/ off output. With the integrated resistor network fixed output voltage versions can be delivered.

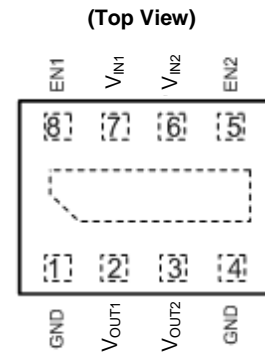
With its low power consumption and line and load transient response, the AP7345D is well suited for low power handheld communication equipment.

The AP7345D is packaged in X2-DFN1612-8 package and allows for smallest footprint and dense PCB layout.

## Features

- Low  $V_{IN}$  and Wide  $V_{IN}$  Range: 1.7V to 5.25V
- Guarantee Each Channel Output Current: 300mA
- $V_{OUT}$  Accuracy  $\pm 1\%$
- Ripple Rejection: 75dB at 1kHz
- Low Output Noise: 60 $\mu$ Vrms from 10Hz to 100kHz
- Quiescent Current as Low as 50 $\mu$ A
- $V_{OUT}$  Fixed 1.2V to 3.6V
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free, Green Device (Note 3)**

## Pin Assignments



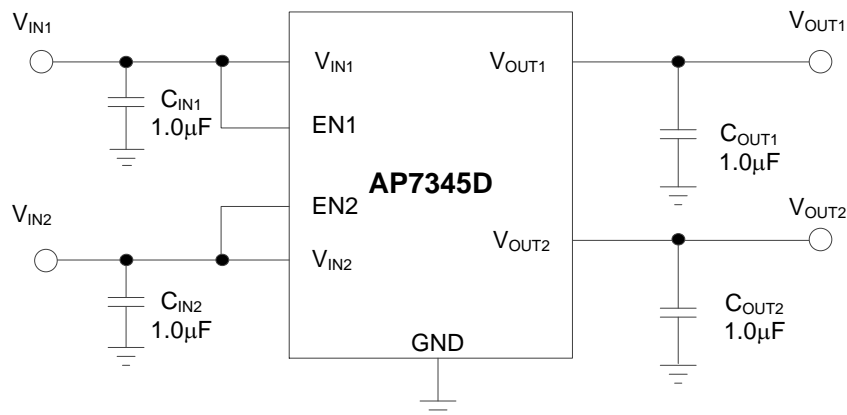
**X2-DFN1612-8**

## Applications

- Smart Phone/PAD
- RF Supply
- Cameras
- Portable Video
- Portable Media Player
- Wireless Adapter
- Wireless Communication

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Typical Applications Circuit

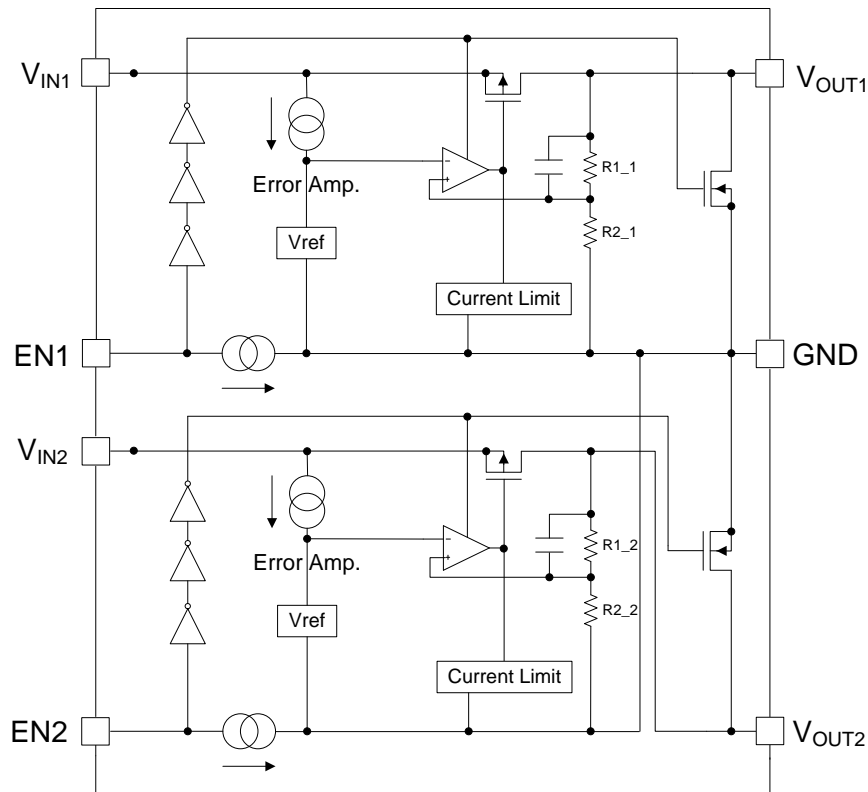


**Pin Descriptions**

Pin Number	Pin Name	Function
GND	1, 4	Ground
V <sub>OUT1</sub>	2	Channel 1 Output Voltage pin
V <sub>OUT2</sub>	3	Channel 2 Output Voltage pin
EN2	5	Channel 2 Enable pin. This pin should be driven either high or low and must not be floating. Driving this pin high enables channel 2 output, while pulling it low puts Channel 2 regulator into shutdown mode.
V <sub>IN2</sub>	6	Channel 2 Input Voltage pin
V <sub>IN1</sub>	7	Channel 1 Input Voltage pin
EN1	8	Channel 1 Enable pin. This pin should be driven either high or low and must not be floating. Driving this pin high enables channel 1 output, while pulling it low puts Channel 1 regulator into shutdown mode.
—	Thermal PAD	In PCB layout, prefer to use large copper area to cover this pad for better thermal dissipation, then connect this area to GND or leave it open. However do not use it as GND electrode function alone.

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**Functional Block Diagram**



**Absolute Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified. Note 4)

Symbol	Parameter	Rating	Unit
V <sub>IN</sub>	Input Voltage	6.0	V
V <sub>EN</sub>	Input Voltage at EN Pins	6.0	V
V <sub>OUT</sub>	Output Voltage	-0.3 to V <sub>IN</sub> +0.3	V
I <sub>OUT</sub>	Output Current	400	mA
P <sub>D</sub>	Power Dissipation	600	mW
T <sub>A</sub>	Operating Ambient Temperature	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C

Note 4: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**Recommended Operating Conditions** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V <sub>IN</sub>	Input Voltage	1.7	5.25	V
I <sub>OUT</sub>	Each Channel Output Current	0	300	mA
T <sub>A</sub>	Operating Ambient Temperature	-40	+85	°C

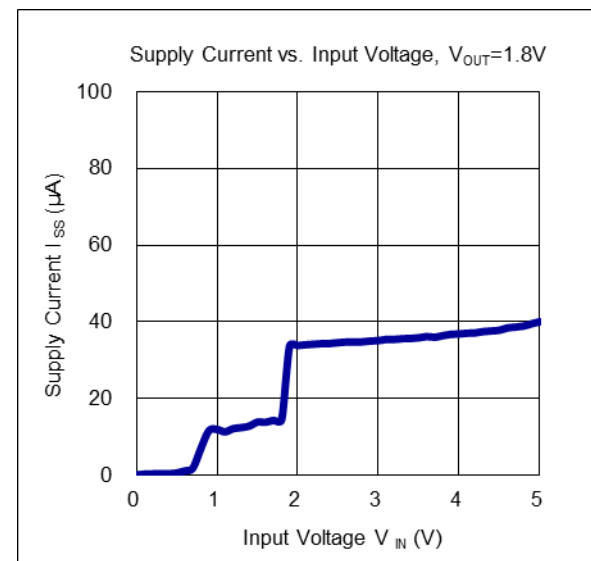
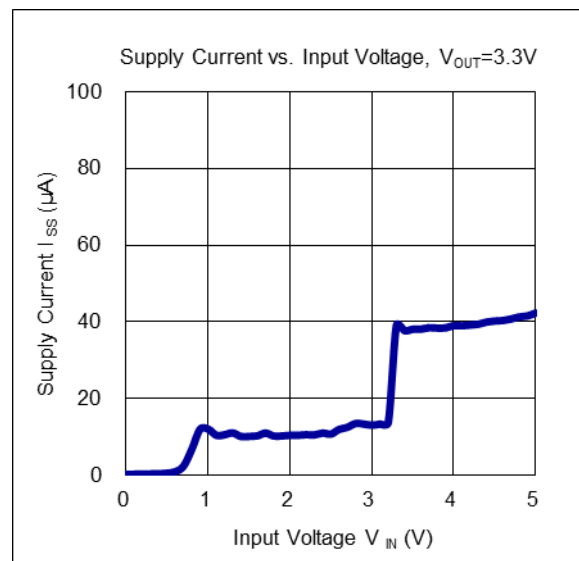
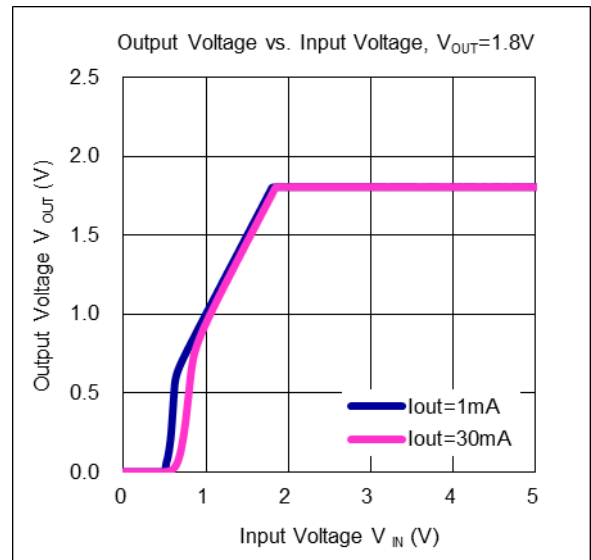
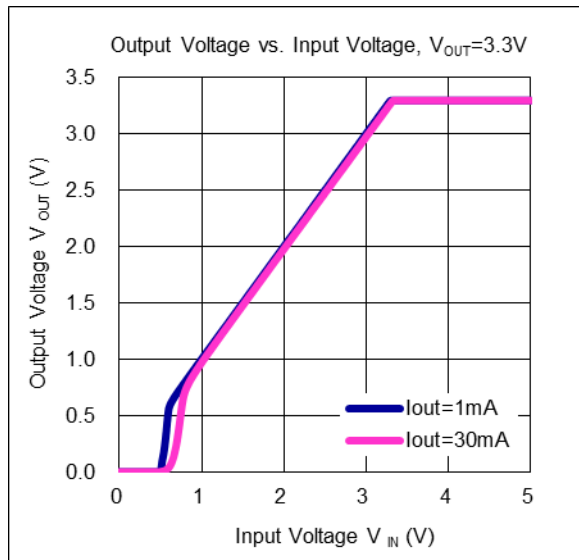
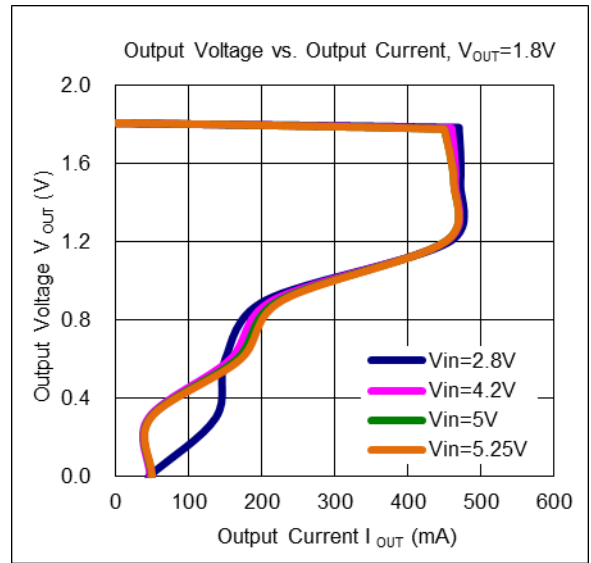
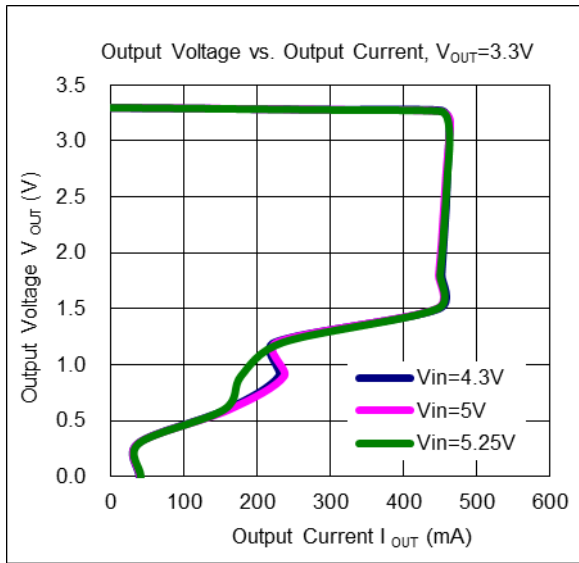
**Electrical Characteristics** (@ $T_A = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT} + 1\text{V}$  ( $V_{OUT} > 1.5\text{V}$ ),  $V_{IN} = 2.5\text{V}$  ( $V_{OUT} \leq 1.5\text{V}$ ),  $I_{OUT} = 1\text{mA}$ ,  $C_{IN} = C_{OUT} = 1.0\mu\text{F}$ , unless otherwise specified.)

Parameter	Conditions	Min	Typ	Max	Unit	
Input Voltage	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.7	—	5.25	V	
Output Voltage Accuracy (Note 11)	$V_{IN} = (V_{OUT-Nom} + 1.0\text{V})$ to 5.25V, $I_{OUT} = 1\text{mA}$ to 300mA	$T_A = +25^\circ\text{C}$	-1	—	1	%
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-1.5	—	1.5	
Line Regulation ( $\Delta V_{OUT}/\Delta V_{IN}/V_{OUT}$ )	$V_{IN} = (V_{OUT-Nom} + 1.0\text{V})$ to 5.25V, $I_{OUT} = 1.0\text{mA}$	—	0.02	0.1	%/V	
Load Regulation	$V_{IN} = V_{OUT-Nom} + 1.0\text{V}$ , $I_{OUT} = 1\text{mA}$ to 300mA	—	15	30	mV	
Quiescent Current (Note 6)	Set EN1 High, Set EN2 Low, or Set EN2 High, Set EN1 Low, No Load	—	50	70	$\mu\text{A}$	
	Set EN1/EN2 High, No Load	—	100	140	$\mu\text{A}$	
$I_{STANDBY}$	Set EN1/EN2 Low, No Load	—	0.1	1.0	$\mu\text{A}$	
Each Channel Output Current	—	300	—	—	mA	
Fold-back Short Current (Note 7)	$V_{OUT}$ short to ground	—	55	—	mA	
PSRR (Note 8)	$V_{IN} = (V_{OUT} + 1\text{V}) V_{DC} + 0.2\text{Vp-pAC}$ , $V_{OUT} \geq 1.8\text{V}$ , $I_{OUT} = 30\text{mA}$	$f = 1\text{kHz}$	—	75	—	dB
Output Noise Voltage (Notes 8 & 9)	BW = 10Hz to 100kHz, $I_{OUT} = 30\text{mA}$	—	60	—	$\mu\text{Vrms}$	
Dropout Voltage (Note 5)	$I_{OUT} = 30\text{mA}$	$V_{OUT} \leq 1.2\text{V}$	—	0.46	0.70	V
		$1.2\text{V} < V_{OUT} \leq 1.4\text{V}$	—	0.39	0.58	
		$1.4\text{V} < V_{OUT} \leq 1.7\text{V}$	—	0.35	0.44	
		$1.7\text{V} < V_{OUT} \leq 2.1\text{V}$	—	0.30	0.39	
		$2.1\text{V} < V_{OUT} \leq 2.5\text{V}$	—	0.26	0.34	
		$2.5\text{V} < V_{OUT} \leq 3.0\text{V}$	—	0.25	0.30	
		$3.0\text{V} < V_{OUT} \leq 3.6\text{V}$	—	0.22	0.29	
Output Voltage Temperature Coefficient	$I_{OUT} = 30\text{mA}$ , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	—	$\pm 30$	—	ppm/ $^\circ\text{C}$	
Thermal Shutdown Threshold (TSHDN)	—	—	+150	—	$^\circ\text{C}$	
Thermal Shutdown Hysteresis (THYS)	—	—	+20	—	$^\circ\text{C}$	
EN Input Low Voltage	—	0	—	0.5	V	
EN Input High Voltage	—	1.3	—	5.25	V	
EN Input Leakage	$V_{EN} = 0\text{V}$ , $V_{IN} = 5.0\text{V}$ or $V_{EN} = 5.0\text{V}$ , $V_{IN} = 0\text{V}$	-1.0	—	1.0	$\mu\text{A}$	
On Resistance of N-channel for Auto-discharge (Note 10)	$V_{IN} = 4.0\text{V}$ , $V_{EN} = 0\text{V}$ (Disabled)	D Version, Chanel 1 & 2	—	30	—	$\Omega$

- Notes:
- Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.
  - Quiescent current is defined here is the difference in current between the input and the output.
  - Short circuit current is measured with  $V_{OUT}$  pulled to GND.
  - This specification is guaranteed by design.
  - To make sure lowest environment noise minimizes the influence on noise measurement.
  - AP7345D has 2 options for output, built-in discharge and non-discharge.
  - Potential multiple grades based on following output voltage accuracy.

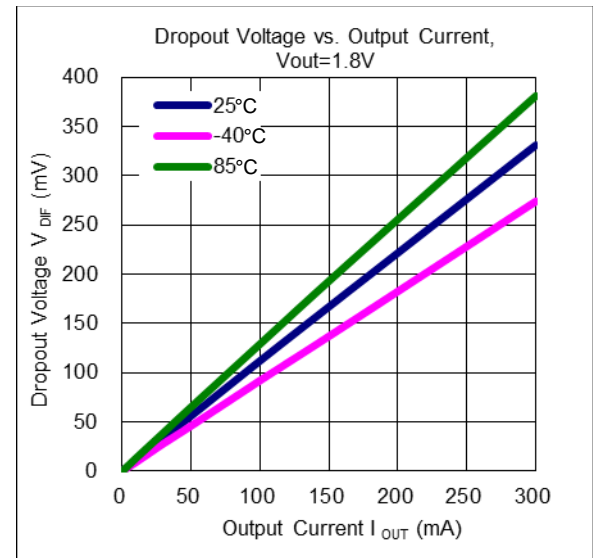
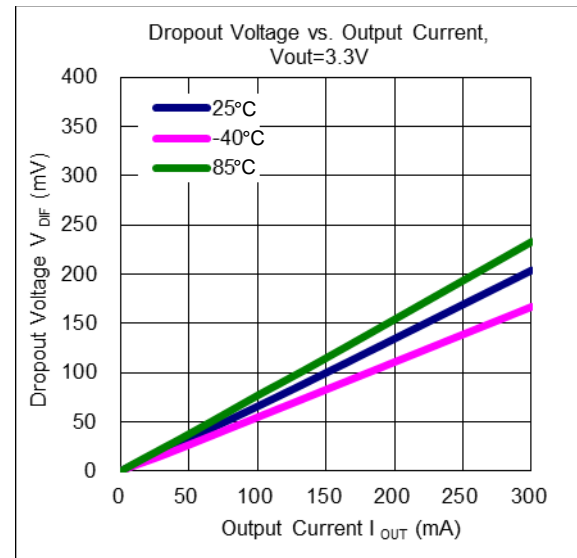
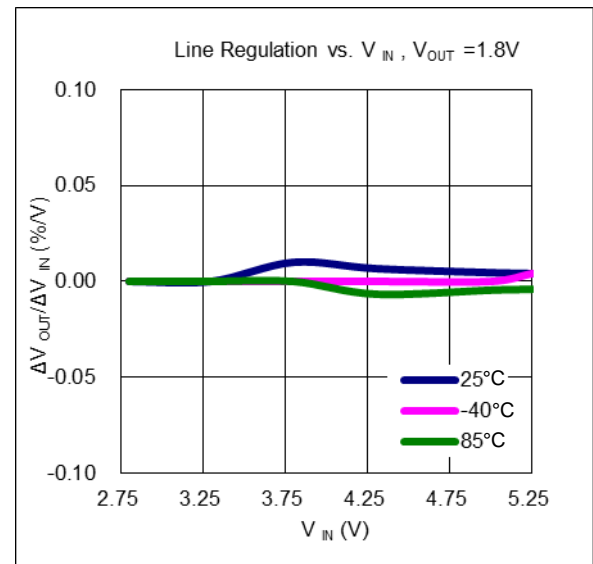
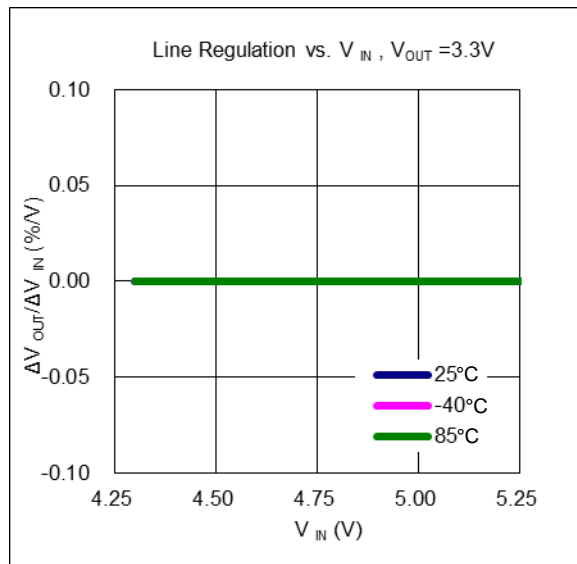
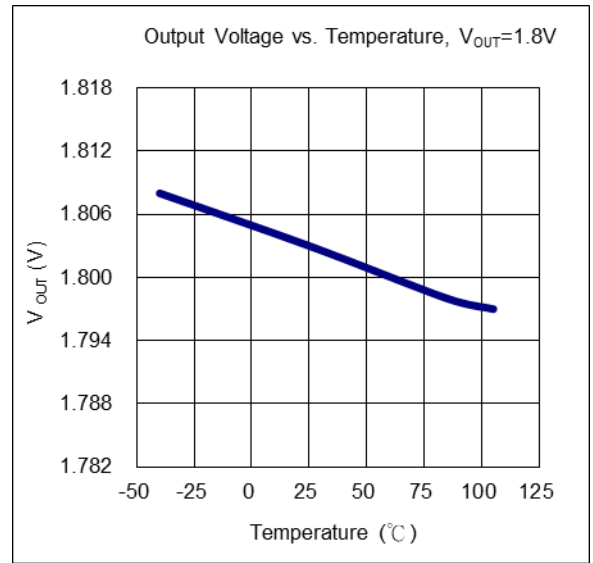
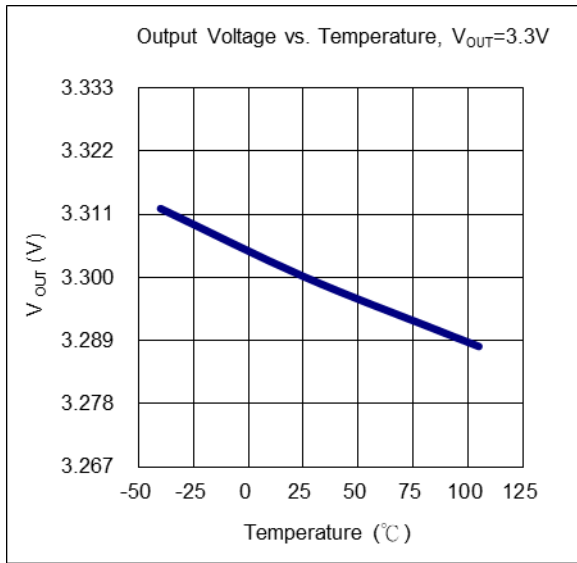
**Performance Characteristics**

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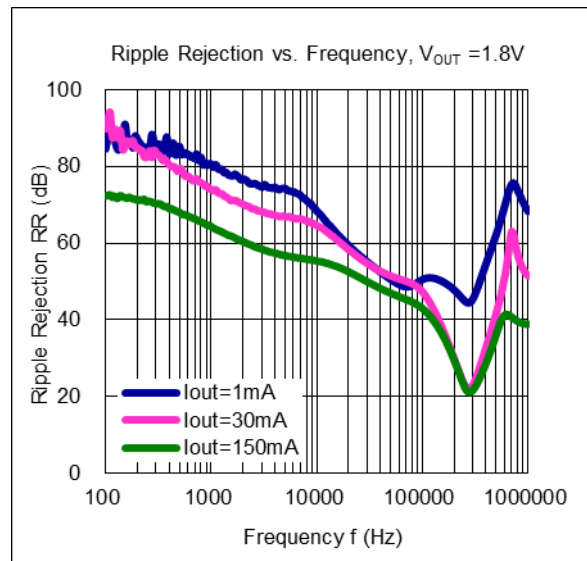
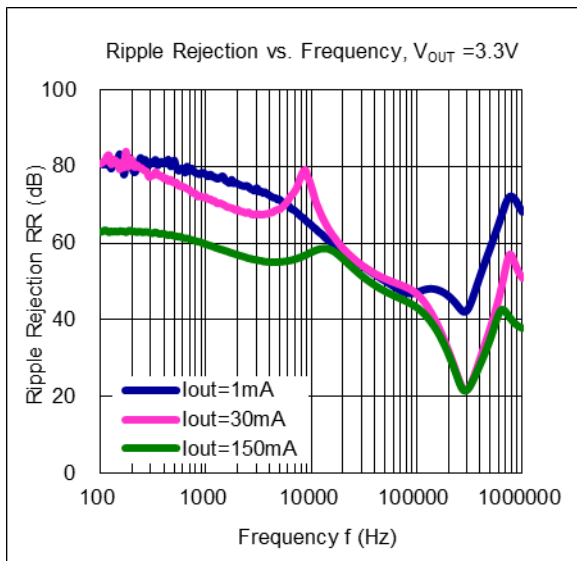
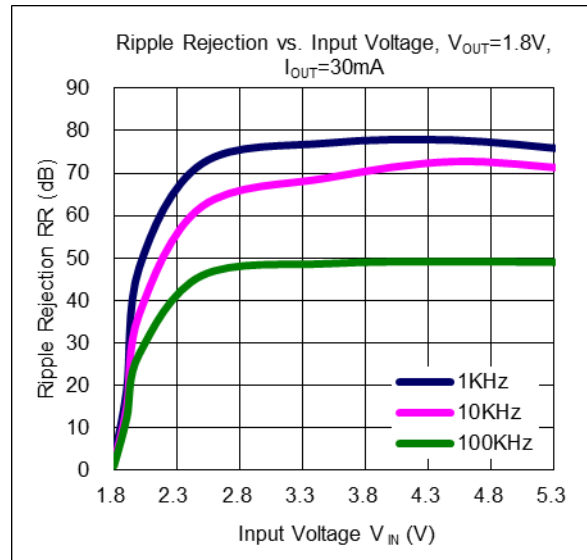
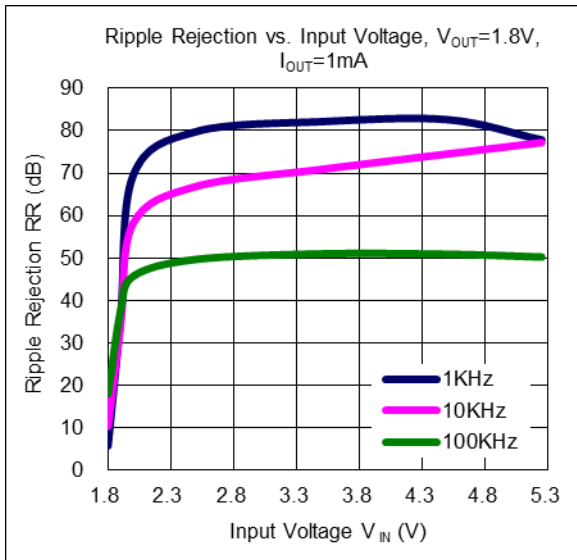
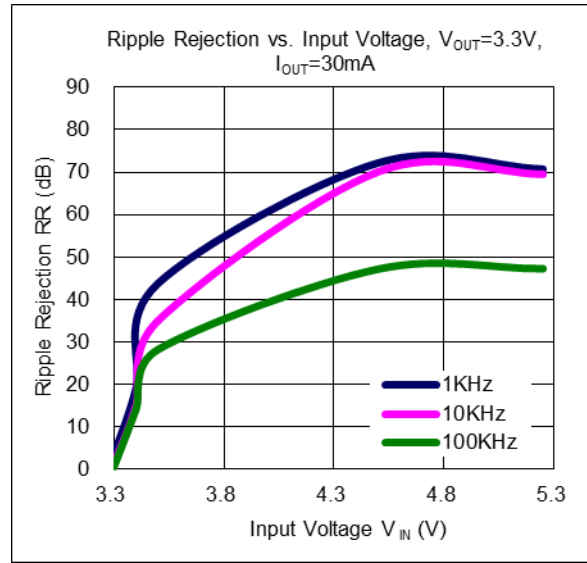
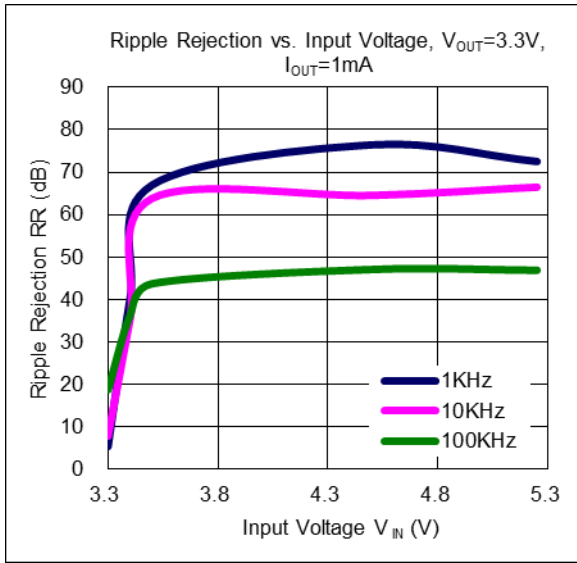
Performance Characteristics (Cont.)

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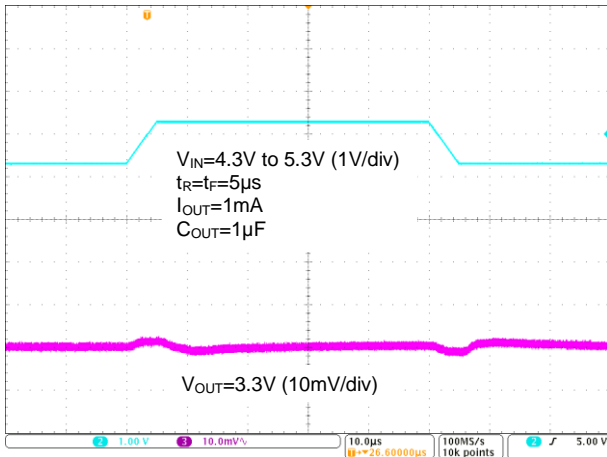
Performance Characteristics (Cont.)

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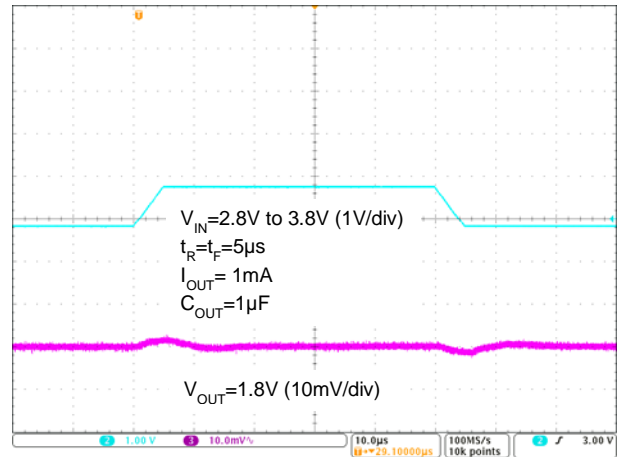


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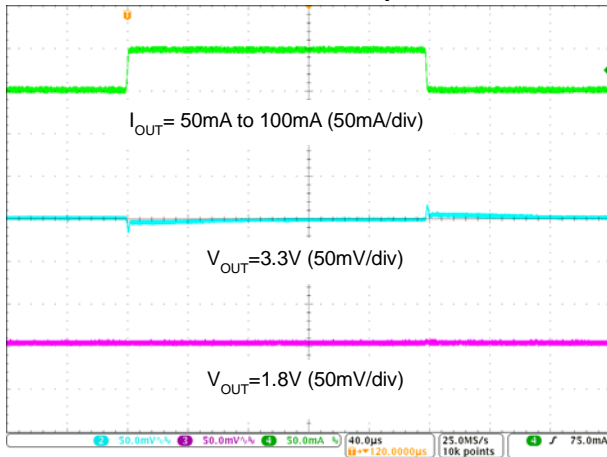
Line Transient Response



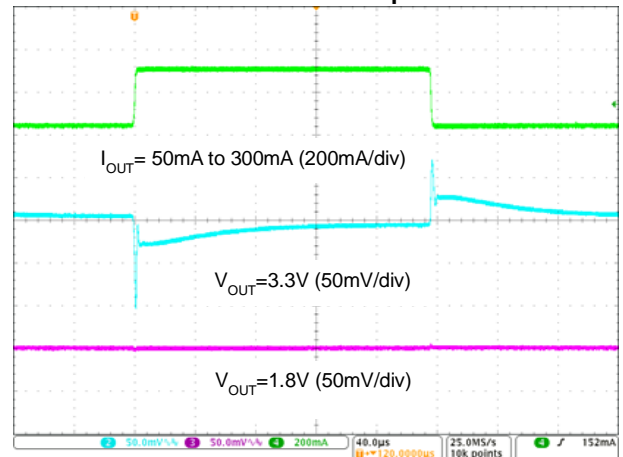
Line Transient Response



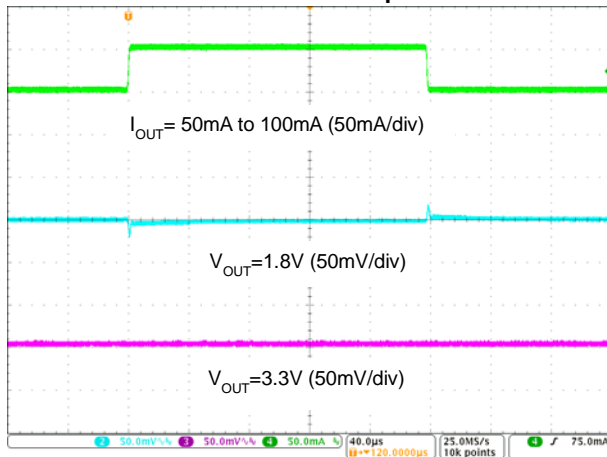
Load Transient Response



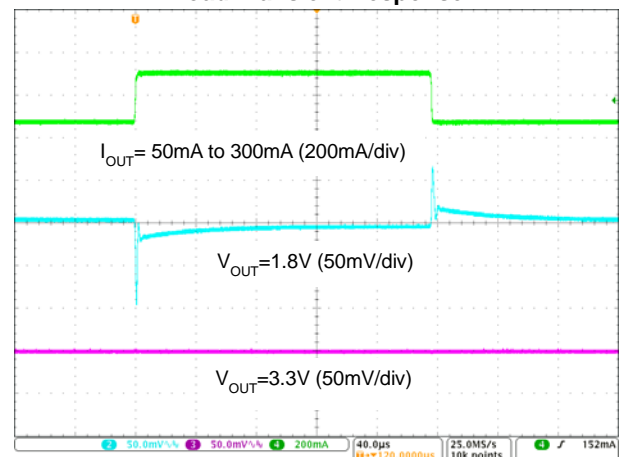
Load Transient Response



Load Transient Response



Load Transient Response

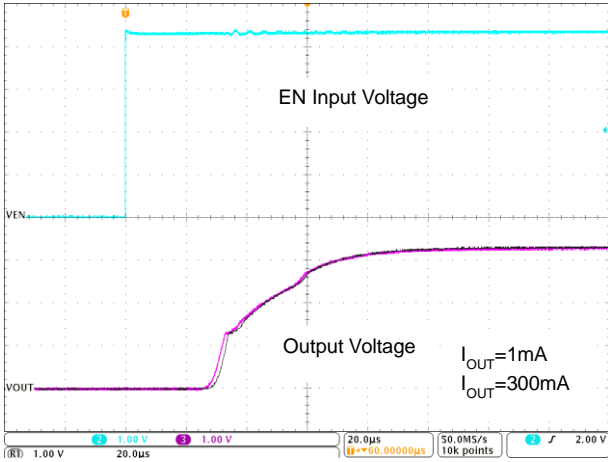


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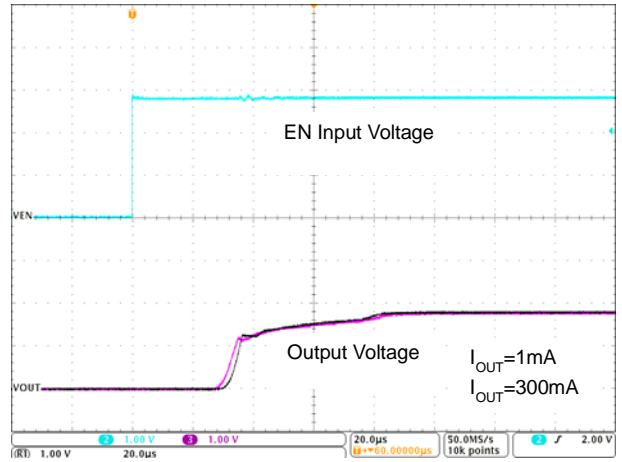
Performance Characteristics (Cont.)

Turn on Waveform,  $V_{OUT}=3.3V$



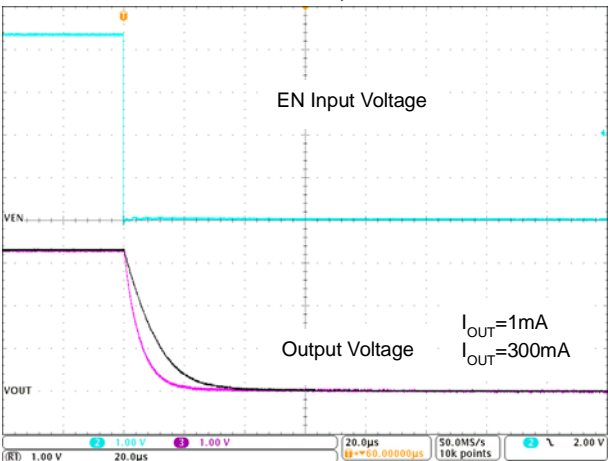
Time (20µs/div)

Turn on Waveform,  $V_{OUT}=1.8V$



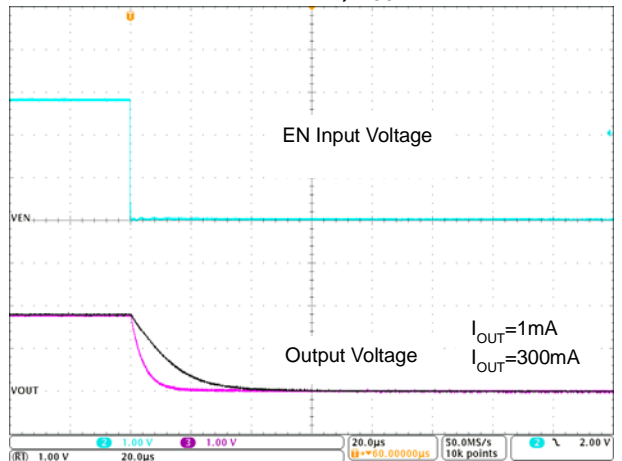
Time (20µs/div)

Turn off Waveform,  $V_{OUT}=3.3V$



Time (20µs/div)

Turn off Waveform,  $V_{OUT}=1.8V$



Time (20µs/div)

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## Application Information

### Output Capacitor

An output capacitor ( $C_{OUT}$ ) is needed to improve transient response and maintain stability. The AP7345D is stable with very small ceramic output capacitors. The ESR (Equivalent Series Resistance) and capacitance drives the selection. If the application has large load variations, it is recommended to utilize low-ESR bulk capacitors. It is recommended to place ceramic capacitors as close as possible to the load and the GND pins and care should be taken to reduce the impedance in the layout.

### Input Capacitor

To prevent the input voltage from dropping during load steps, it is recommended to utilize an input capacitor ( $C_{IN}$ ). A minimum  $1\mu\text{F}$  ceramic capacitor is recommended between  $V_{IN}$  and GND pins to decouple input power supply glitch. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both  $V_{IN}$  and GND pins.

### Enable Control

The AP7345D is turned on by setting the EN pins high, and is turned off by pulling it low. If this feature is not used, the EN pins should be tied to  $V_{IN}$  pins to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pins must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section.

### Short Circuit Protection

When  $V_{OUT}$  pins are short-circuit to GND, short circuit protection will be triggered and clamp the output current to approximately 60mA. This feature protects the regulator from over-current and damage due to overheating.

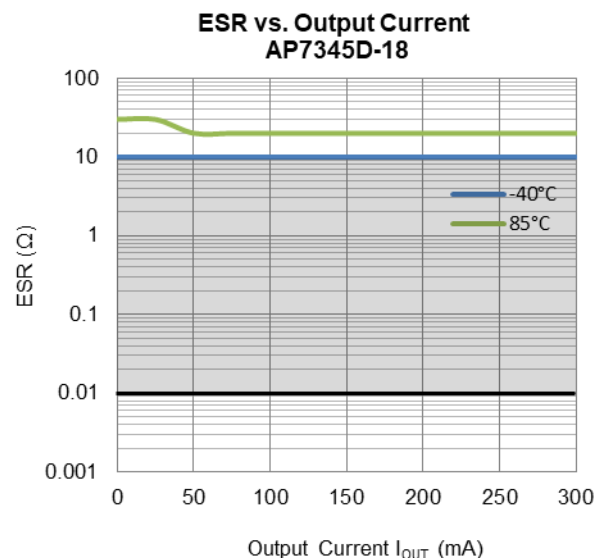
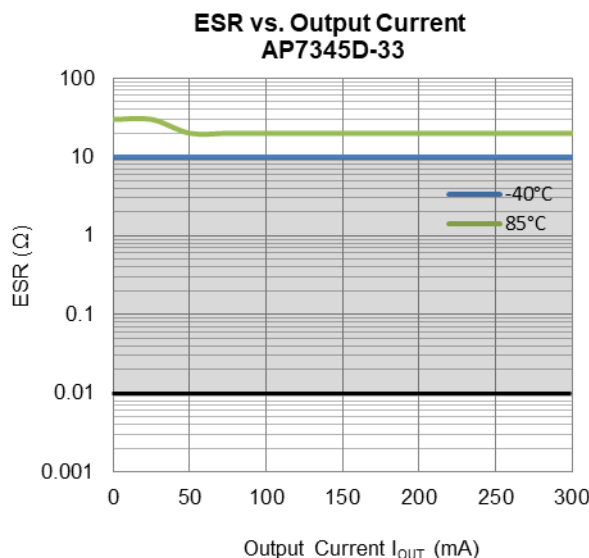
### Layout Considerations

For good ground loop and stability, the input and output capacitors should be located close to the input, output, and GND pins of the device. The regulator GND pins should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance. Wide trace should be used for large current paths from  $V_{IN}$  to  $V_{OUT}$ , and load circuit.

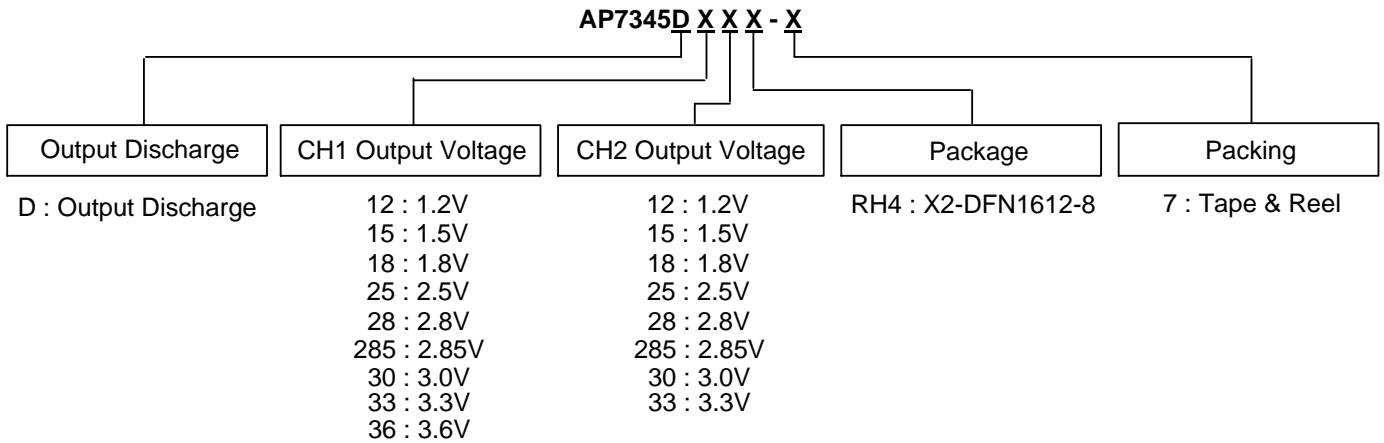
## ESR vs. Output Current

Ceramic type output capacitor is recommended for this series; however, the other output capacitors with low ESR also can be used. The relations between  $I_{OUT}$  (Output Current) and ESR of an output capacitor are shown below. The stable region is marked as the hatched area in the graph.

Measurement conditions: Frequency Band: 10Hz to 2MHz, Temperature:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .



## Ordering Information

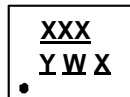


Part Number	Package Code	Packaging	7" Tape and Reel	
			Quantity	Part Number Suffix
AP7345D-XXXX(XX)RH4-7	RH4	X2-DFN1612-8	5000/Tape & Reel	-7

## Marking Information

(1) X2-DFN1612-8

(Top View)



**XXX** : Identification Code  
**Y** : Year : 0~9  
**W** : Week : A~Z : 1~26 week;  
           a~z : 27~52 week; z represents  
           52 and 53 week  
**X** : Internal code

Part Number	V <sub>OUT1</sub> /V <sub>OUT2</sub>	Package	Identification Code
AP7345D-1218RH4-7	1.2V/1.8V	X2-DFN1612-8	FAA
AP7345D-1528RH4-7	1.5V/2.8V	X2-DFN1612-8	FAB
AP7345D-1812RH4-7	1.8V/1.2V	X2-DFN1612-8	FAC
AP7345D-1815RH4-7	1.8V/1.5V	X2-DFN1612-8	FAD
AP7345D-1818RH4-7	1.8V/1.8V	X2-DFN1612-8	FAE
AP7345D-1828RH4-7	1.8V/2.8V	X2-DFN1612-8	FAF
AP7345D-1833RH4-7	1.8V/3.3V	X2-DFN1612-8	FAG
AP7345D-2518RH4-7	2.5V/1.8V	X2-DFN1612-8	FAH

## Marking Information (Cont.)

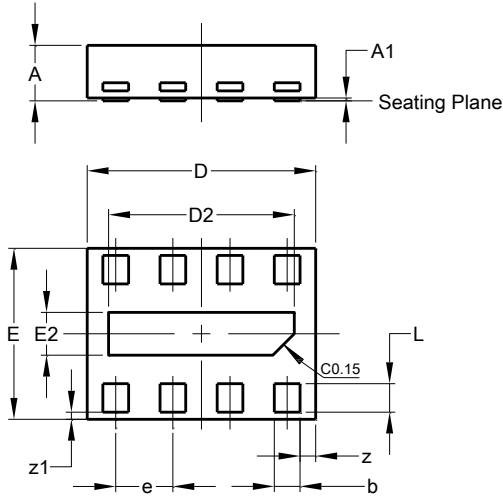
Part Number	V <sub>OUT1</sub> /V <sub>OUT2</sub>	Package	Identification Code
AP7345D-2812RH4-7	2.8V/1.2V	X2-DFN1612-8	FAJ
AP7345D-2818RH4-7	2.8V/1.8V	X2-DFN1612-8	FAK
AP7345D-2825RH4-7	2.8V/2.5V	X2-DFN1612-8	FAM
AP7345D-2833RH4-7	2.8V/3.3V	X2-DFN1612-8	FAN
AP7345D-2828RH4-7	2.8V/2.8V	X2-DFN1612-8	FAP
AP7345D-285285RH4-7	2.85V/2.85V	X2-DFN1612-8	FAR
AP7345D-3018RH4-7	3.0V/1.8V	X2-DFN1612-8	FAS
AP7345D-3028RH4-7	3.0V/2.8V	X2-DFN1612-8	FAT
AP7345D-3030RH4-7	3.0V/3.0V	X2-DFN1612-8	FAU
AP7345D-3318RH4-7	3.3V/1.8V	X2-DFN1612-8	FAV
AP7345D-3328RH4-7	3.3V/2.8V	X2-DFN1612-8	FAW
AP7345D-3330RH4-7	3.3V/3.0V	X2-DFN1612-8	FAX
AP7345D-3333RH4-7	3.3V/3.3V	X2-DFN1612-8	FAY
AP7345D-3612RH4-7	3.6V/1.2V	X2-DFN1612-8	FAZ

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**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DFN1612-8

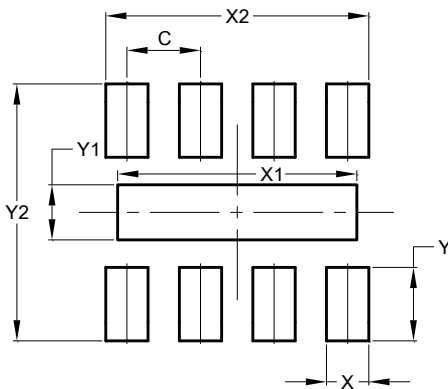


X2-DFN1612-8			
Dim	Min	Max	Typ
A	—	0.40	0.39
A1	0.00	0.05	0.02
b	0.13	0.23	0.18
D	1.55	1.65	1.60
D2	1.25	1.35	1.30
E	1.15	1.25	1.20
E2	0.25	0.35	0.30
e	—	—	0.40
L	0.15	0.25	0.20
z	—	—	0.11
z1	—	—	0.05
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

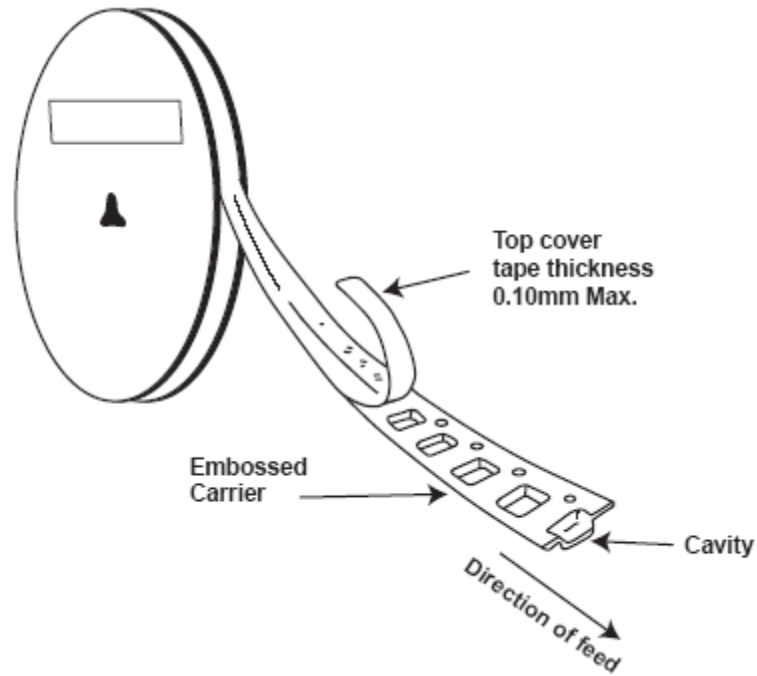
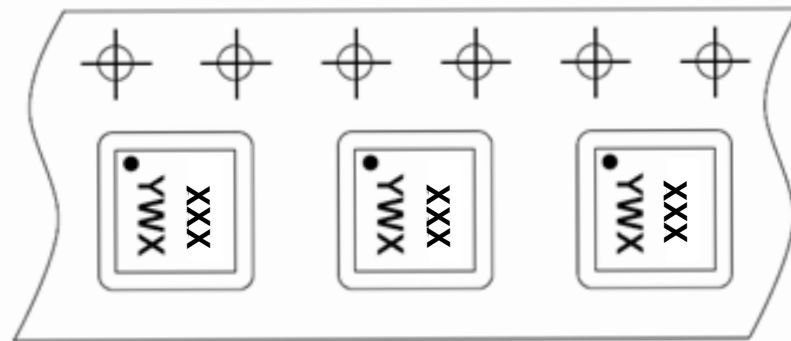
X2-DFN1612-8



Dimensions	Value (in mm)
C	0.400
X	0.230
X1	1.300
X2	1.430
Y	0.400
Y1	0.300
Y2	1.400

NEW PRODUCT

## Tape Orientation



Note: The taping orientation of the other package type can be found on our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

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