1.5A, LOW QUIESCENT CURREENT, FAST TRANSIENT ULTRA-LOW DROPOUT LINEAR REGULATOR

Description

The AP7362 is a 1.5A adjustable output voltage linear regulator with ultra-low dropout. The device includes pass element, error amplifier, band-gap, current limit and thermal shutdown circuitry. The integrated Enable block allows the part to be turned on and off via a logic signal. A logic high level on EN turns the device on and a logic low turns the part off.

The low dropout voltage characteristics and fast transient response to step changes in load make it suitable for low voltage microprocessor applications. The typical quiescent current is approximately 0.5mA and changes little with load current. The built-in current-limit and thermal-shutdown functions prevent damage to the IC in fault conditions.

This device is available in U-DFN2030-8 and SO-8EP packages.

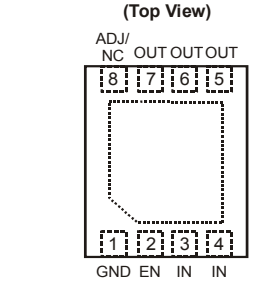
Features

- 1.5A Ultra-Low Dropout Linear Regulator with EN
- Ultra-Low Dropout: 190mV at 1.5A
- Stable with 10µF Input/Output Capacitor, any type
- Wide Input Voltage Range: 2.2V to 5.5V
- Adjustable Output Voltage: 0.6V to 5.0V
- Fixed Output Options: 1V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V
- Low Ground Pin Current
- 25nA Quiescent Current in Shutdown Mode
- V_{ADJ} Accuracy of ±1.5% @ +25°C
- V_{ADJ} Accuracy of ±3% Over Line, Load and Temperature
- Excellent Load/Line Transient Response
- Current Limit and Thermal Shutdown Protection
- Ambient Temperature Range: -40°C to +85°C
- U-DFN2030-8, SO-8EP: Available in Lead free “Green” Molding Compound (No Br, Sb)
  - **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
  - **Halogen and Antimony Free. “Green” Device (Note 3)**

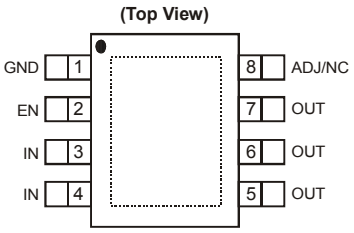
Applications

- ASIC Power Supplies in Printers, Graphics Cards, DVD Players, STBs, Routers, etc
- FPGA and DSP Core or I/O Power Supplies
- SMPS Regulator
- Conversion from 3.3V or 5V Rail

Pin Assignments

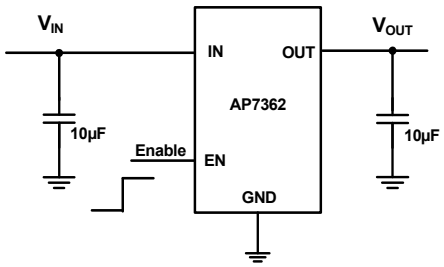


U-DFN2030-8

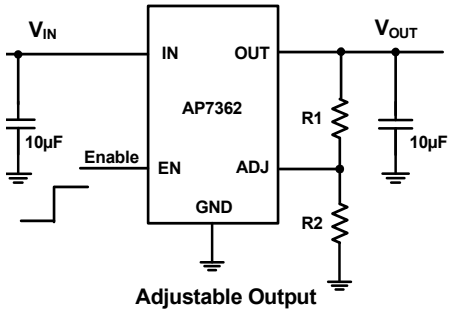


SO-8EP

Typical Application Circuit



Fixed Output



Adjustable Output

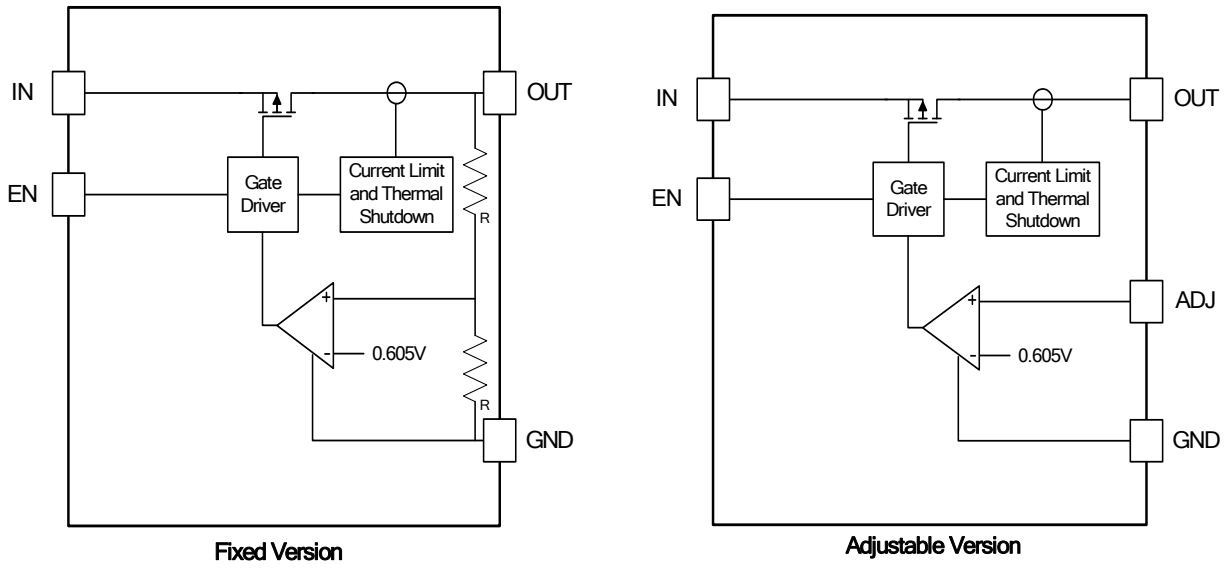
$$V_{OUT} = V_{REF}\left(1+\frac{R_1}{R_2}\right) \text{ where } R_2 \le 10k\Omega$$

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Descriptions

Pin Name	Pin Number	Function
GND	1	Ground.
EN	2	Enable input, active high.
IN	3, 4	Voltage input pin.
OUT	5, 6, 7	Voltage output pin.
ADJ	8	Output feedback pin for adjustable version only – a resistor divider from this pin to the OUT pin and ground sets the output voltage.
NC	8	No connection for fixed output version.
EP	EP	The exposed pad (EP) is used to remove heat from the package and it is recommended that it is connected to a copper area. The die is electrically connected to the exposed pad. It is recommended to connect it externally to GND, but should not be the only ground connection.

Functional Block Diagram



Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body Model ESD Protection	2000	V
ESD MM	Machine Model ESD Protection	200	V
V_{IN}	Input Voltage	-0.3 to +6.0	V
V_{OUT}, V_{EN}	OUT, EN Voltage	-0.3V to V_{IN} +0.3	V
I_{OUT}	Continuous Load Current	Internal Limited	
T_{ST}	Storage Temperature Range	-65 to +150	°C
T_J	Maximum Junction Temperature	150	°C

Note: 4. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress Ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input voltage	2.2	5.5	V
I_{OUT}	Output Current	0	1.5	A
T_A	Operating Ambient Temperature	-40	+85	°C
T_J	Operating Junction Temperature (Note 5)	-40	+125	°C

Note: 5. Operating junction temperature must be evaluated and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature (T_{J-MAX}), and package thermal resistance (θ_{JA}).

Electrical Characteristics

(@T_A = +25°C, V_{IN} = 3.3V, V_{OUT} =1.8V, I_{OUT} = 10mA, V_{EN} = V_{IN}, C_{IN} = 10µF, C_{OUT} = 10µF, V_{EN} = 2V, unless otherwise stated.)

Minimum and maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = +25°C, and are provided for reference purposes only.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{ADJ}	ADJ Pin Voltage	V_{IN} = V_{IN-MIN} to V_{IN-MAX}, I_{OUT} = 10mA to 1.5A	T_A = +25°C	0.584	0.605	0.626	V
			Over temp	0.575		0.635	
V_{ADJ}	ADJ Pin Voltage (A Grade)	V_{IN} = V_{IN-MIN} to V_{IN-MAX}, I_{OUT} = 10mA to 1.5A	T_A = +25°C	0.596	0.605	0.614	V
			Over temp	0.587		0.623	
I_{ADJ}	ADJ Pin Bias Current	V_{IN} = V_{IN-MIN} to V_{IN-MAX}	T_A = +25°C		50		nA
			Over temp			750	
$V_{DROPOUT}$	Dropout Voltage (Note 6)	I_{OUT} = 1.5A, V_{OUT} = 2.5V	T_A = +25°C		190	240	mV
			Over temp			280	
ΔV_{OUT} /ΔV_{IN}	Line Regulation (Note 7)	V_{IN} = V_{IN-MIN} to V_{IN-MAX}	T_A = +25°C	-	0.04	-	%/V
			Over temp		0.05		
ΔV_{OUT} /ΔI_{OUT}	Load Regulation (Note 7)	I_{OUT} = 10mA to 1.5A	T_A = +25°C	-	0.18	-	%/A
			Over temp		0.33		
I_{GND}	Ground Pin Current in Normal Operation Mode	I_{OUT} = 10mA to 1.5A	T_A = +25°C		1	1.2	mA
			Over temp			1.3	
I_{SHDN}	Ground Pin Current	V_{EN} < V_{IL}	T_A = +25°C		0.025	0.125	µA
			Over temp			15	
I_{OUT-PK}	Peak Output Current	V_{OUT} ≥ $V_{OUT-NOM}$ -5%			3.6		A
I_{SC}	Short Circuit Current	OUT grounded	T_A = +25°C		3.7		A
			Over temp	2			
V_{IH}	Enable Logic High	V_{IN} = V_{IN-MIN} to V_{IN-MAX}	Over temp	1.4			V
V_{IL}	Enable Logic Low	V_{IN} = V_{IN-MIN} to V_{IN-MAX}	Over temp			0.65	
I_{IH}	Enable Pin High Current	V_{EN} = V_{IN}			1		nA
I_{IL}	Enable Pin Low Current	V_{EN} = 0V			0.1		
$t_{d(OFF)}$	Turn-Off Delay	From V_{EN} < V_{IL} to V_{OUT} = OFF, I_{OUT} = 1.5A			25		µs
$t_{d(ON)}$	Turn-On Delay	From V_{EN} > V_{IH} to V_{OUT} = ON, I_{OUT} = 1.5A			25		µs

Notes: 6. Dropout voltage is the minimum voltage difference between the input and the output at which the output voltage drops 2% below its nominal value. For any output voltage less than 2.5V, the minimum V_{IN} operating voltage is the limiting factor.
7. The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the adjust voltage tolerance specification.

Electrical Characteristics (cont.)

(@T_A = +25°C, V_{IN} = 3.3V, V_{OUT} =1.8V, I_{OUT} = 10mA, V_{EN} = V_{IN}, C_{IN} = 10µF, C_{OUT} = 10µF, V_{EN} = 2V, unless otherwise stated.)

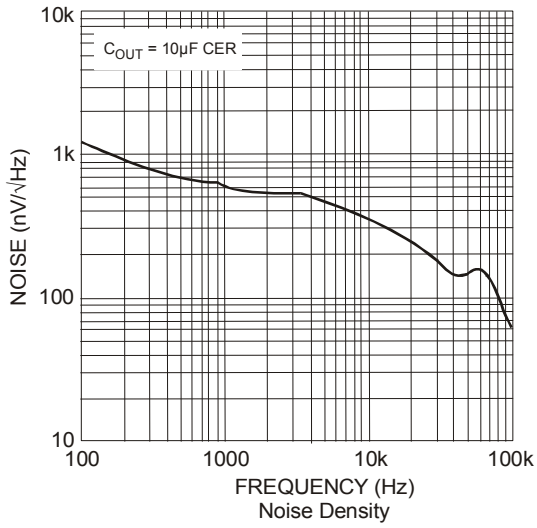
Minimum and maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = +25°C, and are provided for reference purposes only.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
PSRR	Ripple Rejection	V_{IN} = 3.0V, I_{OUT} = 1.5A, f = 120Hz		65		dB
		V_{IN} = 3.0V, I_{OUT} = 1.5A, f = 1kHz		61		
$\rho_{n(l/f)}$	Output Noise Density	f = 120Hz, C_{OUT} = 10µF ceramic		1.0		µV/√Hz
e_n	Output Noise Voltage	BW = 100Hz – 100kHz, C_{OUT} = 10µF ceramic		90		µV(rms)
T_{SHDN}	Thermal shutdown threshold	T_J rising		170		°C
T_{HYS}	Thermal shutdown hysteresis	T_J falling from T_{SHDN}		10		
θ_{JA}	Thermal Resistance Junction-to-Ambient	U-DFN2030-8 (Note 8)		85.0		°C/W
		SO-8EP (Note 8)		52.8		
θ_{JC}	Thermal Resistance Junction-to-Case	U-DFN2030-8 (Note 8)		17.0		°C/W
		SO-8EP (Note 8)		10.0		

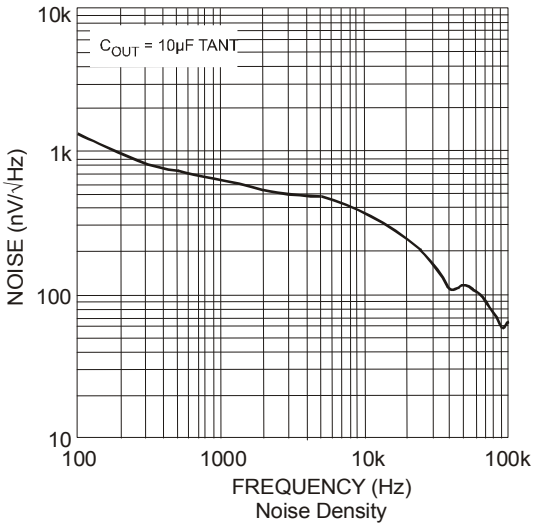
Note: 8. Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper with minimum recommended pad layout.

Typical Performance Characteristics

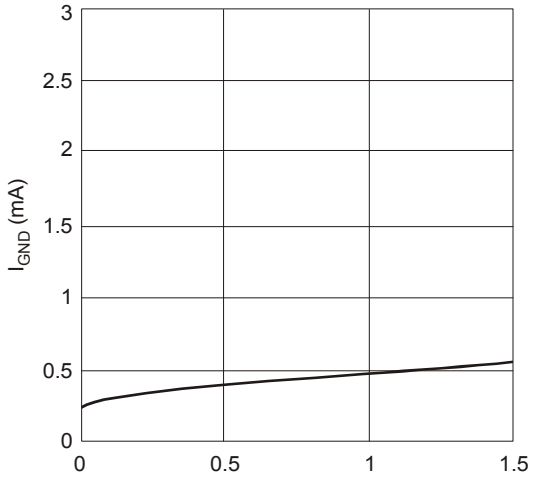
(@T_A = +25°C, V_{IN} = 2.7V, V_{EN} = V_{IN}, C_{IN} = 10µF, C_{OUT} = 10µF, I_{OUT} = 10mA, V_{OUT} = 1.8V, unless otherwise stated.)



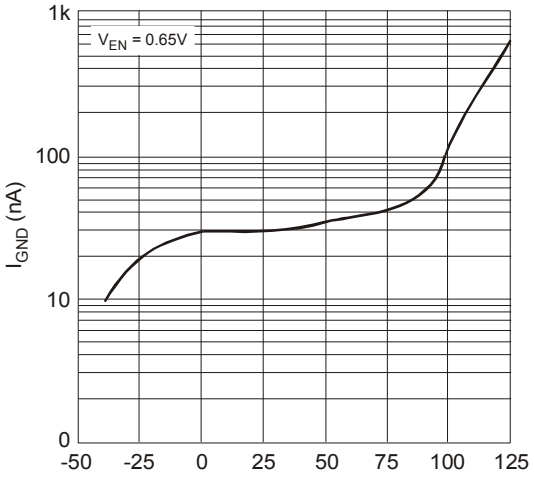
Noise Density



Noise Density



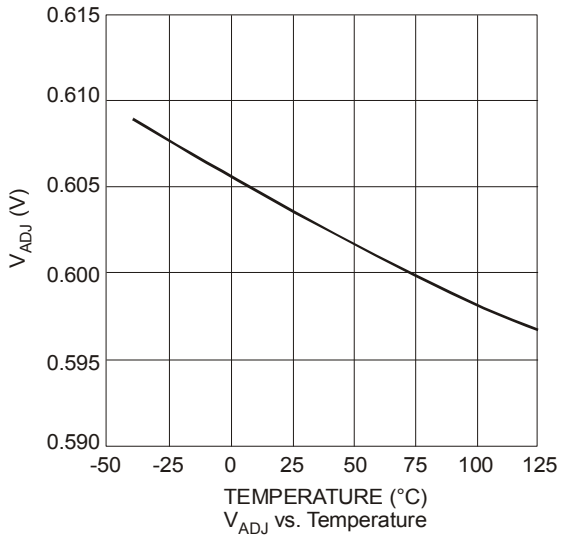
I_{GND} vs. Load Current



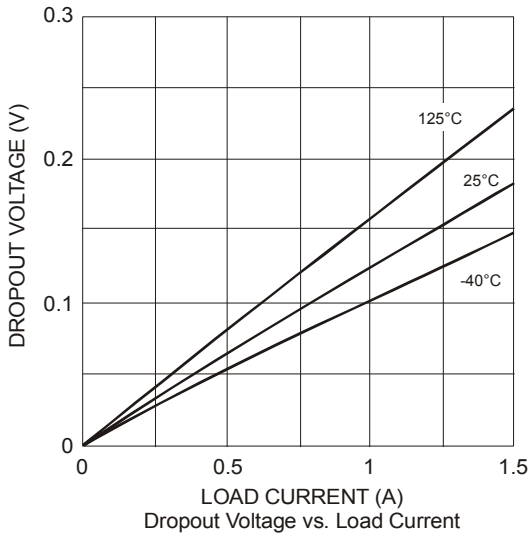
$I_{GND(OFF)}$ vs. Temperature

Typical Performance Characteristics (cont.)

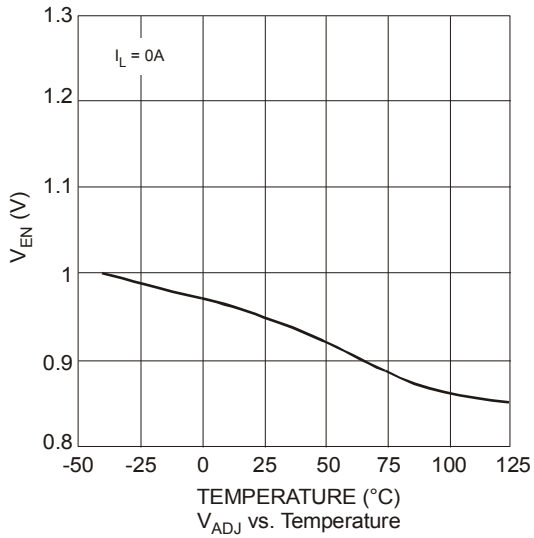
(@T_A = +25°C, V_{IN} = 2.7V, V_{EN} = V_{IN}, C_{IN} = 10µF, C_{OUT} = 10µF, I_{OUT} = 10mA, V_{OUT} = 1.8V, unless otherwise stated.)



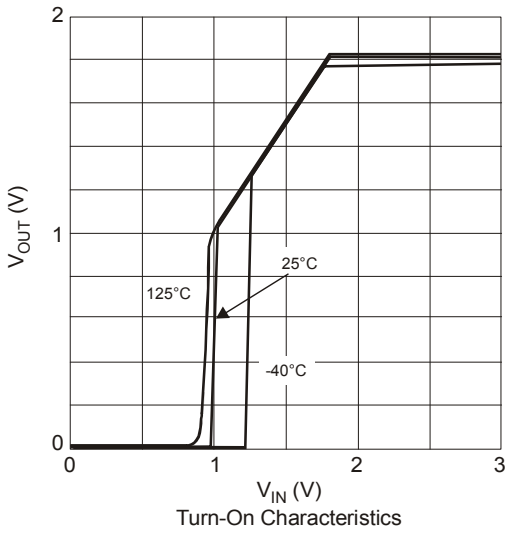
V_{ADJ} vs. Temperature



Dropout Voltage vs. Load Current



V_{ADJ} vs. Temperature

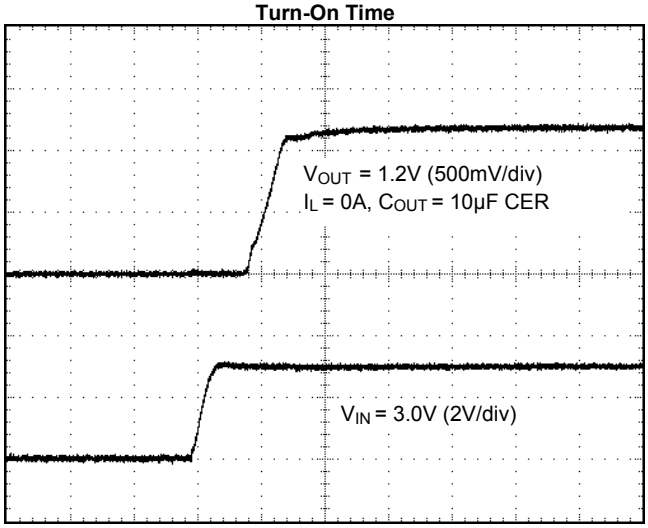


Turn-On Characteristics

Typical Performance Characteristics (cont.)

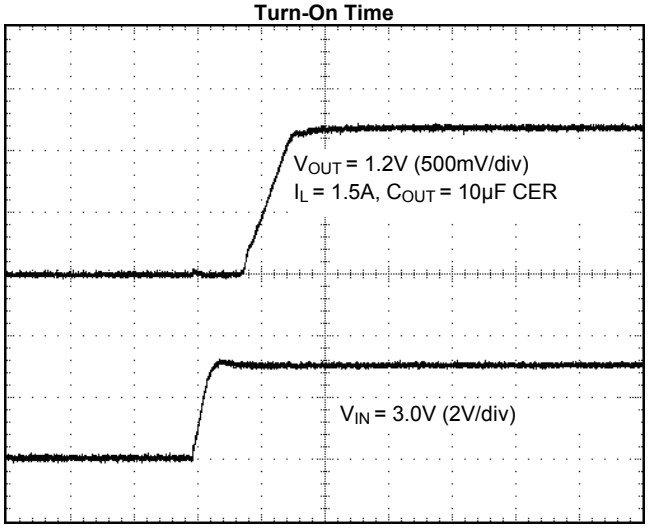
(@T_A = +25°C, V_{IN} = 2.7V, V_{EN} = V_{IN}, C_{IN} = 10µF, C_{OUT} = 10µF, I_{OUT} = 10mA, V_{OUT} = 1.8V, unless otherwise stated.)

Turn-On Time



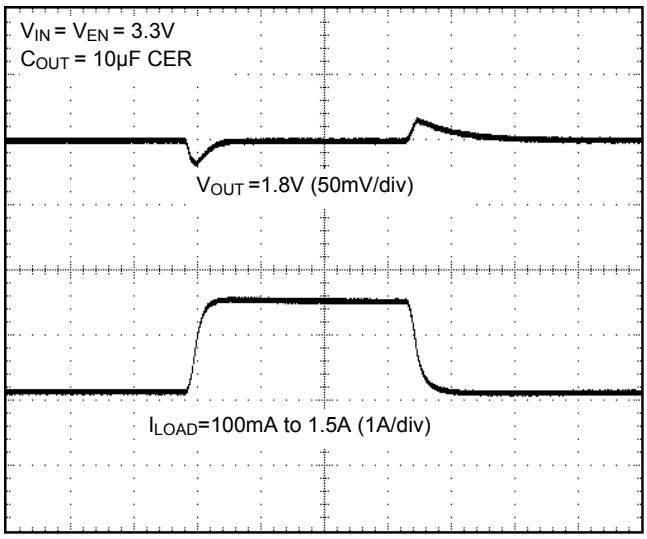
Time (10µs/div)

Turn-On Time

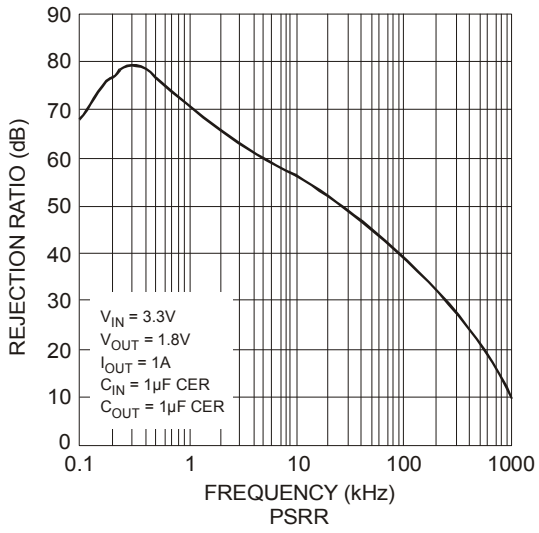


Time (10µs/div)

Load Transient Response



Time (40µs/div)



Application Information

Input Capacitor

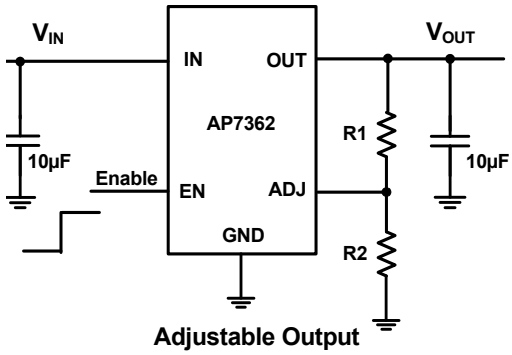
A minimum 2.2μF ceramic capacitor is recommended between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. Larger input capacitor like 10μF will provide better load transient response. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both IN and GND pins. A lower ESR capacitor type allows the use of less capacitance, while higher ESR type requires more capacitance.

Output Capacitor

The output capacitor is required to stabilize and help the transient response of the LDO. The AP7362 is stable with any type of capacitor, with no limitations on minimum or maximum ESR. The device is designed to have excellent transient response for most applications with a small amount of output capacitance. The device is also stable with multiple capacitors in parallel, which can be of any type of value. Additional capacitance helps to reduce undershoot and overshoot during transient loads. This capacitor should be placed as close as possible to OUT and GND pins for optimum performance.

Adjustable Operation

The AP7362 provides output voltage from 0.6V to 5.0V through external resistor divider as shown below.



Adjustable Output

The output voltage is calculated by:

$$V_{OUT} = V_{REF}\left(1+\frac{R_1}{R_2}\right)$$

Where V_{REF} = 0.6V (the internal reference voltage)

Rearranging the equation will give the following that is used for adjusting the output to a particular voltage:

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}}-1\right)$$

To maintain the stability of the internal reference voltage, R_2 need to be kept smaller than 10kΩ.

No Load Stability

Other than external resistor divider, no minimum load is required to keep the device stable. The device will remain stable and regulated in no load condition.

Application Information (cont.)

Stability and Phase Margin

Any regulator which operates using a feedback loop must be compensated in such a way as to ensure adequate phase margin, which is defined as the difference between the phase shift and -180 degrees at the frequency where the loop gain crosses unity (0 dB). For most LDO regulators, the ESR of the output capacitor is required to create a zero to add enough phase lead to ensure stable operation. The AP7362 has an internal compensation circuit which maintains phase margin regardless of the ESR of the output capacitor, any type of capacitor can be used.

Below two charts show the gain/phase plot of the AP7362 with an output of 1.2V, 10μF ceramic output capacitor, delivering 1.5A load current and no load. It can be seen the phase margin is about 90° (which is very stable).

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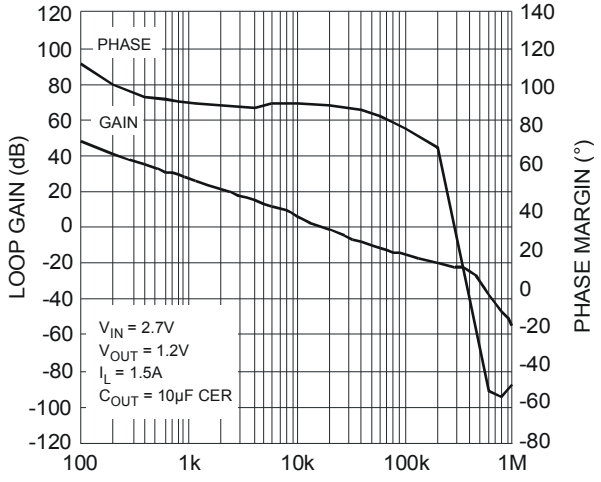
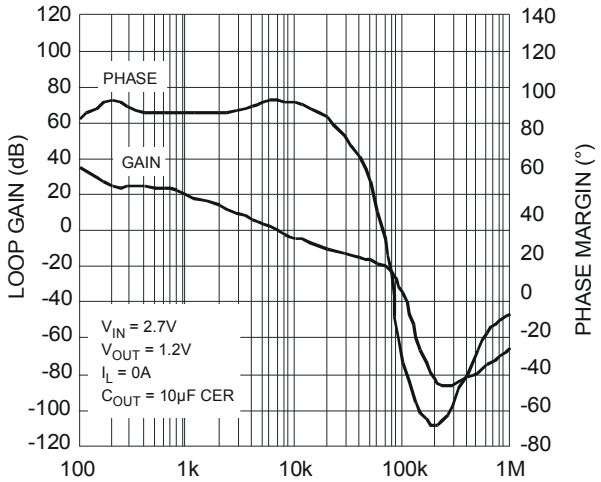


Gain-Bandwidth Plot for 1.5A Load



Gain-Bandwidth Plot for no Load

ON/OFF Input Operation

The AP7362 is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

Application Information (cont.)

Short Circuit Protection

When output current at OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to prevent over-current and to protect the regulator from damage due to overheating.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +170°C, allowing the device to cool down. When the junction temperature reduces to approximately +160°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits
the heat dissipation of the regulator, protecting it from damage due to overheating.

Low Quiescent Current

The AP7362, consumes only around 0.5mA for all input voltage range and load currents, this provides great power saving in portable and low power applications.

Output Noise

This is the integrated value of the output noise over a specified frequency range. Input voltage and output load current are kept constant during the measurement. Results are expressed in μVrms or μV √Hz.
The AP7362 is a low noise regulator and needs no external noise reduction capacitor. Output voltage noise is typically 100μVrms overall noise level between 100 Hz and 100 kHz

Noise is specified in two ways:

Output noise density is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.

Output noise voltage is the RMS sum of spot noise over a specified bandwidth. Spot noise is measured in units μV/√Hz or nV/√Hz and total output noise is measured in μV(RMS). The primary source of noise in low-dropout regulators is the internal reference.

Power Dissipation

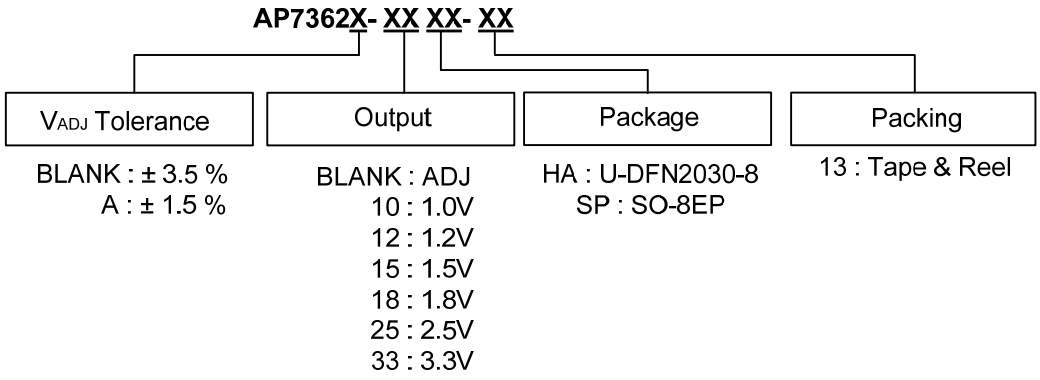
The device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoid thermal shutdown and ensure reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated by:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The maximum power dissipation, handled by the device, depends on the junction to ambient thermal resistance, and maximum ambient temperature, which can be calculated by the equation in the following:

$$P_{D\_MAX} = \frac{(+150°C - T_A)}{R_{\theta JA}}$$

Ordering Information

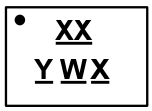


Part Number	Package Code	Packaging	7"/13" Tape and Reel	
			Quantity	Part Number Suffix
AP7362-XXHA-7	HA	U-DFN2030-8	3000/Tape & Reel	-7
AP7362A-XXHA-7	HA	U-DFN2030-8	3000/Tape & Reel	-7
AP7362-XXSP-13	SP	SO-8EP	2500/Tape & Reel	-13
AP7362A-XXSP-13	SP	SO-8EP	2500/Tape & Reel	-13

Marking Information

(1) U-DFN2030-8

(Top View)

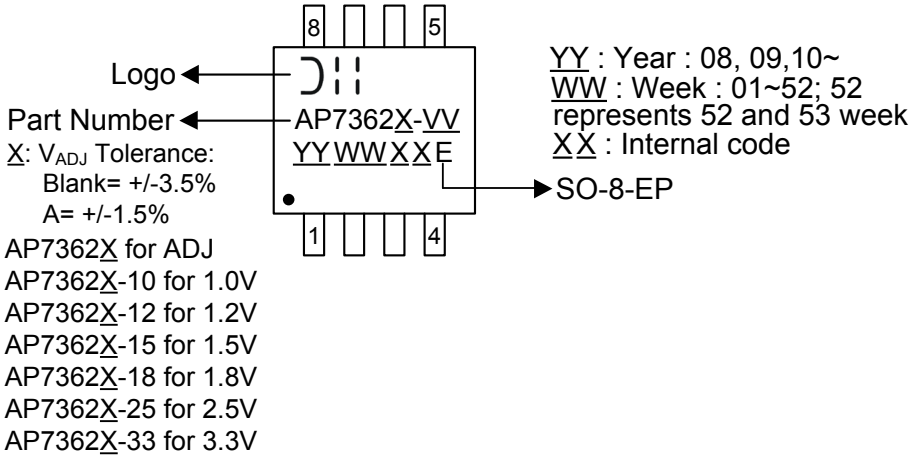


XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : A~Z : Internal code

Device	Package	Identification Code
AP7362 (ADJ)	U-DFN2030-8	RA
AP7362-10	U-DFN2030-8	RB
AP7362-12	U-DFN2030-8	RC
AP7362-15	U-DFN2030-8	RD
AP7362-18	U-DFN2030-8	RE
AP7362-25	U-DFN2030-8	RF
AP7362-33	U-DFN2030-8	RG
AP7362A (ADJ)	U-DFN2030-8	QA
AP7362A-10	U-DFN2030-8	QB
AP7362A-12	U-DFN2030-8	QC
AP7362A-15	U-DFN2030-8	QD
AP7362A-18	U-DFN2030-8	QE
AP7362A-25	U-DFN2030-8	QF
AP7362A-33	U-DFN2030-8	QG

(2) SO-8EP

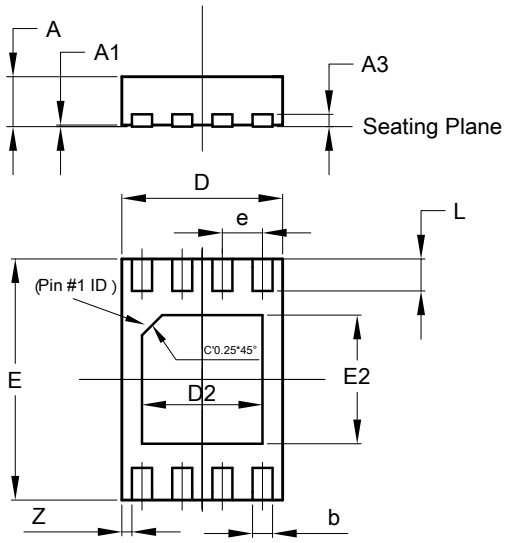
(Top View)



Package Outline Dimensions (All dimensions in mm.)

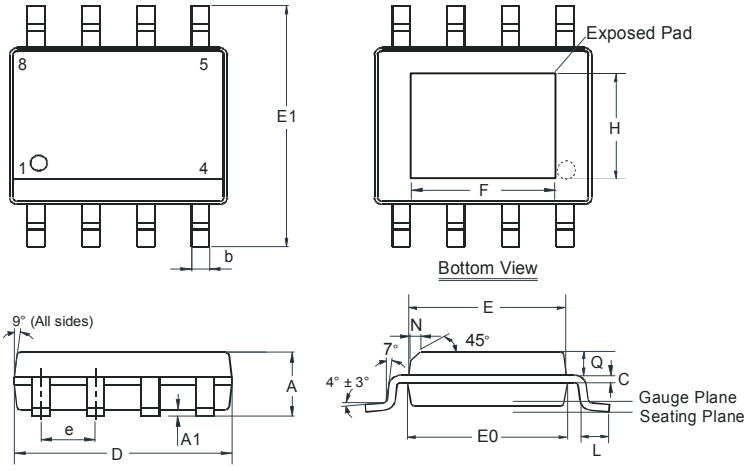
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.

(1) U-DFN2030-8



U-DFN2030-8			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	1.95	2.05	2.00
D2	1.40	1.60	1.50
e	-	-	0.50
E	2.95	3.05	3.00
E2	1.50	1.70	1.60
L	0.35	0.45	0.40
Z	-	-	0.125
All Dimensions in mm			

(2) SO-8EP

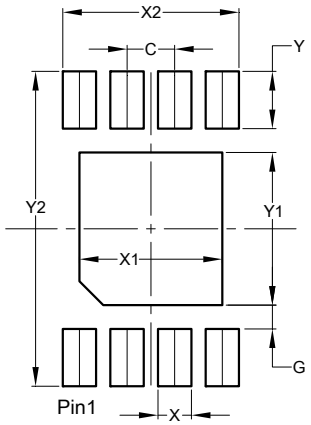


SO-8EP (SOP-8L-EP)			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

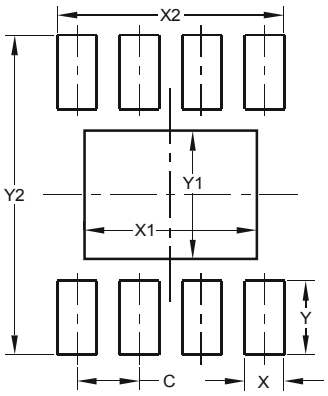
Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

(1) U-DFN2030-8



Dimensions	Value (in mm)
C	0.500
G	0.250
X	0.350
X1	1.500
X2	1.850
Y	0.600
Y1	1.600
Y2	3.300

(2) SO-8EP



Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

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