Description

The AUR9705 is a high efficiency step-down DC-DC voltage converter. The chip operation is optimized using constant frequency, peak-current mode architecture with built-in synchronous power MOSFET switchers and internal compensators to reduce external part counts. It is automatically switching between the normal PWM mode and LDO mode to offer improved system power efficiency covering a wide range of loading conditions.

The oscillator and timing capacitors are all built-in providing an internal switching frequency of 1.5MHz that allows the use of small surface mount inductors and capacitors for portable product implementations. Additional features included Soft Start (SS), Under Voltage Lock Out (UVLO) and Thermal Shutdown Detection (TSD) to provide reliable product applications.

The device is available in adjustable output voltage versions ranging from 1V to 3.3V, and is able to deliver up to 1A.

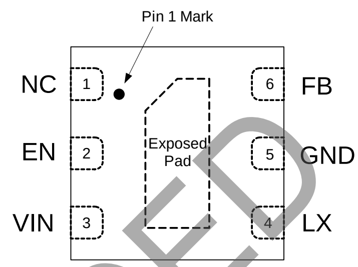
The AUR9705 is available in WDFN-2×2-6 and TSOT-23-5 packages.

Features

- High Efficiency Buck Power Converter
- Low Quiescent Current
- Output Current: 1A
- Adjustable Output Voltage from 1V to 3.3V
- Wide Operating Voltage Range: 2.5V to 5.5V
- Built-In Power Switches for Synchronous Rectification with High Efficiency
- Feedback Voltage: 600mV
- 1.5MHz Constant Frequency Operation
- Automatic PWM/LDO Mode Switching Control
- Thermal Shutdown Protection
- Low Drop-Out Operation at 100% Duty Cycle
- No Schottky Diode Required

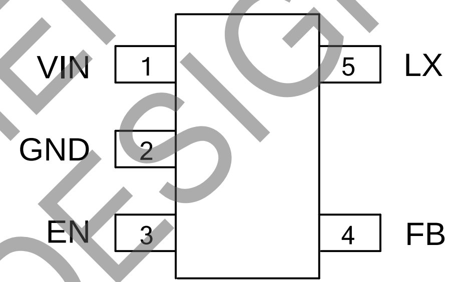
Pin Assignments

(Top View)



WDFN-2×2-6

(Top View)

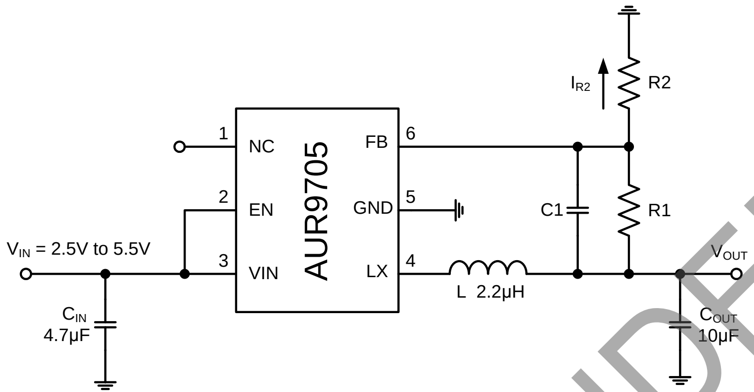


TSOT-23-5

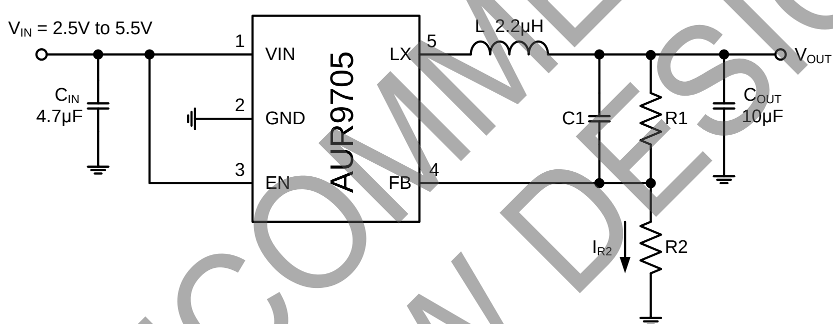
Applications

- Mobile Phone, Digital Camera and MP3 Player
- Headset, Radio and Other Hand-held Instrument
- Post DC-DC Voltage Regulation
- PDA and Notebook Computer

Typical Applications Circuit



For WDFN-2×2-6



For TSOT-23-5

Note 1: $V_{OUT} = V_{FB} \times (1 + \frac{R_1}{R_2})$.

When R2=300kΩ to 60kΩ, the I_{R2}=2μA to 10μA, and R1×C1 should be in the range between 3×10^{-6} and 6×10^{-6} for component selection.

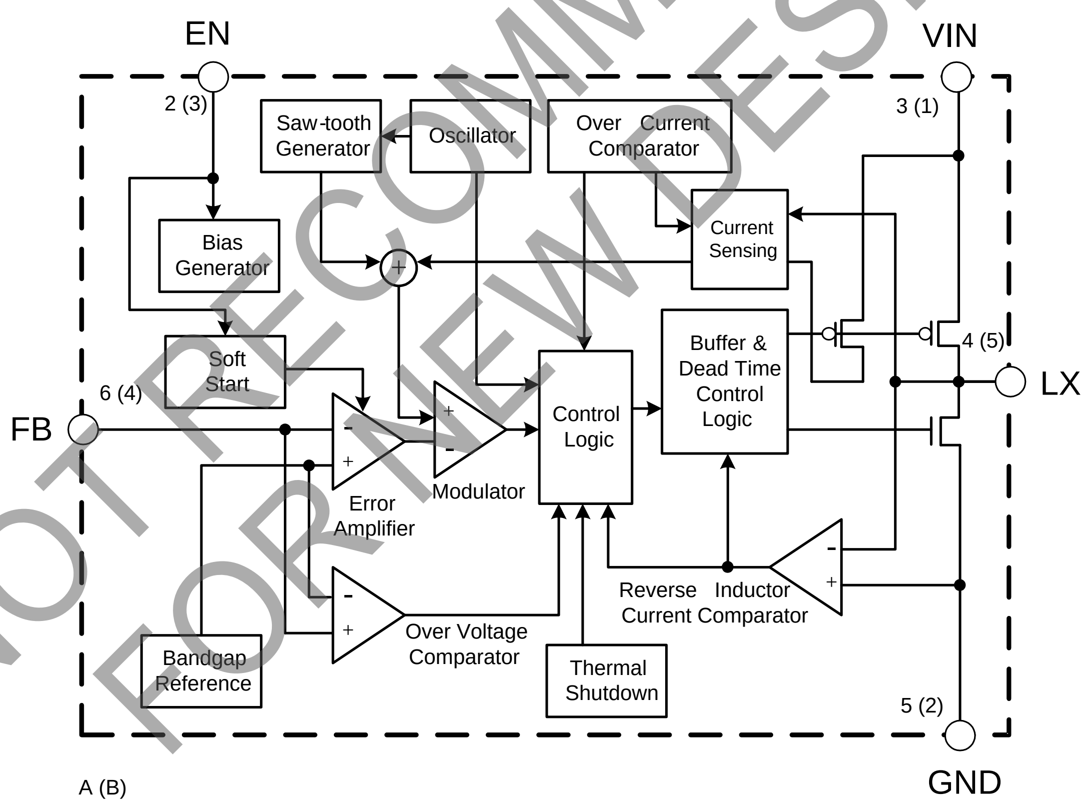
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C1 (pF)	L1 (μH)
3.3	453	100	13	2.2
2.5	320	100	18	2.2
1.8	200	100	30	2.2
1.2	100	100	56	2.2
1.0	68	100	82	2.2

Table 1. Component Guide

Pin Descriptions

Pin Number		Pin Name	Function
WDFN-2×2-6	TSOT-23-5		
1	—	NC	No internal connection (Floating or connected to GND)
2	3	EN	Enable signal input, active high
3	1	VIN	Power supply input
4	5	LX	Connect to inductor
5	2	GND	This pin is the GND reference for the NMOS power stage. It must be connected to the system ground
6	4	FB	Feedback voltage from the output of the power supply

Functional Block Diagram



A (B)
A for WDFN-2×2-6
B for TSOT-23-5

Absolute Maximum Ratings (Note 2)

Symbol	Parameter	Value	Unit
V_{IN}	Supply Input Voltage	0 to 6.0	V
V_{EN}	Enable Input Voltage	-0.3 to V_{IN}+0.3	V
V_{LX}	Switch Output Voltage (Note 3)	-0.3 to V_{IN}+0.3	V
P_D	Power Dissipation (On PCB, T_A=+25°C)	1.89	W
$θ_{JA}$	Thermal Resistance (Junction to Ambient, Simulation)	53	°C/W
$θ_{JC}$	Thermal Resistance (Junction to Case, Simulation)	0.85	°C/W
T_J	Operating Junction Temperature	+160	°C
T_{OP}	Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
V_{HBM}	ESD (Human Body Model)	2000	V
V_{MM}	ESD (Machine Model)	200	V

Note 2: Stresses greater than those listed under "*Absolute Maximum Ratings*" can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "*Recommended Operating Conditions*" is not implied. Exposure to "*Absolute Maximum Ratings*" for extended periods can affect device reliability.

3: If the switching spike duration is less than 100ns, the absolute maximum range of VLX should be -4.5V to 7.5V.

Recommended Operating Conditions

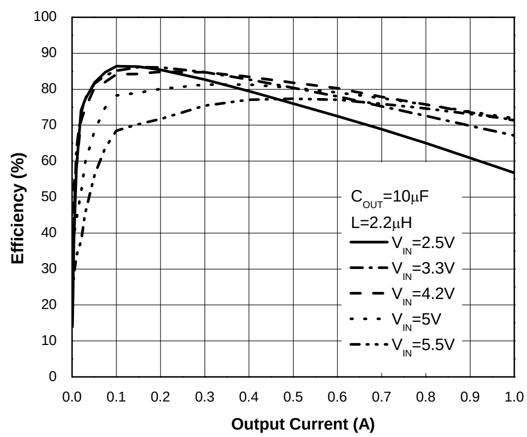
Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Input Voltage	2.5	5.5	V
T_J	Junction Temperature Range	-20	+125	°C
T_A	Ambient Temperature Range	-40	+80	°C

Electrical Characteristics (V_{IN}=V_{EN}=5V, V_{FB}=0.6V, L=2.2µH, C_{IN}= 4.7µF, C_{OUT}=10µF, T_A=+25°C, unless otherwise specified.)

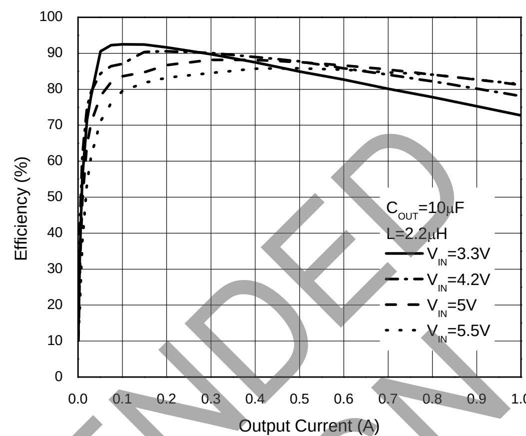
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	—	2.5	—	5.5	V
I_{OFF}	Shutdown Current	V_{EN}=0V	—	0.1	1	µA
V_{FB}	Regulated Feedback Voltage	For Adjustable Output Voltage	0.585	0.6	0.615	V
$\Delta V_{OUT}/V_{OUT}$	Regulated Output Voltage Accuracy	V_{IN}=2.5V to 5.5V, I_{OUT}=0 to 1A	-3	—	3	%
I_{PK}	Peak Inductor Current	V_{FB}=0.5V	—	1.5	—	A
f_{OSC}	Oscillator Frequency	—	1.2	1.5	1.8	MHz
$R_{ON(P)}$	PMOSFET R_{ON}	I_{OUT} =200mA	—	0.25	—	Ω
$R_{ON(N)}$	NMOSFET R_{ON}	I_{OUT} =200mA	—	0.27	—	Ω
I_Q	Quiescent Current	I_{OUT}=0A, V_{FB}=0.7V	—	100	—	µA
I_{LX}	LX Leakage Current	V_{EN}=0V, V_{LX}=0V or 5V	—	0.01	0.1	µA
I_{FB}	Feedback Current	—	—	—	30	nA
I_{EN}	EN Leakage Current	—	—	0.01	0.1	µA
V_{EN_H}	EN High-Level Input Voltage	V_{IN}=2.5V to 5.5V	1.5	—	—	V
V_{EN_L}	EN Low-Level Input Voltage	V_{IN}=2.5V to 5.5V	—	—	0.6	V
V_{UVLO}	Under Voltage Lock Out	Rising	—	1.8	—	V
—	Hysteresis	—	—	0.1	—	V
T_{SD}	Thermal Shutdown	—	—	+160	—	°C

Performance Characteristics

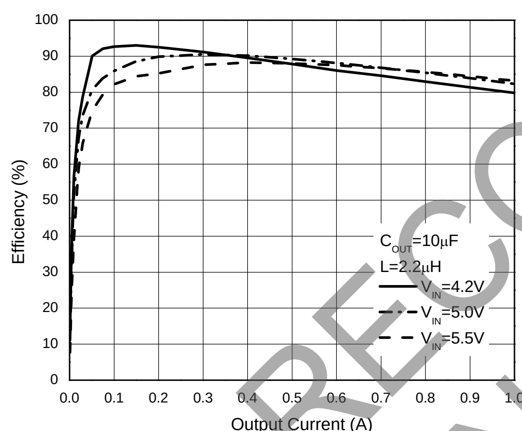
Efficiency vs. Output Current (V_{OUT}=1.2V)



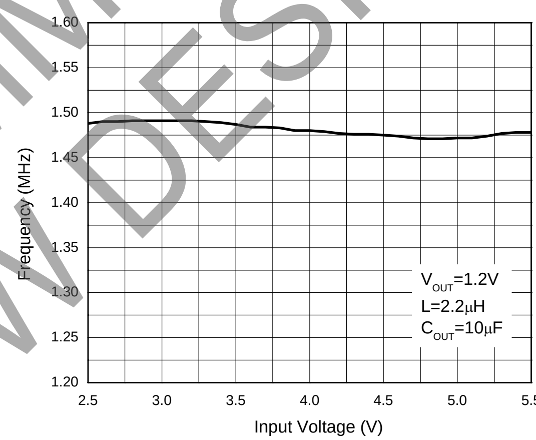
Efficiency vs. Output Current (V_{OUT}=2.5V)



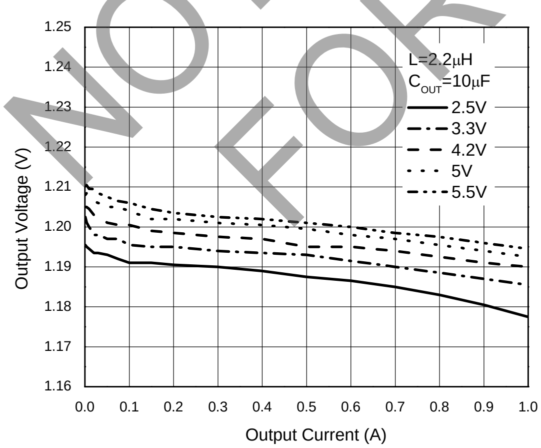
Efficiency vs. Output Current (V_{OUT}=3.3V)



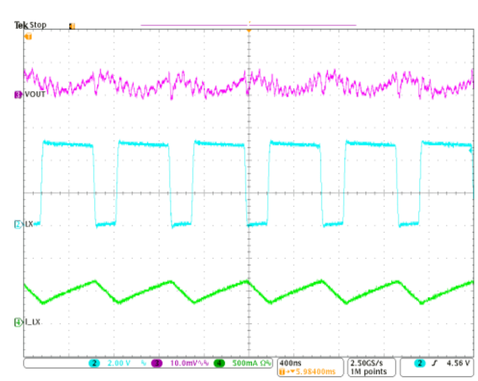
Frequency vs. Input Voltage



Output Voltage vs. Output Current (V_{OUT}=1.2±0.03V)



Output Ripple (V_{IN}=5.0V, V_{OUT}=3.3V, I_{OUT}=1A)



Performance Characteristics (continued)

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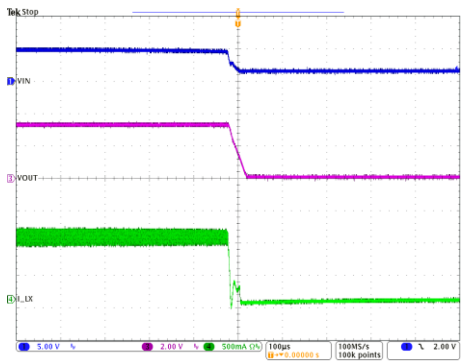
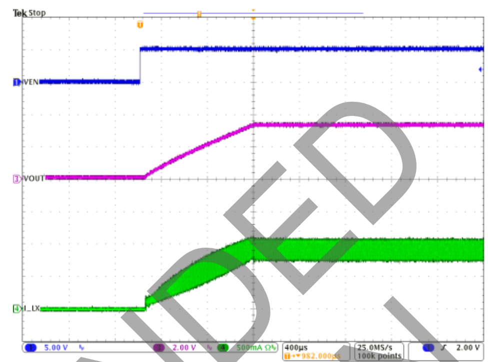
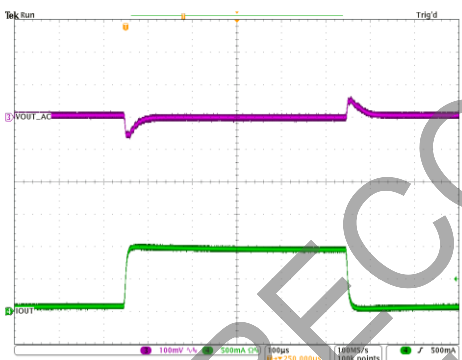
Power Off through VIN
(V_{IN}=V_{EN}=5.0 to 0V, V_{OUT}=3.3V, I_{OUT}=1A)



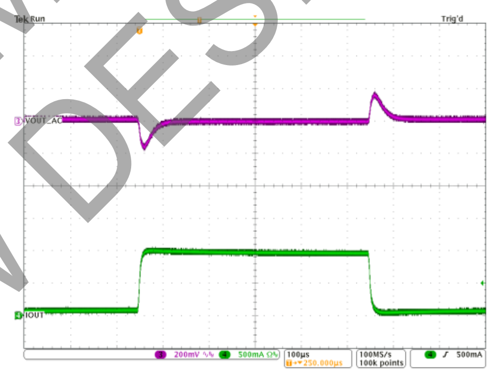
Soft Start (Power Up through EN)
(V_{IN}=5.0V, V_{OUT}=3.3V, I_{OUT}=1A, V_{EN}=0 to 5.0V)



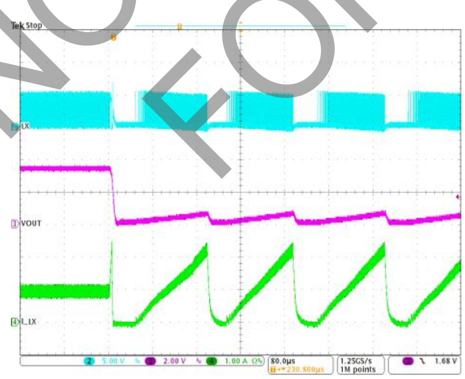
Load Transient
(V_{IN}=5.0V, V_{OUT}=1.2V, I_{OUT}=0.1 to 1A)



Load Transient
(V_{IN}=5.0V, V_{OUT}=3.3V, I_{OUT}=0.1 to 1A)



Short Circuit
(V_{IN}=5.0V, V_{OUT}=3.3V Short to GND, I_{OUT}=1A)



Application Information

The basic AUR9705 application circuit is shown in Typical Applications Circuit, external components selection is determined by the load current and is critical with the selection of inductor and capacitor values.

1. Inductor Selection

For most applications, the value of inductor is chosen based on the required ripple current with the range of 2.2µH to 4.7µH.

$$\Delta I_L = \frac{1}{f \times L} V_{OUT} (1 - \frac{V_{OUT}}{V_{IN}})$$

The largest ripple current occurs at the highest input voltage. Having a small ripple current reduces the ESR loss in the output capacitor and improves the efficiency. The highest efficiency is realized at low operating frequency with small ripple current. However, larger value inductors will be required. A reasonable starting point for ripple current setting is $\Delta I_L = 40\% I_{MAX}$. For a maximum ripple current stays below a specified value, the inductor should be chosen according to the following equation:

$$L = [\frac{V_{OUT}}{f \times \Delta I_L (MAX)}][1 - \frac{V_{OUT}}{V_{IN}(MAX)}]$$

The DC current rating of the inductor should be at least equal to the maximum output current plus half the highest ripple current to prevent inductor core saturation. For better efficiency, a lower DC-resistance inductor should be selected.

2. Capacitor Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} = I_{OMAX} \times \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{\frac{1}{2}}}{V_{IN}}$$

It indicates a maximum value at $V_{IN}=2V_{OUT}$, where $I_{RMS}=I_{OUT}/2$. This simple worse-case condition is commonly used for design because even significant deviations do not much relieve. The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize output voltage ripple and load step transients, as well as the amount of bulk capacitor that is necessary to ensure that the control loop is stable. Loop stability can be also checked by viewing the load step transient response as described in the following section. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \le \Delta I_L [ESR + \frac{1}{8 \times f \times C_{OUT}}]$$

The output ripple is the highest at the maximum input voltage since ΔI_L increases with input voltage.

3. Load Transient

A switching regulator typically takes several cycles to respond to the load current step. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \times ESR$, where ESR is the effective series resistance of output capacitor. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During the recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

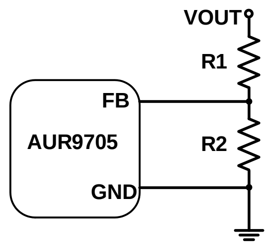
4. Output Voltage Setting

The output voltage of AUR9705 can be adjusted by a resistive divider according to the following formula:

$$V_{OUT} = V_{FB} \times (1 + \frac{R_1}{R_2}) = 0.6V \times (1 + \frac{R_1}{R_2})$$

The resistive divider senses the fraction of the output voltage as shown in Figure of Setting the Output Voltage.

Application Information (continued)



Setting the Output Voltage

5. Efficiency Considerations

The efficiency of switching regulator is equal to the output power divided by the input power times 100%. It is usually useful to analyze the individual losses to determine what is limiting efficiency and which change could produce the largest improvement. Efficiency can be expressed as:

Efficiency=100%-L1-L2-…..

Where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the regulator produce losses, two major sources usually account for most of the power losses: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very light load currents and the I^2R loss dominates the efficiency loss at medium to heavy load current.

5.1 The V_{IN} quiescent current loss comprises two parts: the DC bias current as given in the electrical characteristics and the internal MOSFET switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each cycle the gate is switched from high to low, then to high again, and the packet of charge, dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the internal DC bias current. In continuous mode,

$$I_{GATE} = f \times (Q_P + Q_N)$$

Where Q_P and Q_N are the gate charge of power PMOSFET and NMOSFET switches. Both the DC bias current and gate charge losses are proportional to the V_{IN} and this effect will be more serious at higher input voltages.

5.2 I^2R losses are calculated from internal switch resistance, R_{SW} and external inductor resistance R_L. In continuous mode, the average output current flowing through the inductor is chopped between power PMOSFET switch and NMOSFET switch. Then, the series resistance looking into the LX pin is a function of both PMOSFET $R_{DS(ON)}$ and NMOSFET

$R_{DS(ON)}$ resistance and the duty cycle (D):

$$R_{SW} = R_{DS(ON)P} \times D + R_{DS(ON)N} \times (1 - D)$$

Therefore, to obtain the I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2 % of total additional loss.

6. Thermal Characteristics

In most applications, the part does not dissipate much heat due to its high efficiency. However, in some conditions when the part is operating in high ambient temperature with high $R_{DS(ON)}$ resistance and high duty cycles, such as in LDO mode, the heat dissipated may exceed the maximum junction temperature. To avoid the part from exceeding maximum junction temperature, the user should do some thermal analysis. The maximum power dissipation depends on the layout of PCB, the thermal resistance of IC package, the rate of surrounding airflow and the temperature difference between junction and ambient.

Ordering Information

AUR9705 XX XX - XX

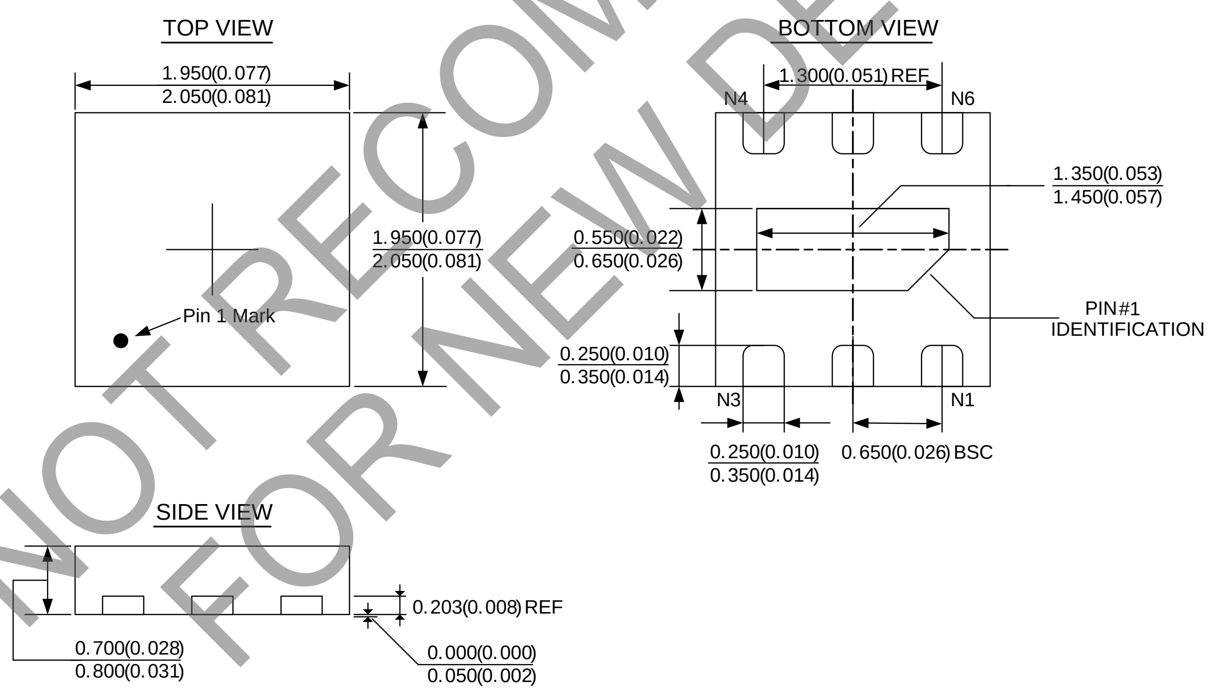
Product Name	Packing	RoHS/Green	Package
	A: Adjustable Output	G1 : RoHS Compliant and Green	D : WDFN-2x2-6 H : TSOT-23-5

Package	Temperature Range	Part Number	Marking ID	Packing
WDFN-2×2-6	-40 to +80°C	AUR9705AGD	705	Tape & Reel
TSOT-23-5		AUR9705AGH	9705AG	Tape & Reel

Package Outline Dimensions (All dimensions in mm (inch).)

Please see http://www.diodes.com/package-outlines.html for the latest version.

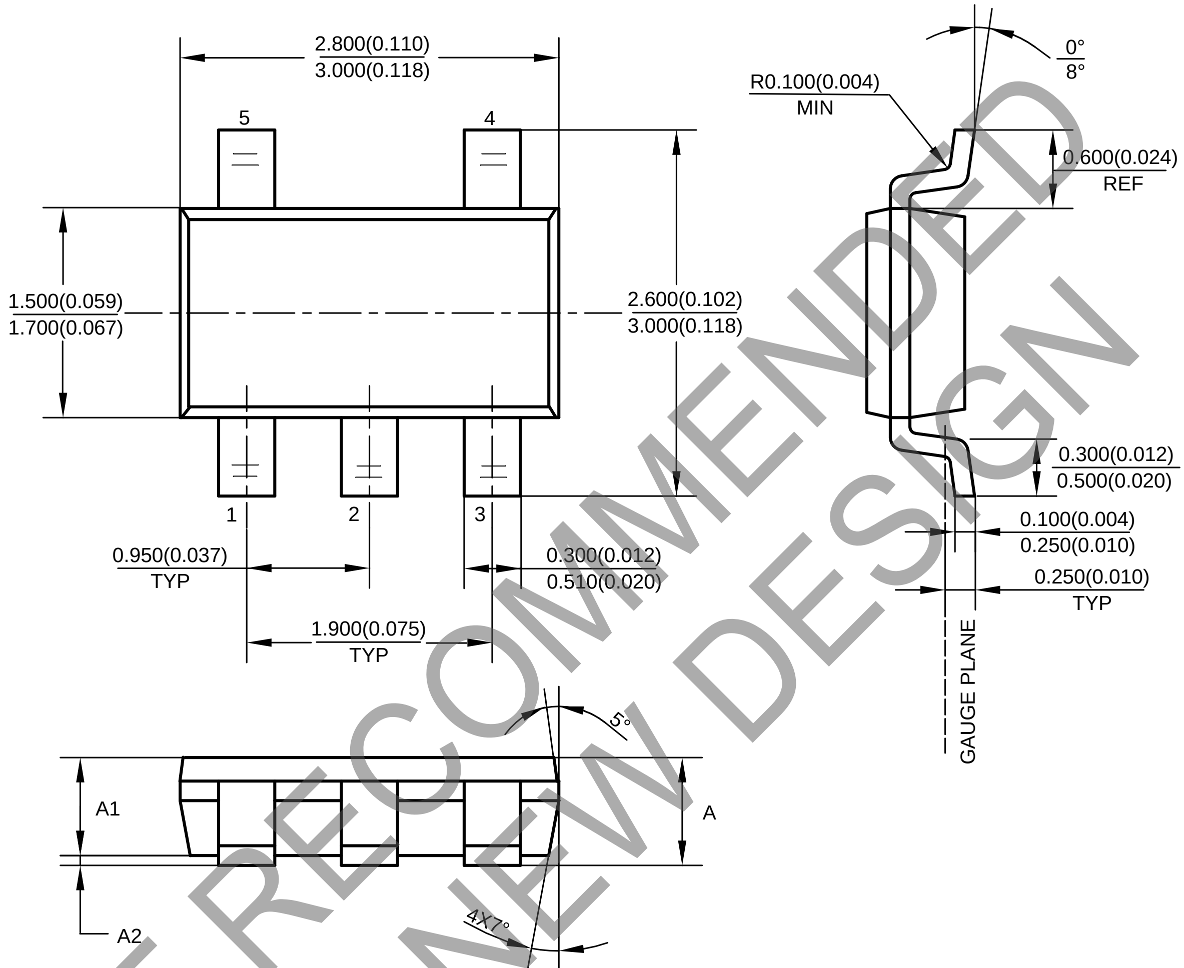
(1) Package Type: WDFN-2×2-6



Package Outline Dimensions (continued) (All dimensions in mm(inch).)

Please see http://www.diodes.com/package-outlines.html for the latest version.

(2) Package Type: TSOT-23-5

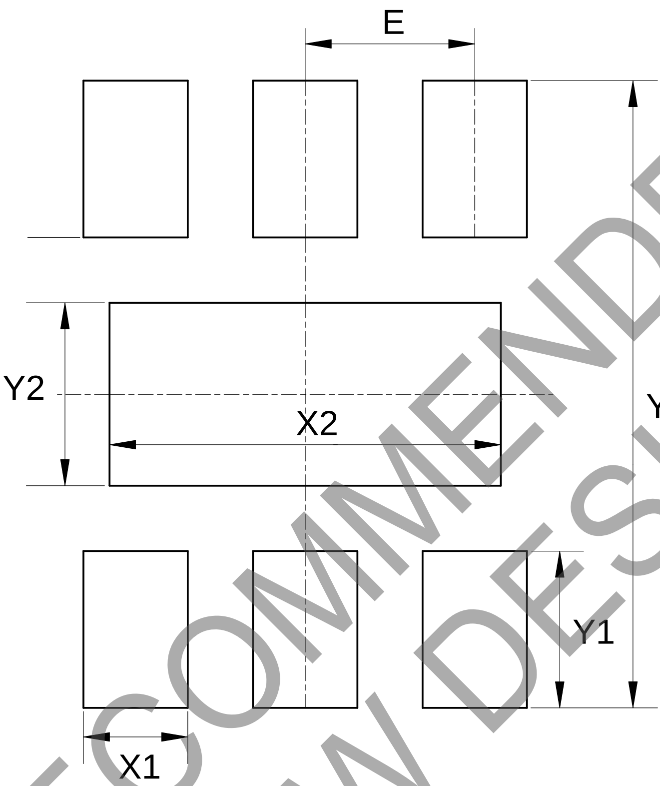


Symbol	A				A1				A2			
	min(mm)	max(mm)	min(inch)	max(inch)	min(mm)	max(mm)	min(inch)	max(inch)	min(mm)	max(mm)	min(inch)	max(inch)
Option1	0.700	0.900	0.028	0.035	0.700	0.800	0.028	0.031	0.000	0.100	0.000	0.004
Option2	-	1.000	-	0.039	0.840	0.900	0.033	0.035	0.010	0.100	0.000	0.004

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) Package Type: WDFN-2×2-6

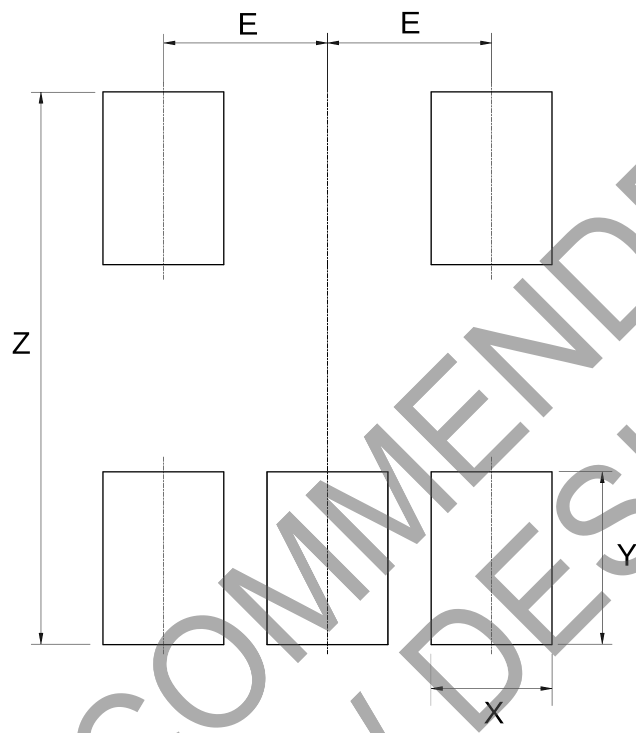


Dimensions	Y (mm)/(inch)	X1 (mm)/(inch)	Y1 (mm)/(inch)	X2 (mm)/(inch)	Y2 (mm)/(inch)	E (mm)/(inch)
Value	2.400/0.094	0.400/0.016	0.600/0.024	1.500/0.059	0.700/0.028	0.650/0.026

Suggested Pad Layout (continued)

Please see http://www.diodes.com/package-outlines.html for the latest version.

(2) Package Type: TSOT-23-5



Dimensions	E (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	Z (mm)/(inch)
Value	0.950/0.037	0.700/0.028	1.000/0.039	3.199/0.126

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