8 CHANNEL LOW CAPACITANCE TVS DIODE ARRAY

Product Summary

$V_{BR\ (Min)}$	$I_{PP\ (Max)}$	$C_{I/O\ (Typ)}$
5.5V	5	0.55pF

Description

The D3V3F8U9LP3810 is a high-performance device suitable for protecting four high speed I/Os. These devices are assembled in U-DFN3810-9 (Type B) package and have high ESD surge capability, low ESD clamping voltage and ultra-low capacitance.

Applications

Typically used at high-speed ports such as USB 3.0, USB 3.1, Serial ATA, Display port.

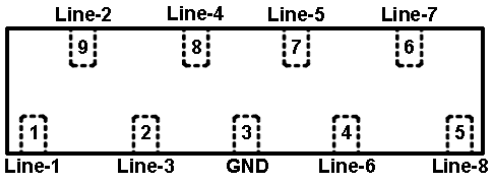
Features

- Clamping Voltage: 5V at 16A TLP
- IEC 61000-4-2 (ESD): Air — ±12kV, Contact — ±12kV
- IEC 61000-4-5 (Lightning): 5A (8/20μs)
- 8 Channels of ESD Protection
- Ultra-Low Channel Input Capacitance of 0.55pF Typical
- TLP Dynamic Resistance: 0.25Ω
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

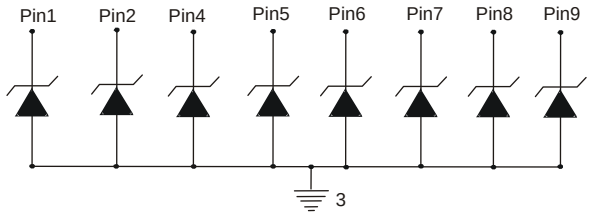
Mechanical Data

- Case: U-DFN3810-9 (Type B)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Schematic
- Terminals: Finish – NiPdAu, Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.005 grams (Approximate)

U-DFN3810-9 (Type B)



Pin Description (Top View)



Device Schematic

Ordering Information (Note 4)

Part Number	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity
D3V3F8U9LP3810-7	Standard	MW5	7	8	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

U-DFN3810-9 (Type B)

MW5 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: E = 2017)
M = Month (ex: 9 = September)

Date Code Key

Year	2016	2017	2018	2019	2020	2021
Code	D	E	F	G	H	I

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Conditions
Peak Pulse Current, per IEC 61000-4-5	I_{PP}	5	A	I/O to V_{SS}, 8/20µs
Peak Pulse Power, per IEC 61000-4-5	P_{PP}	32	W	I/O to V_{SS}, 8/20µs
ESD Protection – Contact Discharge, per IEC 61000-4-2	$V_{ESD\_CONTACT}$	±12	kV	I/O to V_{SS}
ESD Protection – Air Discharge, per IEC 61000-4-2	V_{ESD_AIR}	±12	kV	I/O to V_{SS}
Operating Temperature	T_{OP}	-55 to +85	°C	—
Storage Temperature	T_{STG}	-55 to +150	°C	—

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 5)	P_D	350	mW
Thermal Resistance, Junction to Ambient Typical (Note 5)	$R_{\theta JA}$	360	°C/W

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Reverse Working Voltage	V_{RWM}	—	—	3.3	V	I_R=1mA, I/O to V_{SS}
Reverse Current	I_R	—	—	1.0	µA	V_R = 3.3V, I/O to V_{SS}
Reverse Breakdown Voltage	V_{BR}	5.5	7.0	—	V	I_R = 1mA, I/O to V_{SS}
Forward Clamping Voltage	V_F	-1.0	-0.85	—	V	I_F = -15mA, I/O to V_{SS}
Holding Reverse Voltage	V_{HOLD}	—	1.19	—	V	I/O to V_{SS}
Holding Reverse Current	I_{HOLD}	—	90	—	mA	I/O to V_{SS}
Clamping Voltage (Note 6)	V_C	—	5	—	V	TLP, 16A, tp = 100ns, I/O to V_{SS}
Clamping Voltage (Note 6)	V_C	—	5	—	V	TLP, -16A, tp = 100ns, I/O to V_{SS}
Dynamic Reverse Resistance	R_{DIF-R}	—	0.25	—	Ω	TLP, 10A, tp = 100ns, I/O to V_{SS}
Dynamic Forward Resistance	R_{DIF-F}	—	0.2	—	Ω	TLP, 10A, tp = 100ns, V_{SS} to I/O
Channel Input Capacitance	$C_{I/O}$	—	0.55	—	pF	$V_{I/O}$ = 0V, V_{SS} = 0V, f = 1MHz

Notes: 5. Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes Incorporated's suggested pad layout, which can be found on our website at http://www.diodes.com/package-outlines.html.

6. Clamping voltage value is based on a TLP model. TLP conditions: Z_0=50Ω, tp = 100ns, averaging window; t1=70ns to t2=90ns.

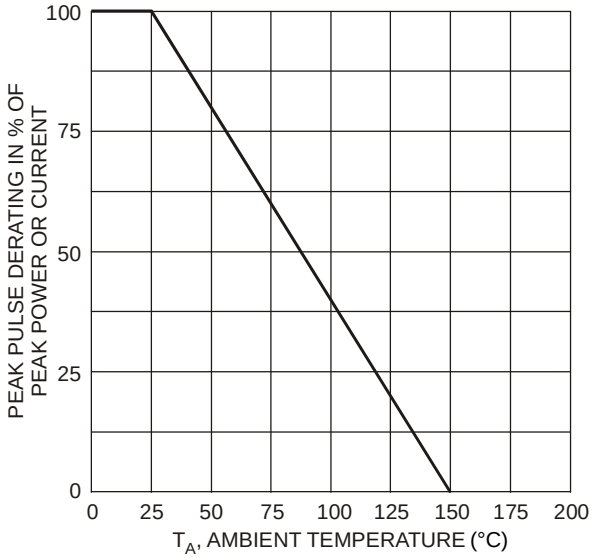


Figure 1 Pulse Derating Curve

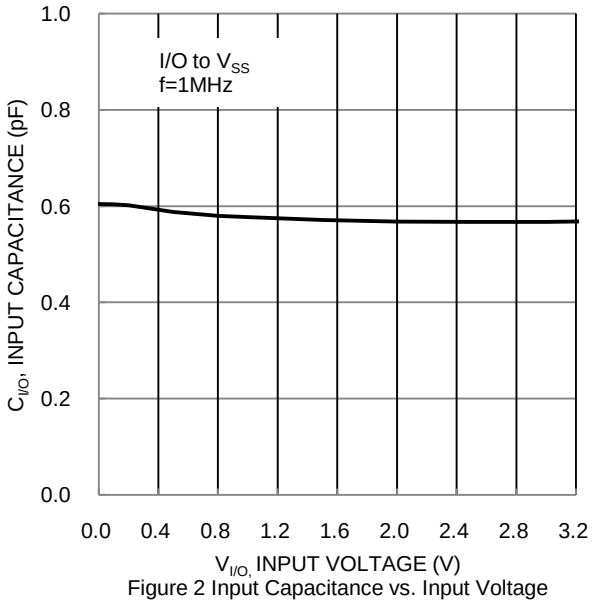


Figure 2 Input Capacitance vs. Input Voltage

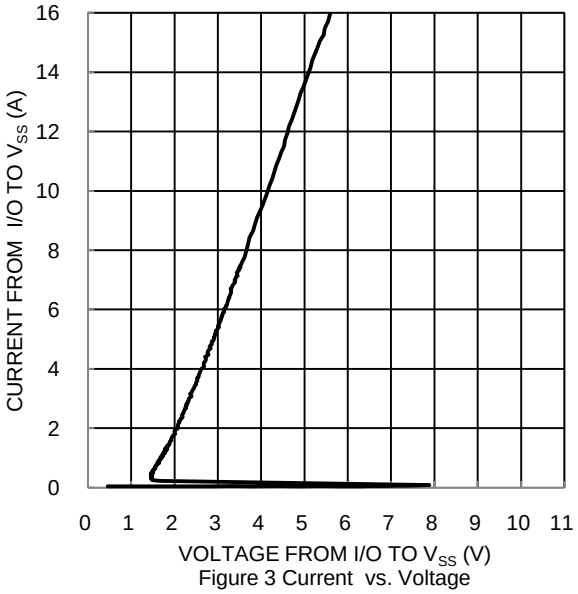
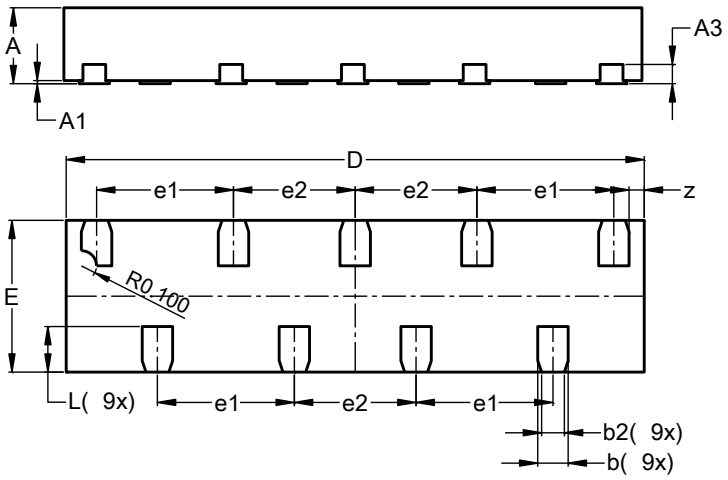


Figure 3 Current vs. Voltage

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN3810-9 (Type B)

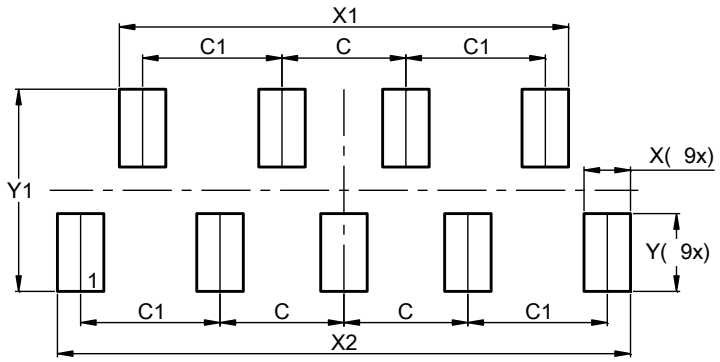


U-DFN3810-9 (Type B)			
Dim	**Min**	**Max**	**Typ**
A	0.45	0.55	0.50
A1	0.00	0.05	0.02
A3	—	—	0.127
b	0.15	0.25	0.20
b2	0.10	0.20	0.15
D	3.75	3.85	3.80
E	0.95	1.05	1.00
e1	—	—	0.90
e2	—	—	0.80
L	0.25	0.35	0.30
z	—	—	0.10
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN3810-9 (Type B)



Dimensions	Value (in mm)
C	0.800
C1	0.900
X	0.300
X1	2.900
X2	3.700
Y	0.500
Y1	1.300

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