

**HIGH FREQUENCY HALF-BRIDGE GATE DRIVER
WITH PROGRAMMABLE DEADTIME
IN W-DFN3030-10 (Type TH)**

Description

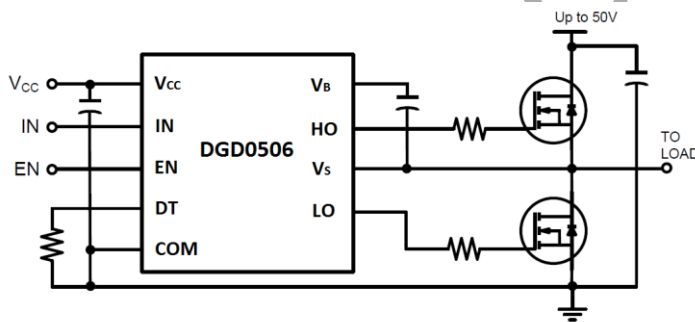
The DGD0506 is a high-frequency half-bridge gate driver capable of driving N-channel MOSFETs in a half-bridge configuration. The floating high-side driver is rated up to 50V.

The DGD0506 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with MCUs. UVLO for high-side and low-side will protect a MOSFET with loss of supply. To protect MOSFETs, cross conduction prevention logic prevents the HO and LO outputs being on at the same time.

Fast and well-matched propagation delays allow a higher switching frequency, enabling a smaller, more compact power switching design using smaller associated components. The DGD0506 is offered in the W-DFN3030-10 (Type TH) package and operates over an extended -40°C to +125°C temperature range.

Applications

- DC-DC Converters
- Motor Controls
- Battery Powered Hand Tools
- eCig Devices
- Class D Power Amplifiers



Typical Configuration

Features

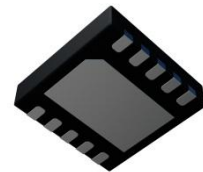
- 50V Floating High-Side Driver
- Drives Two N-Channel MOSFETs in a Half-Bridge Configuration
- 1.25A Source / 2.0A Sink Output Current Capability
- Internal Bootstrap Schottky Diode Included
- Undervoltage Lockout for High-Side and Low-Side Drivers
- Programmable Deadtime to Protect MOSFETs
- Logic Input (IN and EN) 3.3V Capability
- Ultra Low Standby Currents (<1µA)
- Extended Temperature Range: -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

- Case: W-DFN3030-10 (Type TH)
- Case material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Finish Solderable per MIL-STD-202, Method 208 (E3)
- Weight: 0.017 grams (Approximate)



Top View



Bottom View

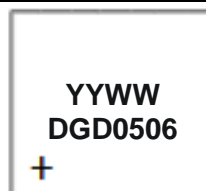
W-DFN3030-10 (Type TH)

Ordering Information (Note 4)

Product	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DGD0506FN-7	DGD0506	7	8	3,000

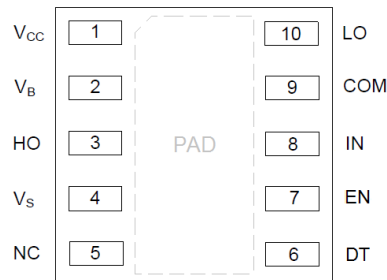
- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



DGD0506 = Product Type Marking Code
YY = Year (ex: 17 = 2017)
WW = Week (01 to 53)

Pin Diagrams

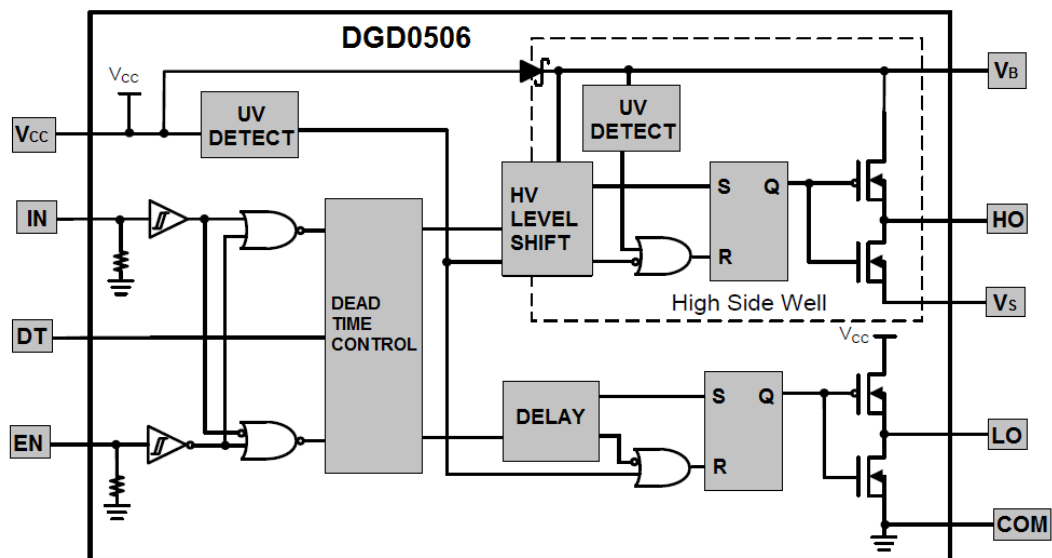


Top View: W-DFN3030-10 (Type TH)

Pin Descriptions

Pin Number	Pin Name	Function
1	V _{CC}	Low-Side and Logic Supply
2	V _B	High-Side Floating Supply
3	HO	High-Side Gate Drive Output
4	V _S	High-Side Floating Supply Return
5	NC	No Connect (No Internal Connection)
6	DT	Deadtime Control
7	EN	Logic Input Enable, a Logic Low turns off Gate Driver
8	IN	Logic Input for High-Side and Low-Side Gate Driver Outputs (HO and LO), in Phase with HO
9	COM	Low-Side and Logic Return
10	LO	Low-Side Gate Drive Output
PAD	Substrate	Connect to COM on PCB

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Positive Supply Voltage	V _B	-0.3 to +50	V
High-Side Floating Negative Supply Voltage	V _S	V _B -14 to V _B +0.3	V
High-Side Floating Output Voltage	V _{HO}	V _S -0.3 to V _B +0.3	V
Offset Supply Voltage Transient	dV _S / dt	50	V/ns
Logic and Low-Side Fixed Supply Voltage	V _{CC}	-0.3 to +15	V
Low-Side Output Voltage	V _{LO}	-0.3 to V _{CC} +0.3	V
Logic Input Voltage (IN and EN)	V _{IN}	-0.3 to +15	V
Bootstrap Diode Current (Pulsed <10μs)	I _{BD}	500	mA

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 5)	P _D	0.4	W
Thermal Resistance, Junction to Ambient (Note 5)	R _{θJA}	64	°C/W
Thermal Resistance, Junction to Case (Note 5)	R _{θJC}	42	°C/W
Operating Temperature	T _J	+150	°C
Lead Temperature (Soldering, 10s)	T _L	+300	
Storage Temperature Range	T _{STG}	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High-Side Floating Supply	V _B	V _S + 8	V _S + 14	V
High-Side Floating Supply Offset Voltage	V _S	(Note 6)	50 (Note 7)	V
High-Side Floating Output Voltage	V _{HO}	V _S	V _B	V
Logic and Low Side Fixed Supply Voltage	V _{CC}	8	14	V
Low-Side Output Voltage	V _{LO}	0	V _{CC}	V
Logic Input Voltage (IN and EN)	V _{IN}	0	5	V
Bootstrap Diode Current (Pulsed <10μs)	I _{BD}	-	400	mA
Ambient Temperature	T _A	-40	+125	°C

Notes: 6. Logic operation for V_S of -5V to +50V. Logic state held for V_S of -5V to -V_Bs.
7. Provided V_B doesn't exceed absolute maximum rating of 50V.

DC Electrical Characteristics ($V_{CC} = V_{BS} = 12V$, $COM = V_S = 0V$, @ $T_A = +25^\circ C$, unless otherwise specified.) (Note 8)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Logic "1" Input Voltage	V_{IH}	2.4	–	–	V	–
Logic "0" Input Voltage	V_{IL}	–	–	0.8	V	–
Enable Logic "1" Input Voltage	V_{ENIH}	1.5	–	–	V	–
Enable Logic "0" Input Voltage	V_{ENIL}	–	–	0.7	V	–
Input Voltage Hysteresis	V_{INHYS}	–	0.6	–	V	–
High Level Output Voltage, $V_{BIAS} - V_O$	V_{OH}	–	0.45	0.6	V	$I_{O+} = 100mA$
Low Level Output Voltage, V_O	V_{OL}	–	0.15	0.22	V	$I_{O-} = 100mA$
Offset Supply Leakage Current	I_{LK}	–	10	50	μA	$V_B = V_S = 50V$
V_{CC} Shutdown Supply Current	I_{CCSD}	–	0	1	μA	$V_{IN} = 0V$ or $5V$, $V_{EN} = 0V$
V_{CC} Quiescent Supply Current	I_{CCQ}	–	0.32	0.5	mA	$V_{IN} = 0V$ or $5V$, $R_{DT} = 100k\Omega$
V_{CC} Operating Supply Current	I_{CCOP}	–	2.1	–	mA	$f_s = 500kHz$
V_{BS} Quiescent Supply Current	I_{BSQ}	–	62	100	μA	$V_{IN} = 0V$ or $5V$
V_{BS} Operating Supply Current	I_{BSOP}	–	1.1	–	mA	$f_s = 500kHz$
Logic "1" Input Bias Current	I_{IN+}	–	25	60	μA	$V_{IN} = 5V$
Logic "0" Input Bias Current	I_{IN-}	–	0	1	μA	$V_{IN} = 0V$
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	5.9	6.9	7.9	V	–
V_{BS} Supply Undervoltage Negative Going Threshold	V_{BSUV-}	5.6	6.6	7.6	V	–
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	5.9	6.9	7.9	V	–
V_{CC} Supply Undervoltage Negative Going Threshold	V_{CCUV-}	5.6	6.6	7.6	V	–
Output High Short-Circuit Pulsed Current	I_{O+}	0.9	1.25	–	A	$V_O = 0V$, $PW \leq 10\mu s$
Output Low Short-Circuit Pulsed Current	I_{O-}	1.5	2.0	–	A	$V_O = 15V$, $PW \leq 10\mu s$
Forward Voltage of Bootstrap Diode	V_{F1}	–	0.27	–	V	$I_F = 100\mu A$
Forward Voltage of Bootstrap Diode	V_{F2}	–	0.8	–	V	$I_F = 100mA$, $PW \leq 10ms$

Note: 8. The V_{IN} and I_{IN} parameters are applicable to the two logic pins: IN and EN. The V_O and I_O parameters are applicable to the respective output pins: HO and LO.

AC Electrical Characteristics ($V_{CC} = V_{BS} = 12V$, $COM = V_S = 0V$, $C_L = 1000pF$, @ $T_A = +25^\circ C$, unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Turn-on Propagation Delay, HO & LO	t_{ON}	65	96	125	ns	$R_{DT} = 10k\Omega$
		350	463	580	ns	$R_{DT} = 100k\Omega$
Turn-off Propagation Delay, HO & LO	t_{OFF}	–	22	56	ns	–
Turn-on Rise Time	t_R	–	17	35	ns	–
Turn-off Fall Time	t_F	–	12	25	ns	–
Delay Matching	t_{DM}	–	–	50	ns	–
Deadtime: $t_{DT LO-HO}$ & $t_{DT HO-LO}$	t_{DT}	40	70	100	ns	$R_{DT} = 10k\Omega$
		300	430	560	ns	$R_{DT} = 100k\Omega$
Deadtime Matching	t_{MDT}	–	–	50	ns	$R_{DT} = 100k\Omega$

Timing Waveforms

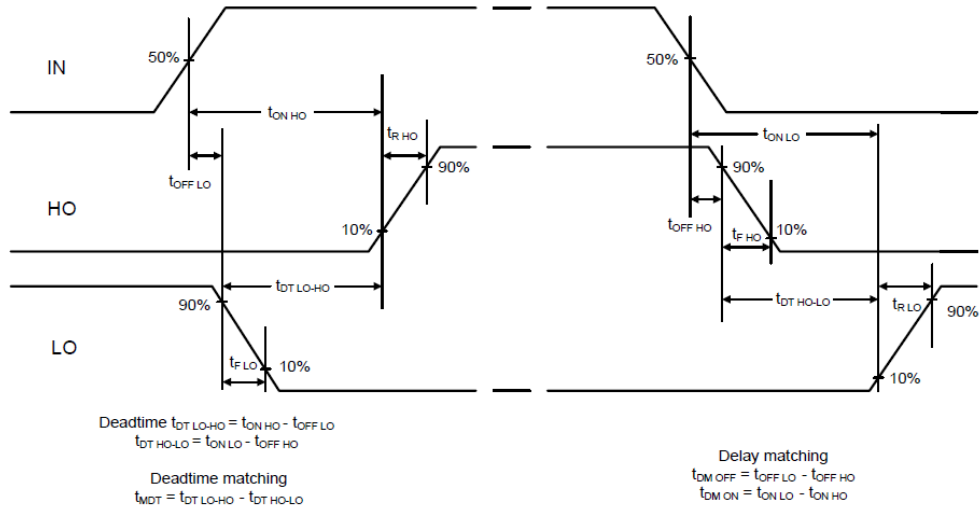


Figure 1. Switching Time Waveform Definitions

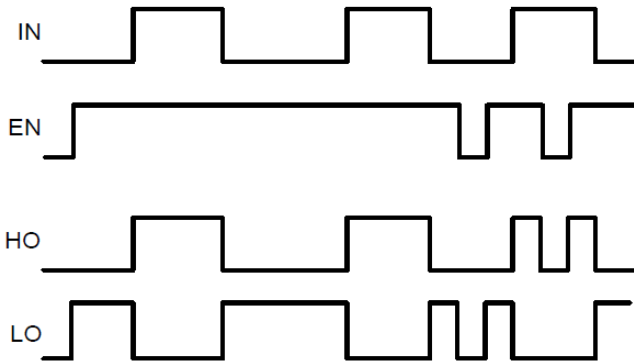


Figure 2. Input / Output Timing Diagram

Typical Performance Characteristics (@T_A = +25°C, unless otherwise specified.)

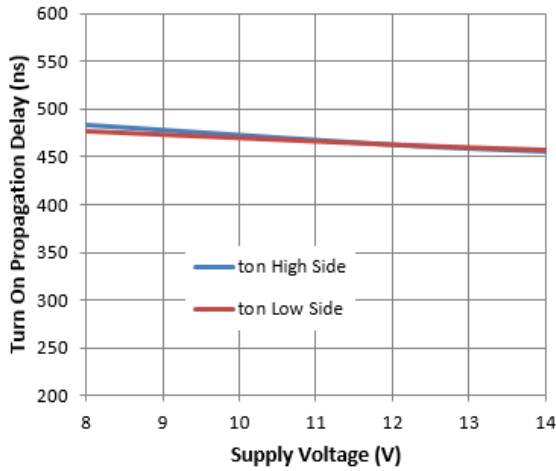


Figure 4. Turn-on Propagation Delay vs. Supply Voltage

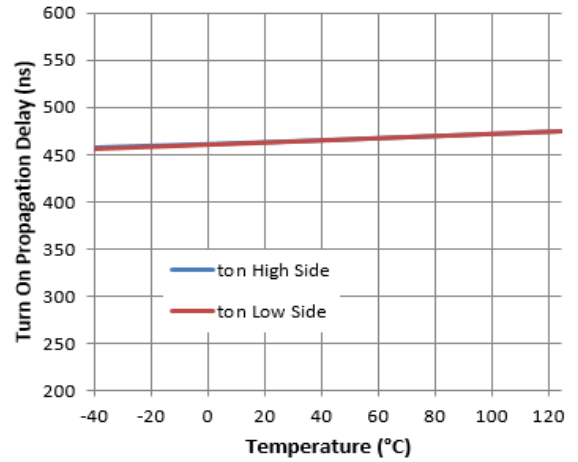


Figure 5. Turn-on Propagation Delay vs. Temperature

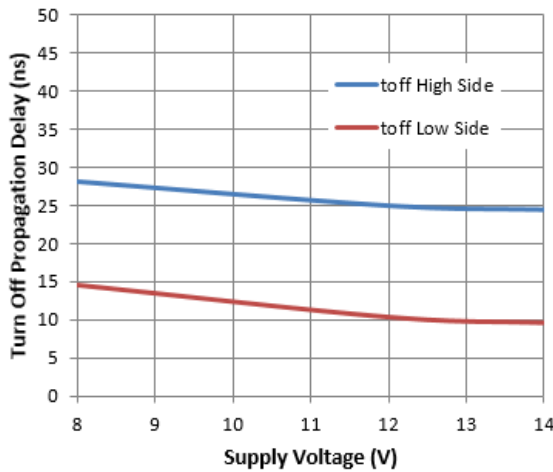


Figure 6. Turn-off Propagation Delay vs. Supply Voltage

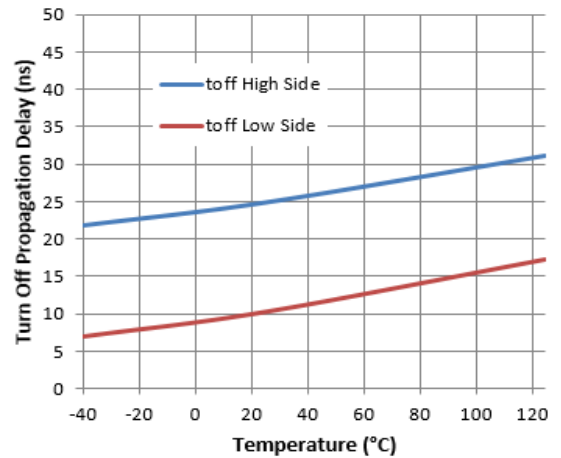


Figure 7. Turn-off Propagation Delay vs. Temperature

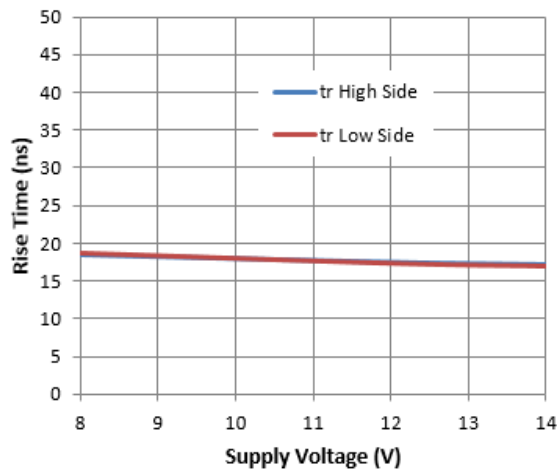


Figure 8. Rise Time vs. Supply Voltage

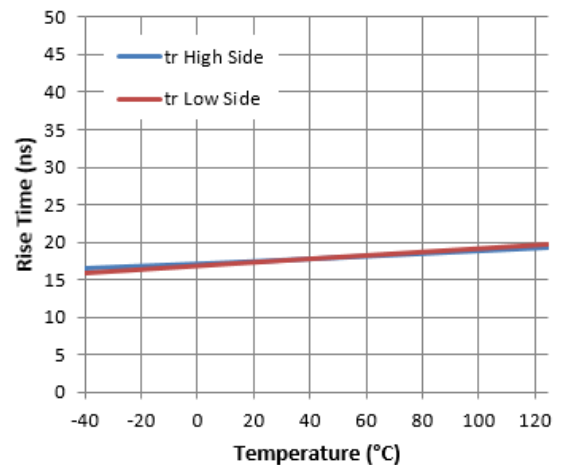


Figure 9. Rise Time vs. Temperature

Typical Performance Characteristics (Cont.)

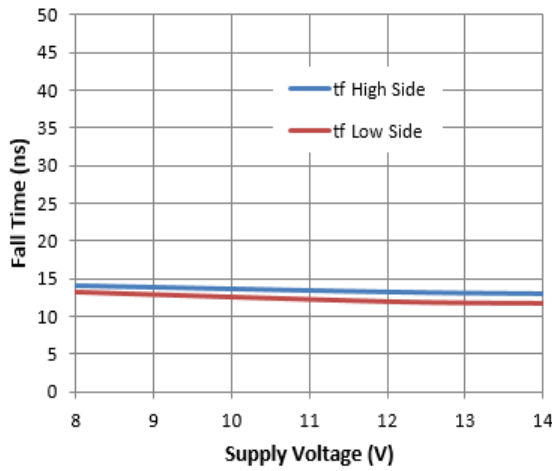


Figure 10. Fall Time vs. Supply Voltage

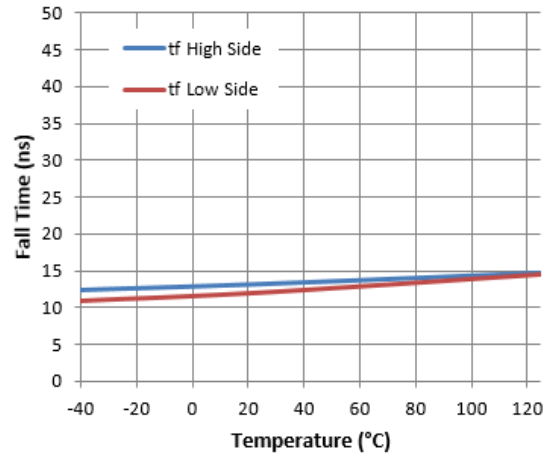


Figure 11. Fall Time vs. Temperature

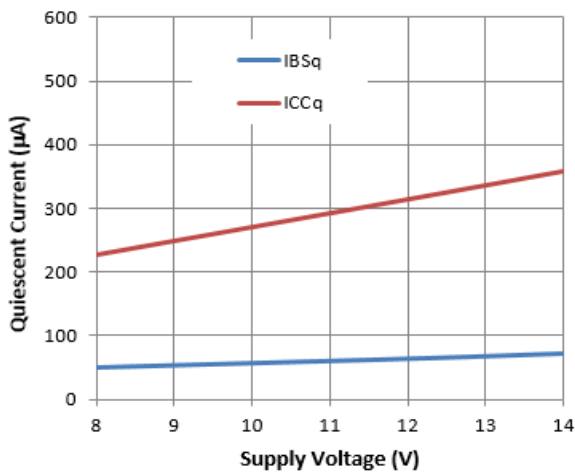


Figure 12. Quiescent Current vs. Supply Voltage

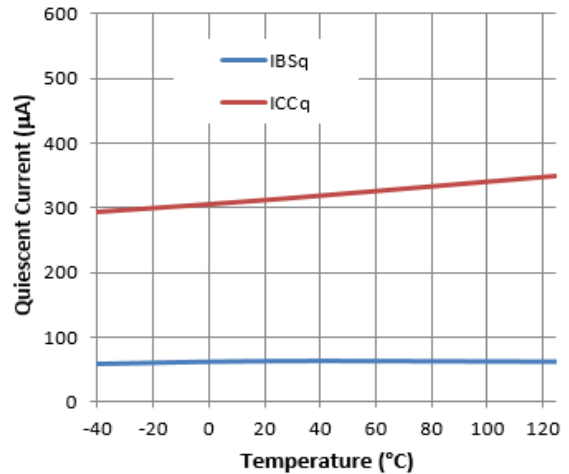


Figure 13. Quiescent Current vs. Temperature

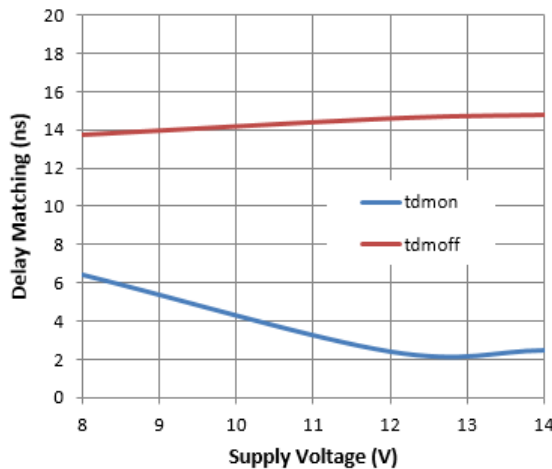


Figure 14. Delay Matching vs. Supply Voltage

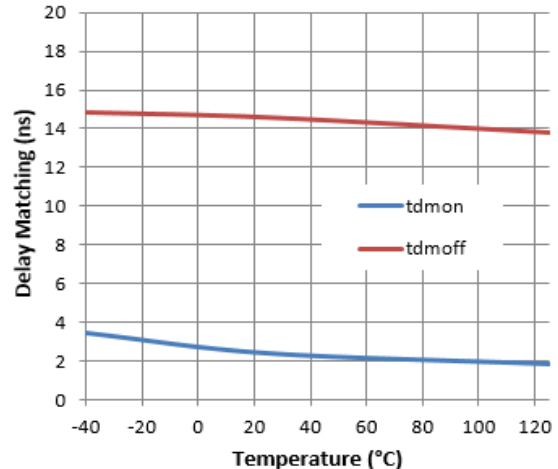


Figure 15. Delay Matching vs. Temperature

Typical Performance Characteristics (Cont.)

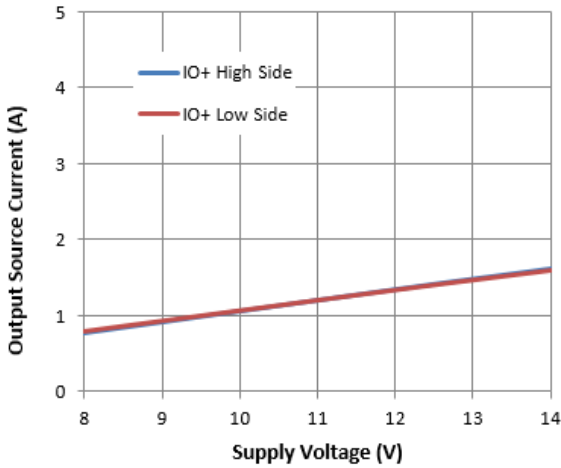


Figure 16. Output Source Current vs. Supply Voltage

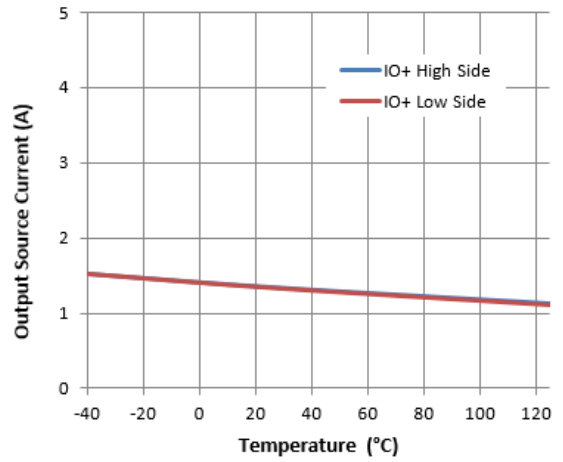


Figure 17. Output Source Current vs. Temperature

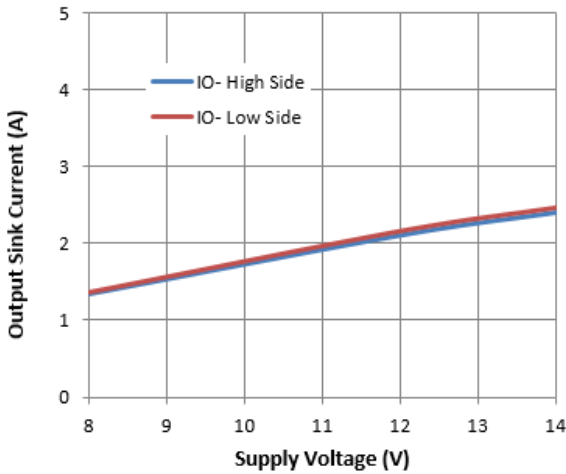


Figure 18. Output Sink Current vs. Supply Voltage

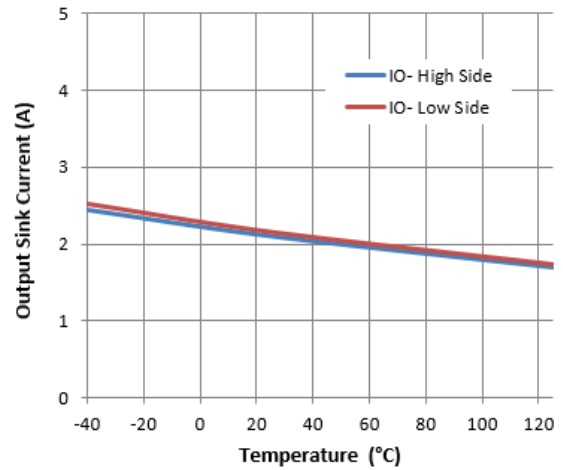


Figure 19. Output Sink Current vs. Temperature

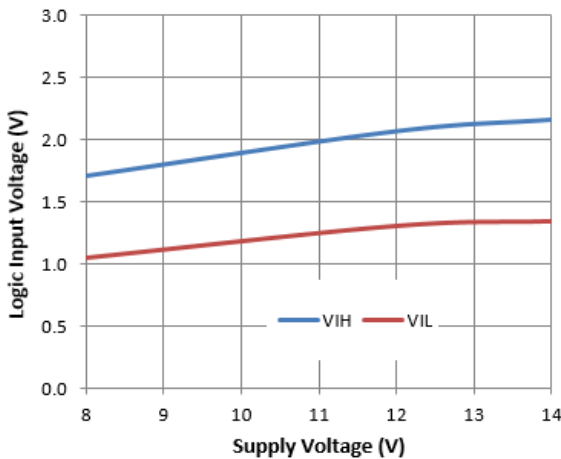


Fig 20. Logic Input Voltage vs. Supply Voltage

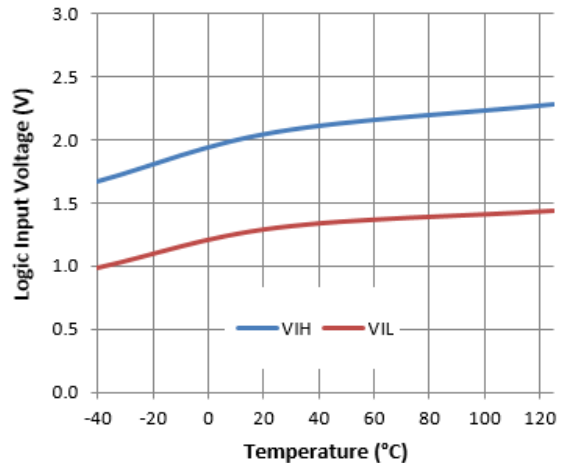


Fig 21. Logic Input Voltage vs. Temperature

Typical Performance Characteristics (Cont.)

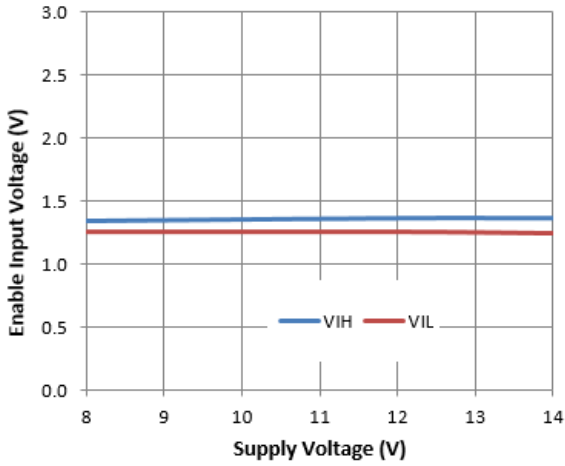


Fig 22. Enable Input Voltage vs. Supply Voltage

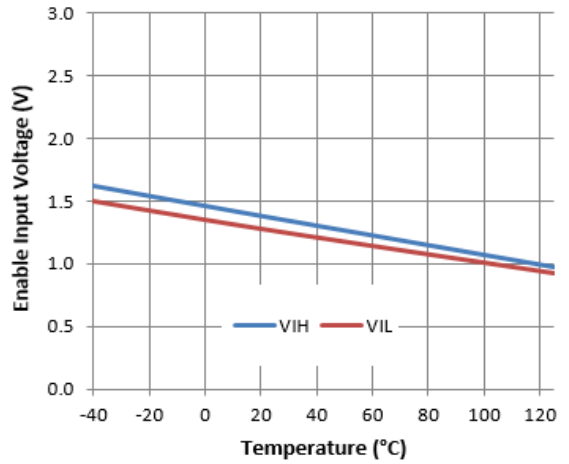


Fig 23. Enable Input Voltage vs. Temperature

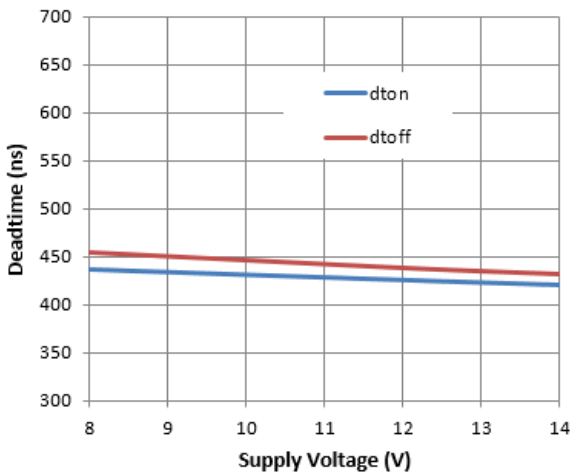


Figure 24. Deadtime vs. Supply Voltage

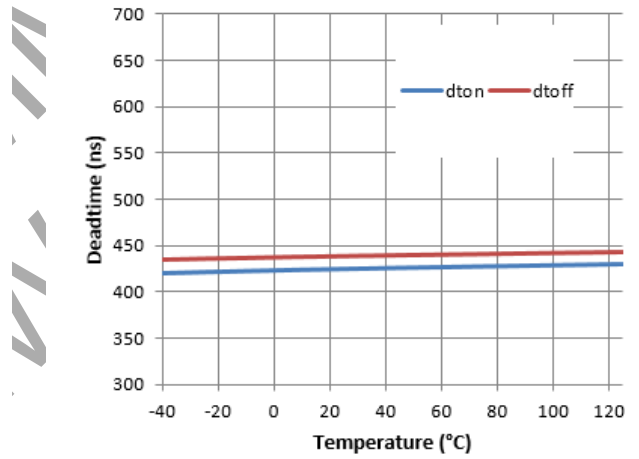


Figure 25. Deadtime vs. Temperature

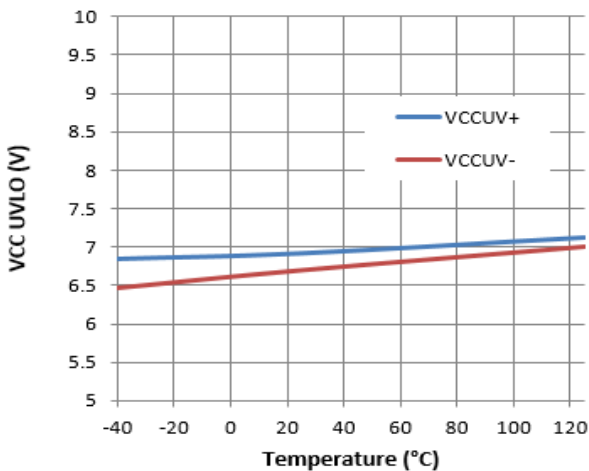


Figure 26. VCC UVLO vs. Temperature

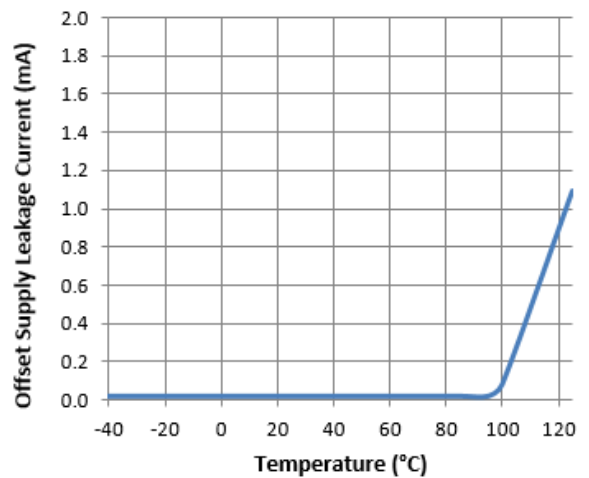


Figure 27. Offset Supply Leakage Current vs. Temperature

Application Information

Bootstrap Capacitor Selection

The capacitance of the bootstrap capacitor should be high enough to provide the charge required by the gate of the high side MOSFET with only a minimal loss of voltage across it. As a general guideline, it is recommended to make sure the charge stored by the bootstrap capacitor is about 50 times more than the required gate charge at operating V_{CC} (usually about 10V to 12V).

The formula to calculate the change in V_{BS} to provide a certain amount of gate charge is shown below;
 $Q = C * V$ where Q is the gate charge required by the external MOSFET to raise its gate voltage to 10V. C is the bootstrap capacitance and V is the voltage drop across the V_{BS} .

Example: To switch a high side MOSFET that requires 20nC of gate charge to raise its gate voltage to 10V, the capacitor size can be calculated as below;

$$Q_{G(MOSFET)} = C_{(BOOTSTRAP)} * \Delta V_{BS} ;$$

ΔV_{BS} = voltage drop across the bootstrap capacitor while providing the required gate charge.

In this example, let's say the acceptable ΔV_{BS} is 200mV.

The required bootstrap capacitor for the job is;

$$C_{(BOOTSTRAP)} = Q_{G(MOSFET)} / \Delta V_{BS} = 20nC / 200mV = 100nF$$

Bootstrap Diode Current

The DGD0506 comes with an integrated bootstrap Schottky diode. The forward characteristics of the diode is shown in the figure 28. The maximum recommended operating current is 400mA pulsed. Under steady state conditions the only current flowing through the internal diode is the charge current required by the highside MOSFET's gate capacitance, however, it is important to cover applications where the inrush current exceeds this rating. In such applications to limit the current flowing through the internal diode to the recommended value, two techniques are suggested as shown in figures 29 and 30.

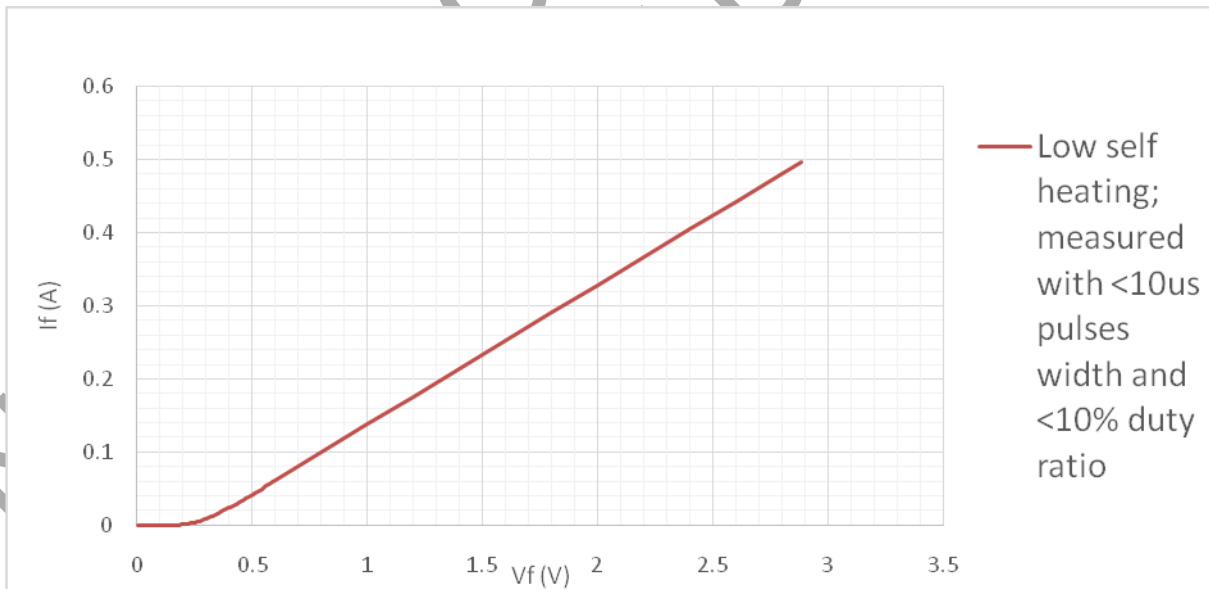


Figure 28. DGD0506 'Internal Diode + Internal Resistor' V_F vs. I_F

Pre-Bias Resistor between Vs and COM

This technique eliminates the inrush current, altogether, by pre-charging the capacitor to a value close to V_{CC} before the DGD0506 is enabled and an input signal is applied. By pre-charging the capacitor to V_{CC} only a small steady state current flows through the internal diode eliminating the need for any external diode. The recommended range for the R_s is 10k Ω to 100k Ω .

Application Information (Cont.)

External Diode and Resistor:

To enable appropriate current sharing and limit the internal bootstrap current to less than 400mA, a Schottky diode must be used as an external diode. The voltage drop across the external diode and resistor must be limited to 2.4V, to limit the internal diode's current share to <400mA. Hence it is important to choose an appropriate external diode and resistor combination. At any observed inrush current peak, it is important that the combined voltage drop of the external resistor and diode is less than 2.4V.

For internal diode current to be <400mA; $(I_{INRUSH} * R_{EXT}) + (V_{fEXT} @ I_{INRUSH}) < 2.4V$.

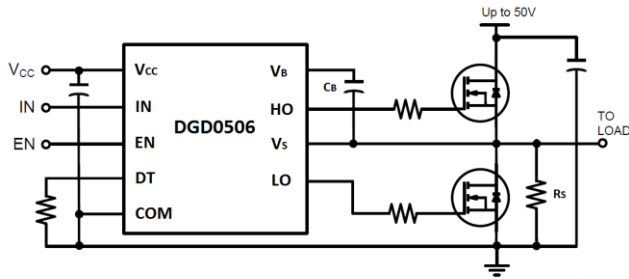


Figure 29. Inrush current is greatly limited by pre-charging the boost-strap Capacitor through Rs

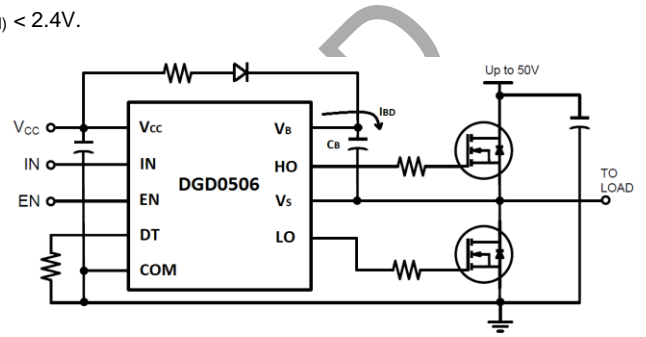


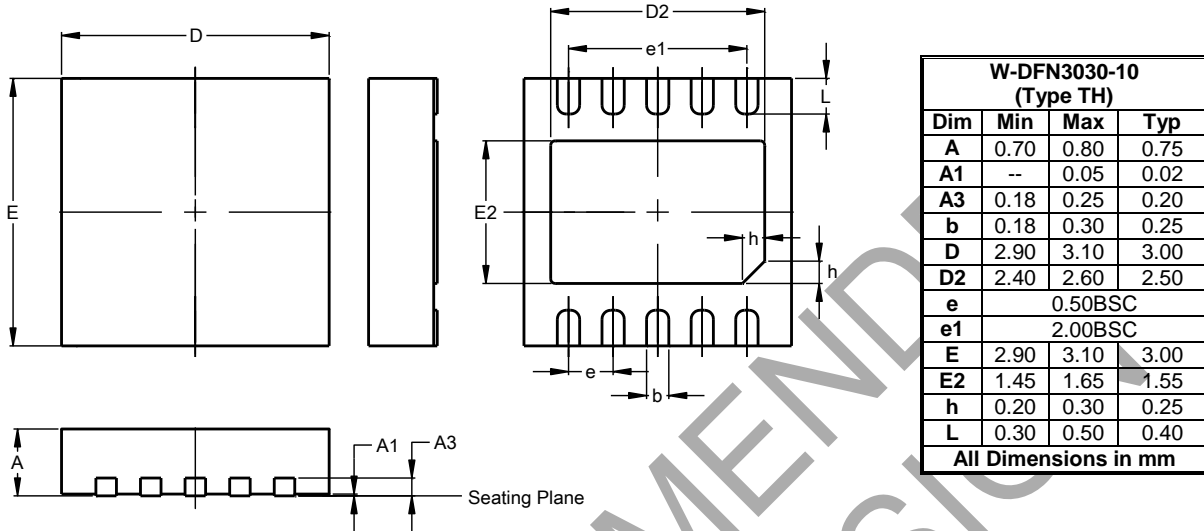
Figure 30. Current into the boost-strap capacitance is shared between the external diode and the internal Diode

NOT RECOMMENDED FOR NEW DESIGN

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

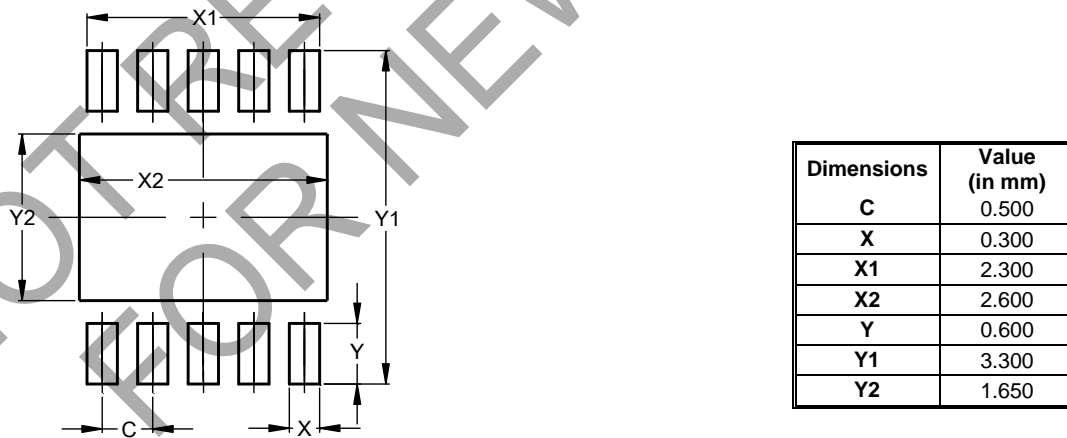
W-DFN3030-10 (Type TH)



Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

W-DFN3030-10 (Type TH)



Note : For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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