

Product Summary

Device	V _{(BR)DSS}	R _{DS(ON)} Max	I _D Max T _A = +25°C (Notes 6 & 8)
Q1	40V	45mΩ @ V _{GS} = 10V	5.5A
		60mΩ @ V _{GS} = 4.5V	4.2A
Q2	-40V	45mΩ @ V _{GS} = -10V	-5.8A
		60mΩ @ V _{GS} = -4.5V	-4.2A

Description and Applications

This MOSFET is designed to ensure that R_{DS(ON)} of N and P channel FET are matched to minimize losses in both arms of the bridge. The DMC4040SSD is optimized for use in 3-phase brushless DC motor circuits (BLDC), and CCFL backlighting.

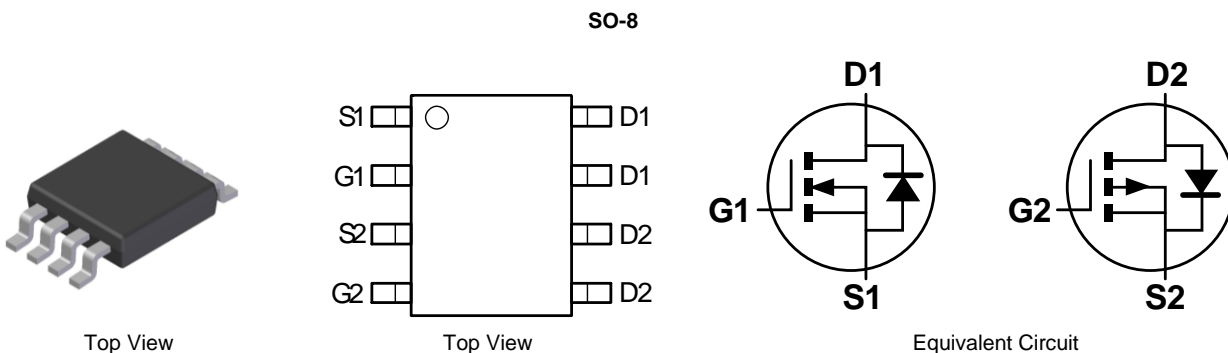
- 3-Phase BLDC Motor
- CCFL Backlighting

Features and Benefits

- Matched N & P R_{DS(ON)} – Minimizes Power Losses
- Fast Switching – Minimizes Switching Losses
- Dual Device – Reduces PCB Area
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **For automotive applications requiring specific change control (i.e.: parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please refer to the related automotive grade (Q-suffix) part. A listing can be found at <https://www.diodes.com/products/automotive/automotive-products/>.**
- This part is qualified to JEDEC standards (as referenced in AEC-Q) for High Reliability. <https://www.diodes.com/quality/product-definitions/>
- **An Automotive-Compliant Part is Available Under Separate Datasheet (DMC4055SSDQ)**

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 (e3)
- Weight: 0.074 grams (Approximate)

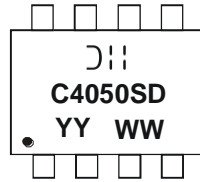


Ordering Information (Note 4)

Product	Case	Packaging
DMC4050SSD-13	SO-8	2500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



☺ = Manufacturer's Marking
 C4050SD = Product Type Marking Code
 YYWW = Date Code Marking
 YY or YY= Year (ex: 20 = 2020)
 WW = Week (01 - 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

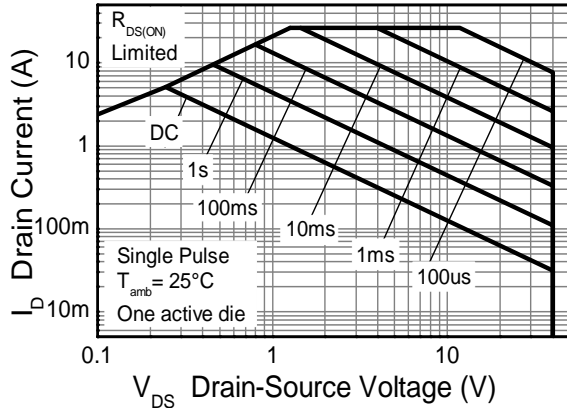
Characteristic		Symbol	N-Channel - Q1	P-Channel - Q2	Units
Drain-Source Voltage		V _{DSS}	40	-40	V
Gate-Source Voltage		V _{GSS}	±20	±20	
Continuous Drain Current	V _{GS} = 10V	(Notes 6 & 8)	5.8	-5.8	A
		T _A = +70°C (Notes 6 & 8)	4.38	-4.52	
		(Notes 5 & 8)	4.2	-4.2	
		(Notes 5 & 9)	5.3	-5.3	
Pulsed Drain Current	V _{GS} = 10V	I _{DM}	24.1	-24.9	
Continuous Source Current (Body Diode)		I _S	2.5	-2.5	
Pulsed Source Current (Body Diode)		I _{SM}	24.1	-24.9	

Thermal Characteristics

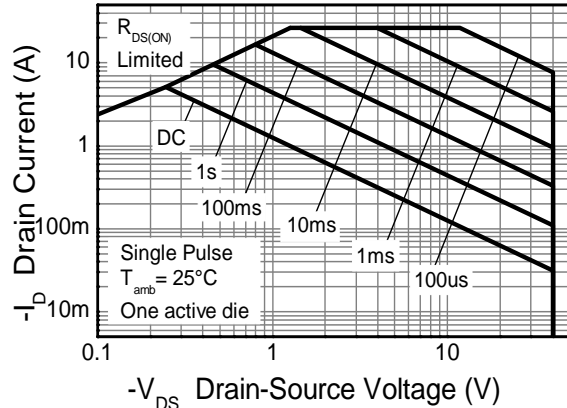
Characteristic	Symbol	Value	Unit
Power Dissipation	P _D	1.25	W
Linear Derating Factor		1.8	
		2.14	
Thermal Resistance, Junction to Ambient	R _{θJA}	100	°C/W
		70	
		58	
Thermal Resistance, Junction to Lead	R _{θJL}	51	
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

- Notes:
5. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
 6. Same as note (5), except the device is measured at t ≤ 10 sec.
 7. Same as note (5), except the device is pulsed with D = 0.02 and pulse width 300µs.
 8. For a dual device with one active die.
 9. For a device with two active die running at equal power.
 10. Thermal resistance from junction to solder-point (at the end of the drain lead).

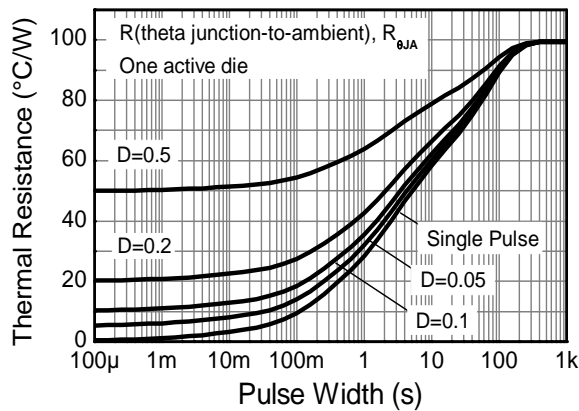
Thermal Characteristics (continued)



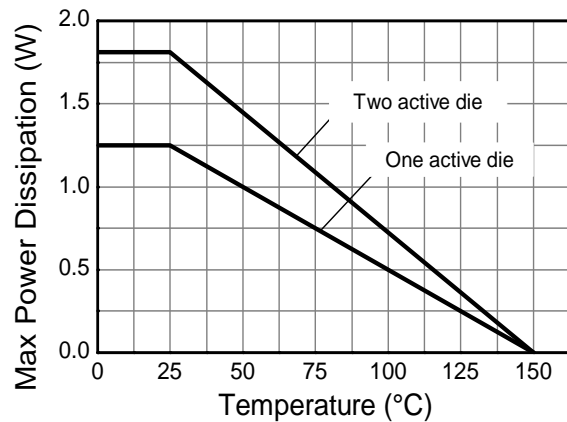
N-channel Safe Operating Area



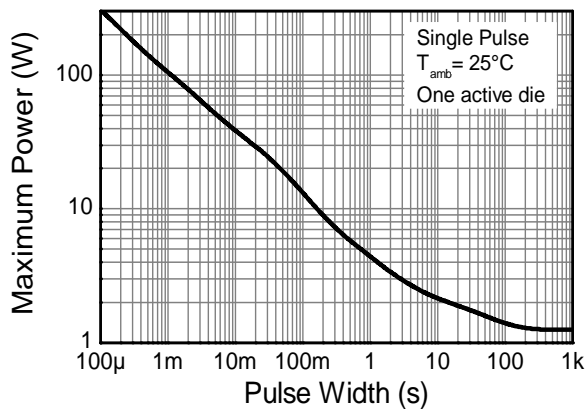
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation

Electrical Characteristics (Q1 N-Channel) (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 11)						
Drain-Source Breakdown Voltage	BV _{DSS}	40	—	—	V	V _{GS} = 0V, I _D = 250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	1.0	μA	V _{DS} = 40V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 11)						
Gate Threshold Voltage	V _{GS(th)}	0.8	1.3	1.8	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	20	45	mΩ	V _{GS} = 10V, I _D = 3A
			33	60		V _{GS} = 4.5V, I _D = 3A
Forward Transfer Admittance	Y _{fs}	—	12.6	—	S	V _{DS} = 5V, I _D = 3A
Diode Forward Voltage (Note 11)	V _{SD}	—	0.7	1.0	V	V _{GS} = 0V, I _S = 1A
DYNAMIC CHARACTERISTICS (Note 12)						
Input Capacitance	C _{iss}	—	1790.8	—	pF	V _{DS} = 20V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	160.6	—	pF	
Reverse Transfer Capacitance	C _{riss}	—	120.5	—	pF	
Gate Resistance	R _g	—	1.03	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge	Q _g	—	37.56	—	nC	V _{GS} = 10V, V _{DS} = 20V, I _D = 3A
Gate-Source Charge	Q _{gs}	—	7.8	—	nC	
Gate-Drain Charge	Q _{gd}	—	6.6	—	nC	
Turn-On Delay Time	t _{D(on)}	—	8.08	—	nS	V _{GS} = 10V, V _{DS} = 20V, I _D = 3A
Turn-On Rise Time	t _r	—	15.14	—	nS	
Turn-Off Delay Time	t _{D(off)}	—	24.29	—	nS	
Turn-Off Fall Time	t _f	—	5.27	—	nS	

Electrical Characteristics (Q2 P-Channel) (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 11)						
Drain-Source Breakdown Voltage	BV _{DSS}	-40	—	—	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	—	—	-1.0	μA	V _{DS} = -40V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 11)						
Gate Threshold Voltage	V _{GS(th)}	-0.8	-1.3	-1.8	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	28	45	mΩ	V _{GS} = -10V, I _D = -3A
			30	60		V _{GS} = -4.5V, I _D = -3A
Forward Transfer Admittance	Y _{fs}	—	16.6	—	S	V _{DS} = -5V, I _D = -3A
Diode Forward Voltage (Note 11)	V _{SD}	—	-0.7	-1.0	V	V _{GS} = 0V, I _S = -1A
DYNAMIC CHARACTERISTICS (Note 12)						
Input Capacitance	C _{iss}	—	1643.17	—	pF	V _{DS} = -20V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oss}	—	179.13	—	pF	
Reverse Transfer Capacitance	C _{riss}	—	127.82	—	pF	
Gate Resistance	R _g	—	6.43	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge	Q _g	—	33.66	—	nC	V _{GS} = -10V, V _{DS} = -20V, I _D = -3A
Gate-Source Charge	Q _{gs}	—	5.54	—	nC	
Gate-Drain Charge	Q _{gd}	—	7.30	—	nC	
Turn-On Delay Time	t _{D(on)}	—	6.85	—	nS	V _{GS} = -10V, V _{DS} = -20V, I _D = -3A
Turn-On Rise Time	t _r	—	14.72	—	nS	
Turn-Off Delay Time	t _{D(off)}	—	53.65	—	nS	
Turn-Off Fall Time	t _f	—	30.86	—	nS	

Notes: 11. Short duration pulse test used to minimize self-heating effect.
12. Guaranteed by design. Not subject to production testing.

Typical Characteristics (Q1 N-Channel)

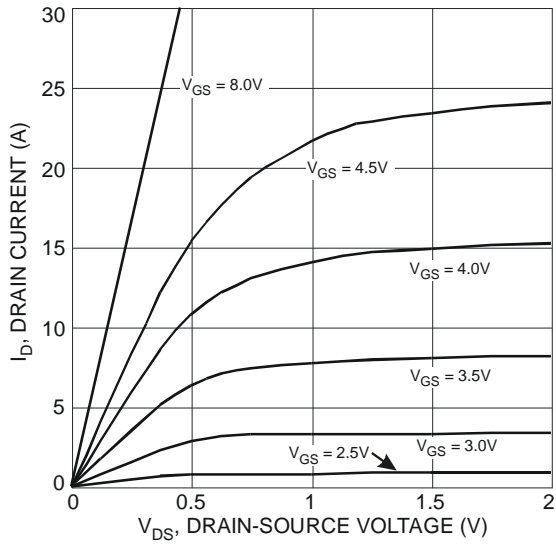


Fig. 1 Typical Output Characteristic

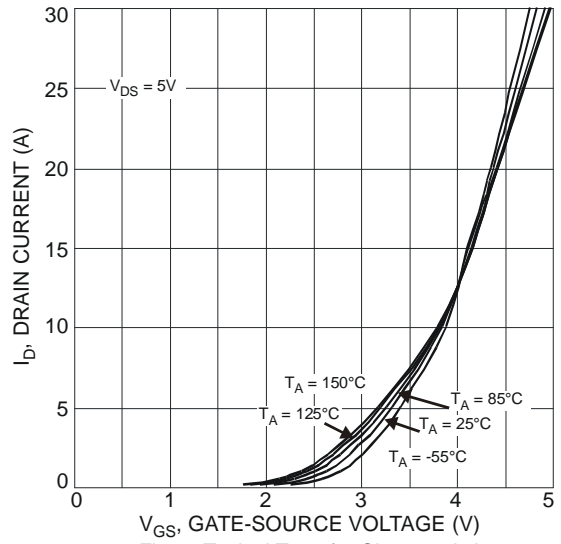


Fig. 2 Typical Transfer Characteristic

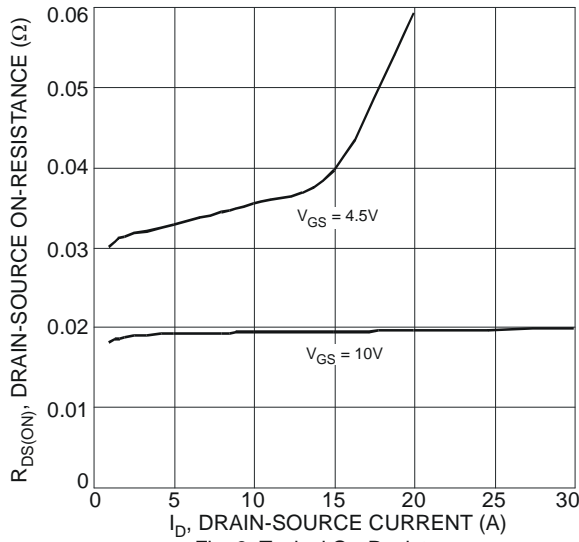


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

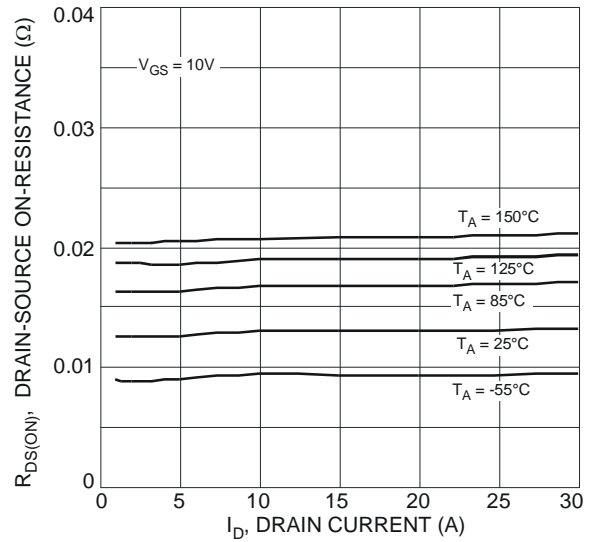


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

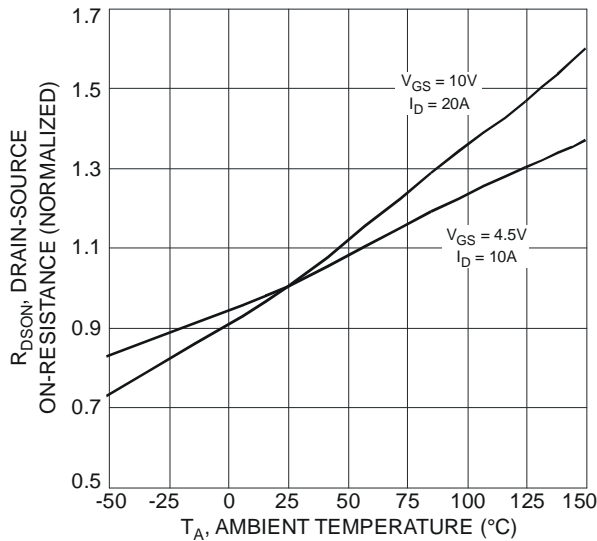


Fig. 5 On-Resistance Variation with Temperature

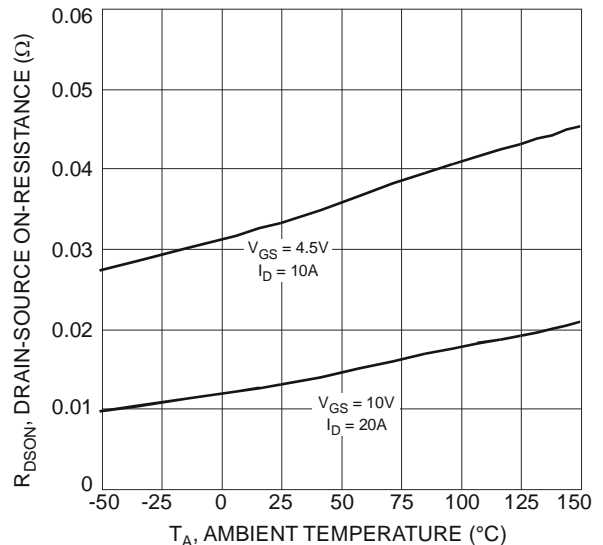


Fig. 6 On-Resistance Variation with Temperature

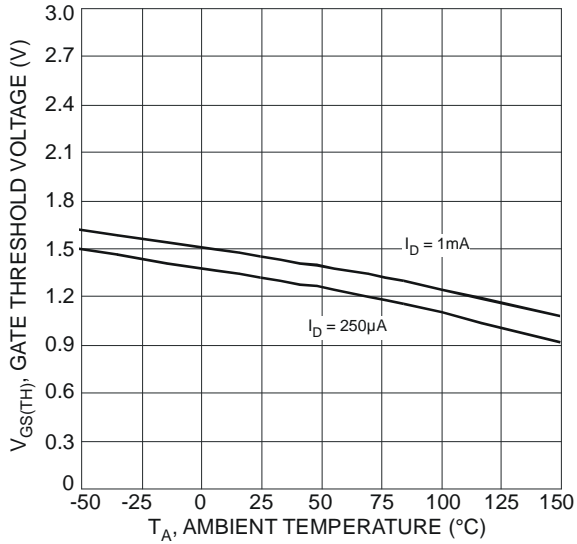


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

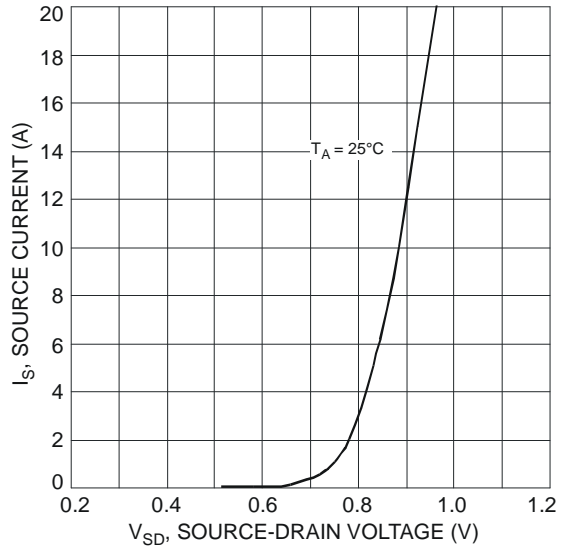


Fig. 8 Diode Forward Voltage vs. Current

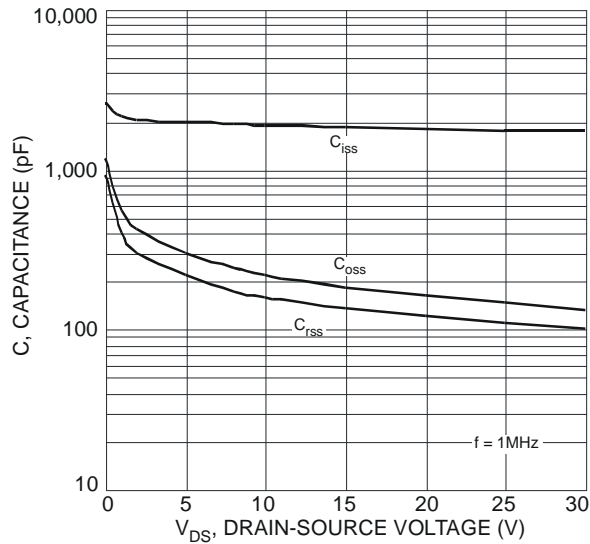


Fig. 9 Typical Total Capacitance

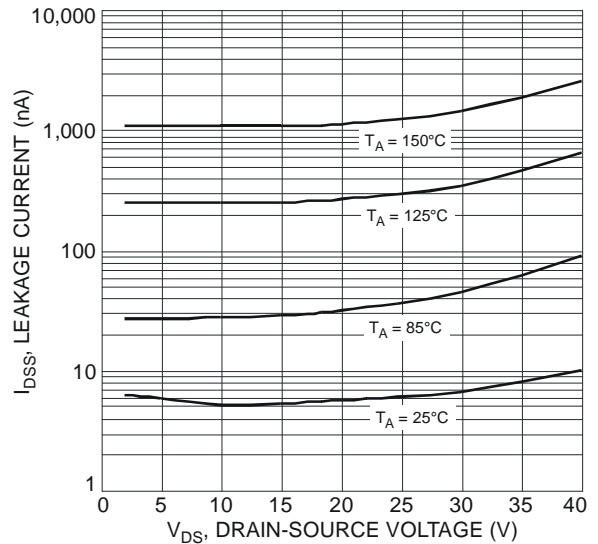


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

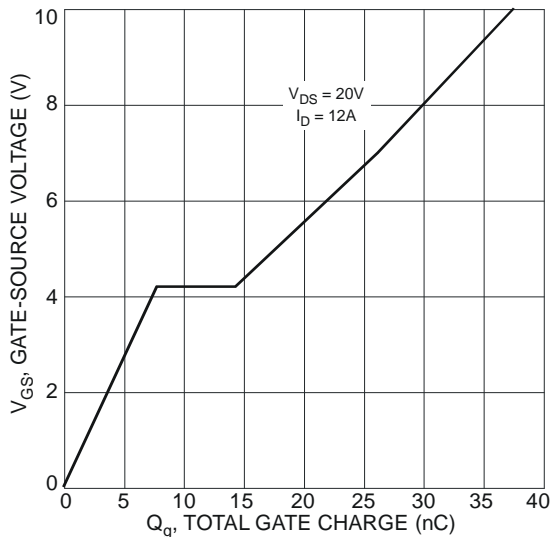


Fig. 11 Gate-Charge Characteristics

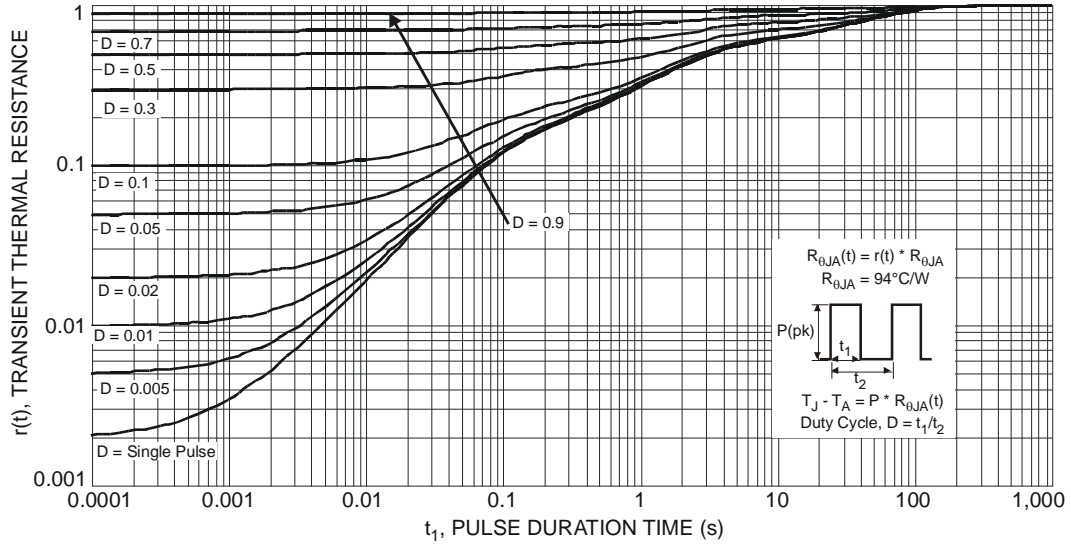


Fig. 12 Transient Thermal Response

Typical Characteristics (Q2 P-Channel)

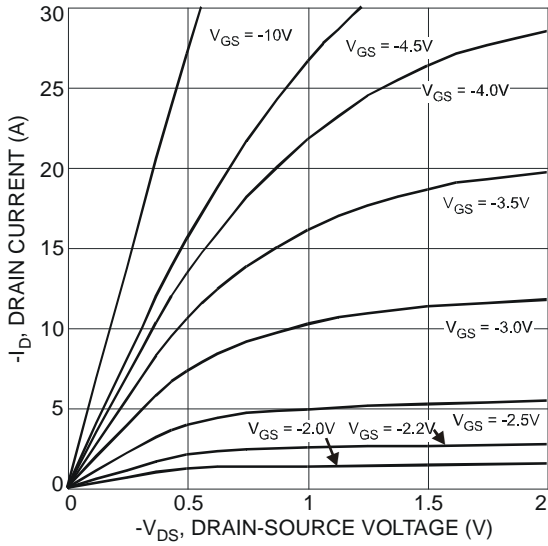


Fig. 13 Typical Output Characteristic

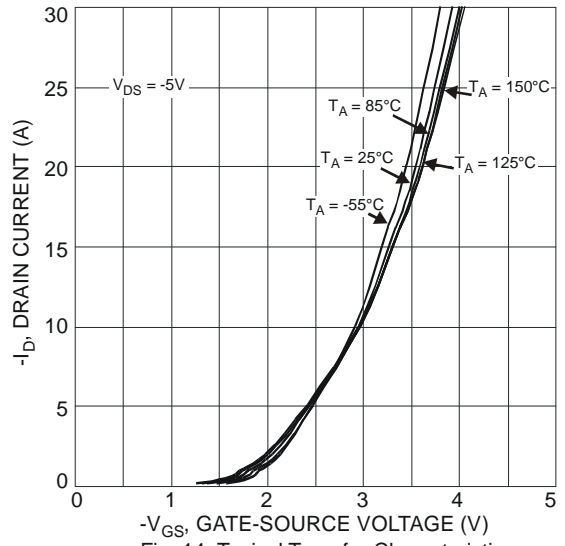


Fig. 14 Typical Transfer Characteristic

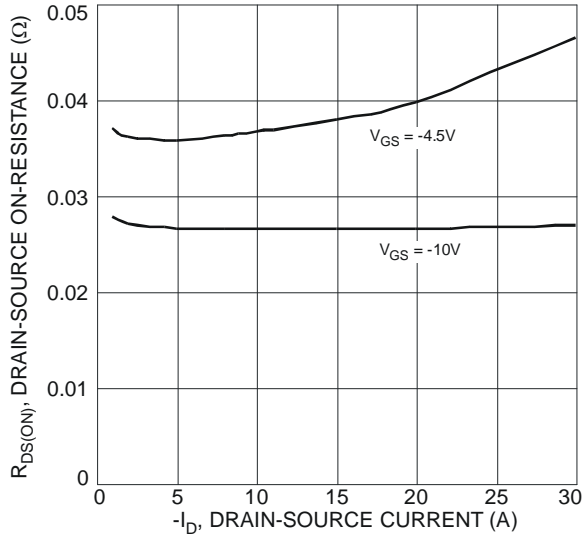


Fig. 15 Typical On-Resistance vs. Drain Current and Gate Voltage

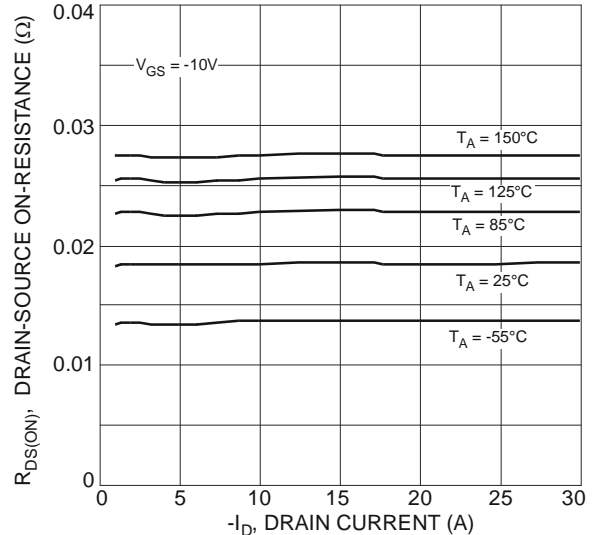


Fig. 16 Typical On-Resistance vs. Drain Current and Temperature

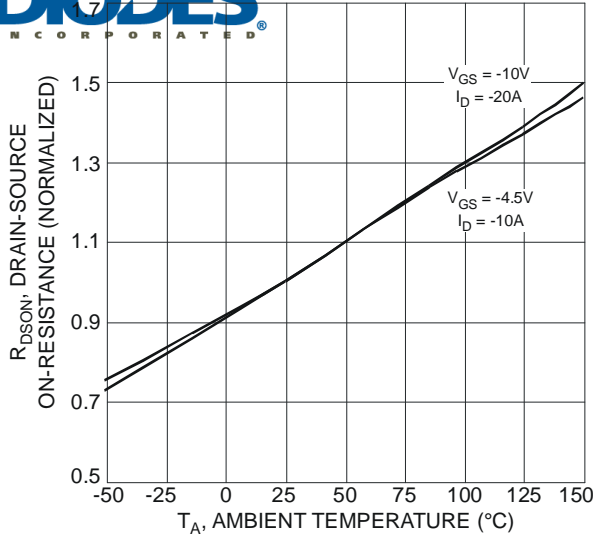


Fig. 17 On-Resistance Variation with Temperature

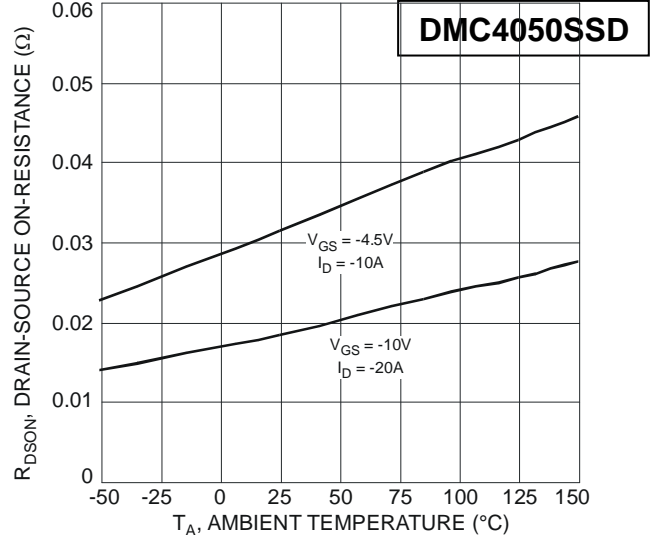


Fig. 18 On-Resistance Variation with Temperature

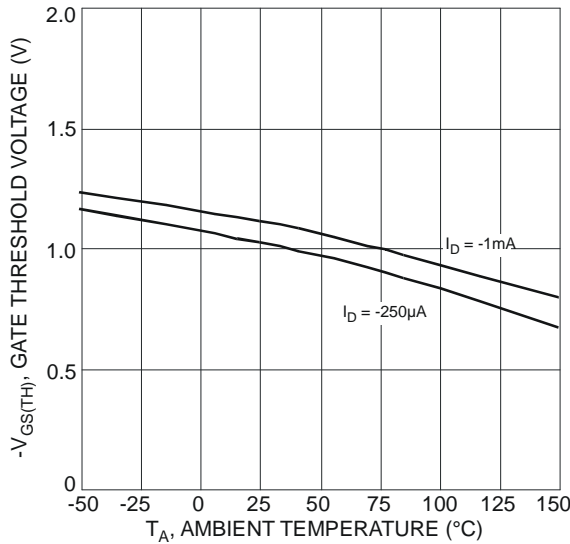


Fig. 19 Gate Threshold Variation vs. Ambient Temperature

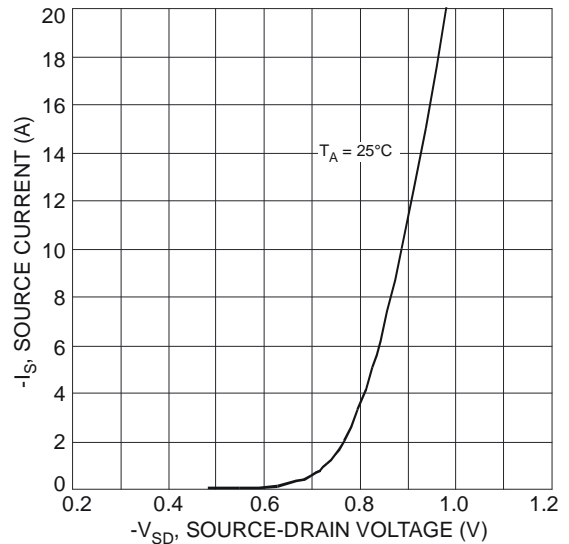


Fig. 20 Diode Forward Voltage vs. Current

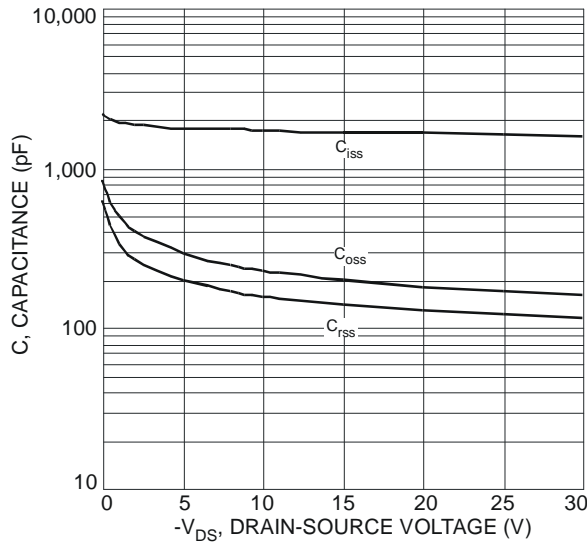


Fig. 21 Typical Total Capacitance

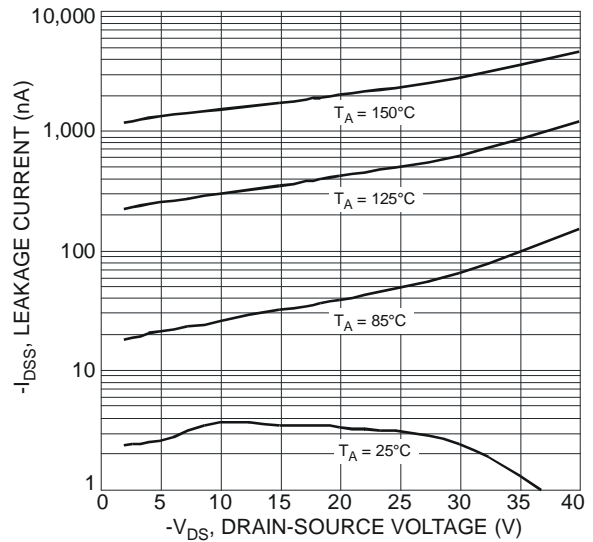


Fig. 22 Typical Leakage Current vs. Drain-Source Voltage

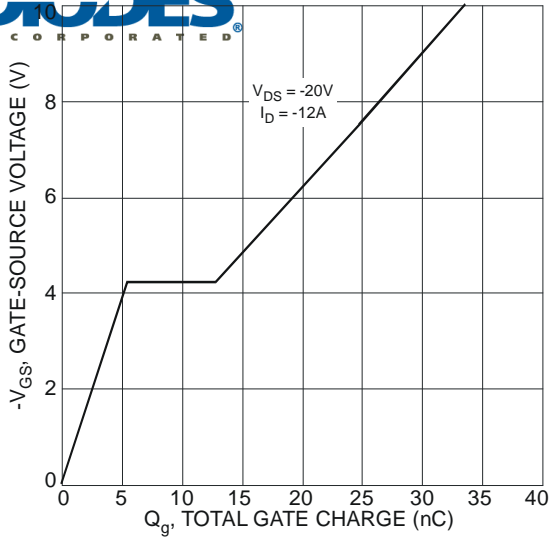


Fig. 23 Gate-Charge Characteristics

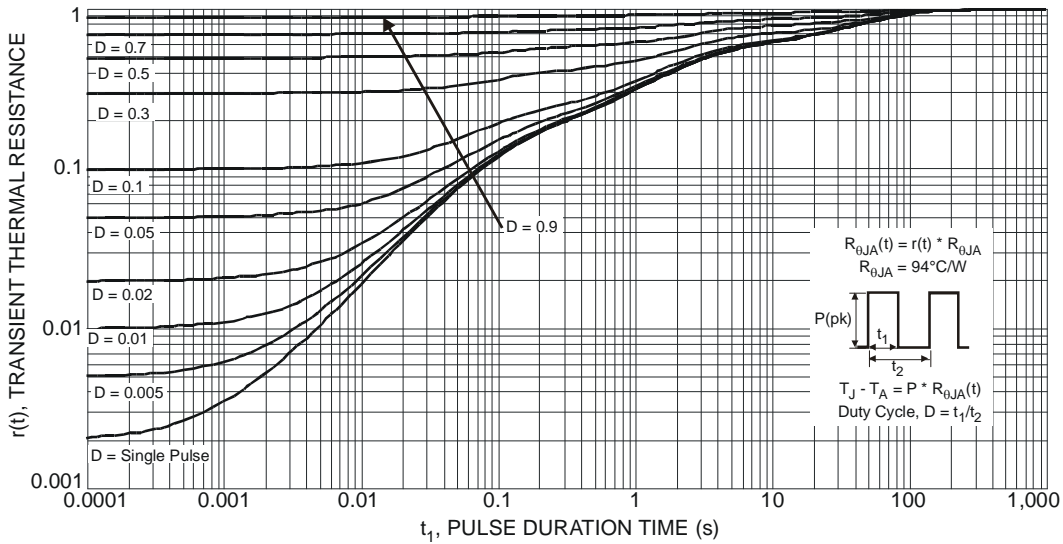
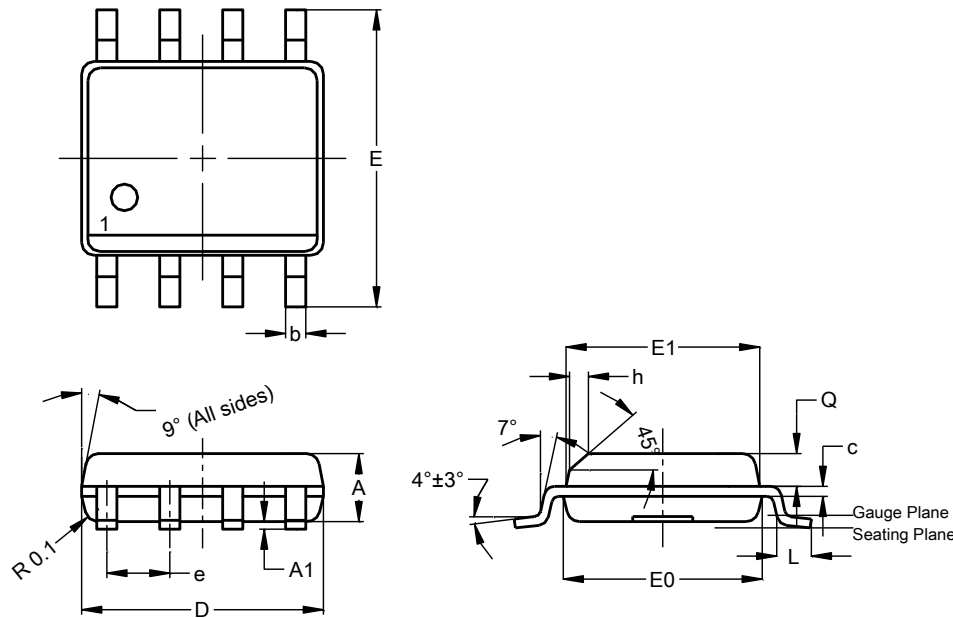


Fig. 24 Transient Thermal Response

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SO-8

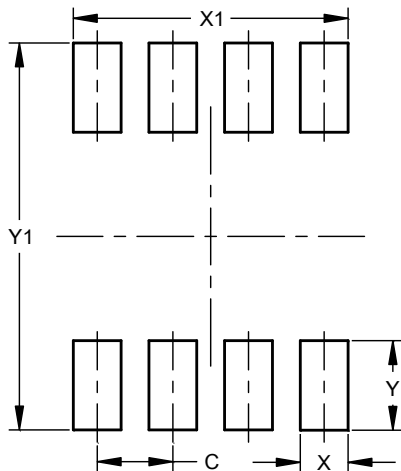


SO-8			
Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50

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[SSM6P69NU,LF](#) [DMP22D4UFO-7B](#) [DMN1006UCA6-7](#) [DMN16M9UCA6-7](#)