Product Summary

Device	BV_{DSS}	$R_{DS(ON)}$ Max	I_D T_A = +25°C
Q1 N-Channel	60V	29mΩ @ V_{GS} = 10V	6.0A
		34mΩ @ V_{GS} = 6V	5.5A
Q2 P-Channel	-60V	50mΩ @ V_{GS} = -10V	-5.0A
		70mΩ @ V_{GS} = -4.5V	-4.6A

Features and Benefits

- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

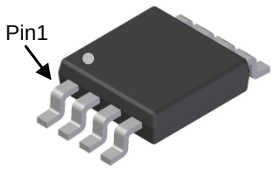
Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

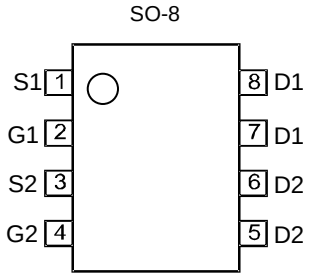
- DC-DC Converters
- Power Management Functions
- Backlighting

Mechanical Data

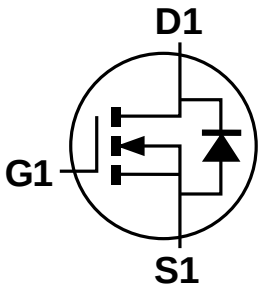
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Tin Finish Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.074 grams (Approximate)



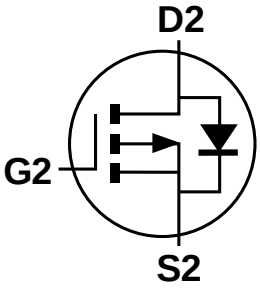
Top View



Top View
Pin Configuration



Q1 N-Channel MOSFET



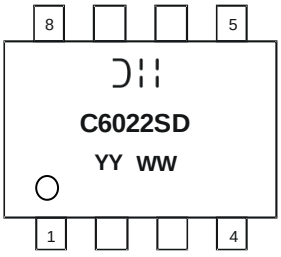
Q2 P-Channel MOSFET

Ordering Information (Note 4)

Part Number	Case	Packaging
DMC6022SSD-13	SO-8	2,500/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



= Manufacturer's Marking
C6022SD = Product Type Marking Code
YYWW = Date Code Marking
YY or $\overline{YY}$ = Year (ex: 16= 2016)
WW = Week (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Q1	Q2	Unit
Drain-Source Voltage			V_{DSS}	60	-60	V
Gate-Source Voltage			V_{GSS}	±20	±20	V
Continuous Drain Current (Note 6) N-Channel: V_{GS} = 10V P-Channel: V_{GS} = -10V	Steady State	T_A = +25°C T_A = +70°C	I_D	6.0 5.0	-5.0 -4.0	A
	t<10s	T_A = +25°C T_A = +70°C	I_D	8.4 6.7	-6.5 -5.2	A
Maximum Body Diode Forward Current (Note 6)			I_S	2.0	-2.0	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	45	-35	A
Avalanche Current (Note 7) L = 0.1mH			I_{AS}	22	-25	A
Avalanche Energy (Note 7) L = 0.1mH			E_{AS}	24	24	mJ

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	1.5	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	$R_{\theta JA}$	102	°C/W
	t < 10s		64	
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	2.0	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	$R_{\theta JA}$	74	°C/W
	t<10s		47	
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	10	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics N-Channel Q1 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1	µA	V_{DS} = 60V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.0	—	3.0	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	21	29	mΩ	V_{GS} = 10V, I_D = 5A
			22	34		V_{GS} = 6V, I_D = 5A
Diode Forward Voltage	V_{SD}	—	0.8	1.2	V	V_{GS} = 0V, I_S = 1.7A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	2110	—	pF	V_{DS} = 30V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	78	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	51	—	pF	
Gate Resistance	R_g	—	2.0	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge at (V_{GS} = 4.5V)	Q_g	—	14	—	nC	V_{DS} = 30V, I_D = 6A
Total Gate Charge at (V_{GS} = 10V)	Q_g	—	32	—	nC	
Gate-Source Charge	Q_{gs}	—	7.0	—	nC	
Gate-Drain Charge	Q_{gd}	—	4.0	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	5.4	—	ns	V_{GS} = 10V, V_{DS} = 30V, R_G = 6Ω, I_D = 1A
Turn-On Rise Time	t_R	—	4.4	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	30.4	—	ns	
Turn-Off Fall Time	t_F	—	8.4	—	ns	
Body Diode Reverse Recovery Time	t_{RR}	—	18.1	—	ns	I_F = 1.7A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q_{RR}	—	12.5	—	nC	I_F = 1.7A, di/dt = 100A/µs

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. UIS in production with L = 0.1mH, starting T_A = +25°C.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

Electrical Characteristics P-Channel Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	-60	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	-1	µA	V_{DS} = -60V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1.0	—	-3.0	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	35	50	mΩ	V_{GS} = -10V, I_D = -5A
			45	70		V_{GS} = -4.5V, I_D = -4A
Diode Forward Voltage	V_{SD}	—	-0.7	-1.2	V	V_{GS} = 0V, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1525	—	pF	V_{DS} = -30V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	90	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	70	—	pF	
Gate Resistance	R_g	—	16	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	14.5	—	nC	V_{DS} = -30V, I_D = -5A
Total Gate Charge (V_{GS} = -10V)	Q_g	—	30.6	—	nC	
Gate-Source Charge	Q_{gs}	—	4.9	—	nC	
Gate-Drain Charge	Q_{gd}	—	5.2	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	5.3	—	ns	V_{GS} = -10V, V_{DS} = -30V, R_G = 3Ω, I_D = -5A
Turn-On Rise Time	t_R	—	15.4	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	79.2	—	ns	
Turn-Off Fall Time	t_F	—	45.3	—	ns	
Body Diode Reverse Recovery Time	t_{RR}	—	15.2	—	ns	I_F = -5A, di/dt = -100A/µs
Body Diode Reverse Recovery Charge	Q_{RR}	—	9.3	—	nC	I_F = -5A, di/dt = -100A/µs

Notes: 8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

N-Channel

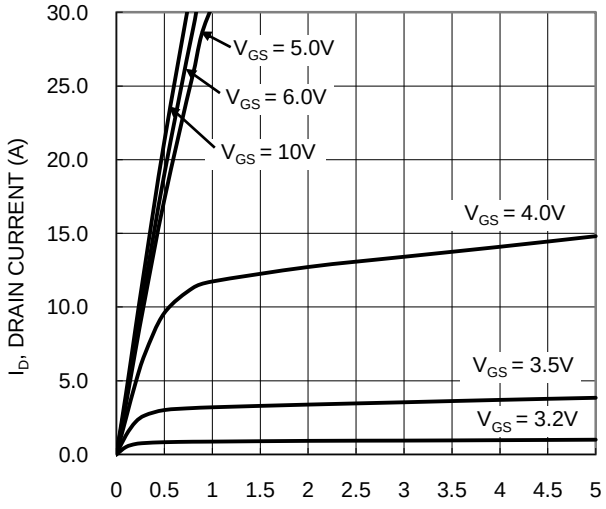


Figure 1. Typical Output Characteristic

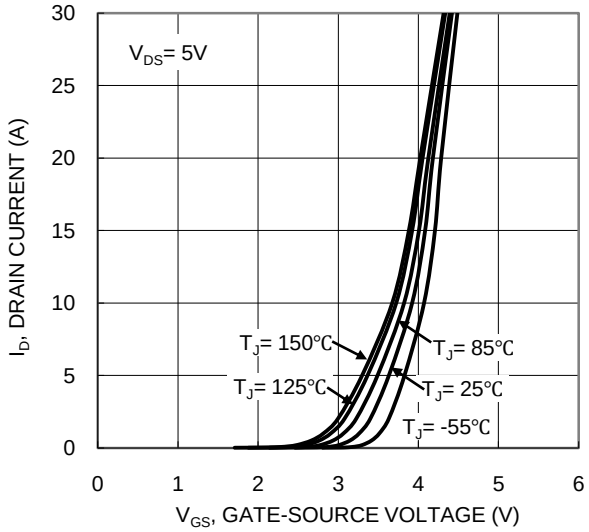


Figure 2. Typical Transfer Characteristic

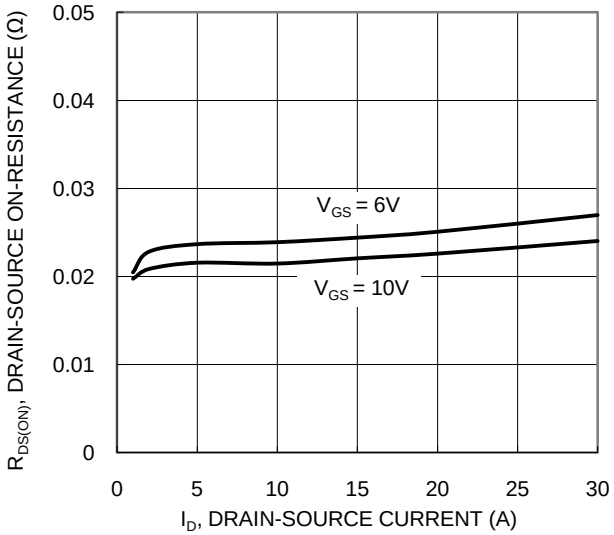


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

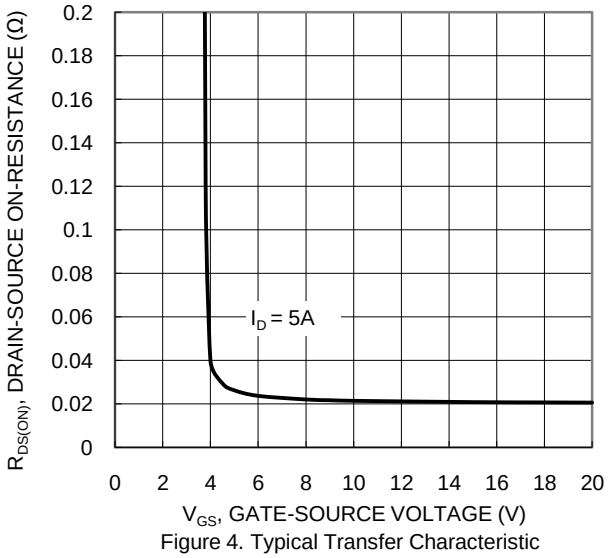


Figure 4. Typical Transfer Characteristic

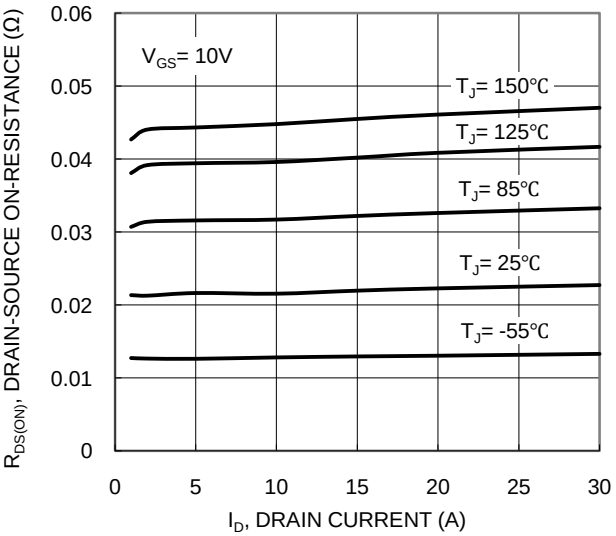


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

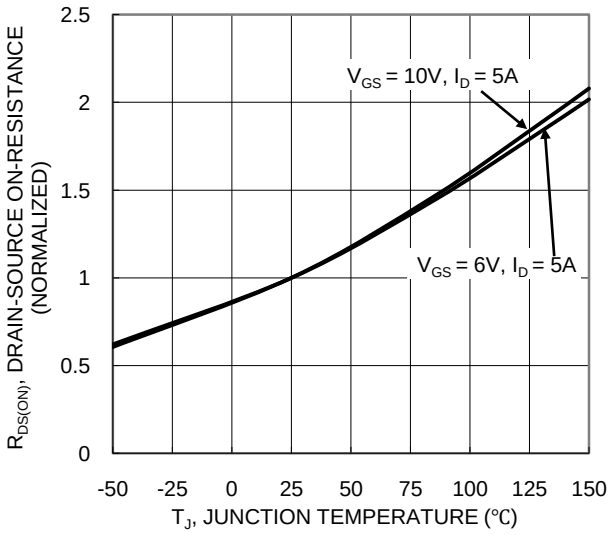


Figure 6. On-Resistance Variation with Junction Temperature

N-Channel (Cont.)

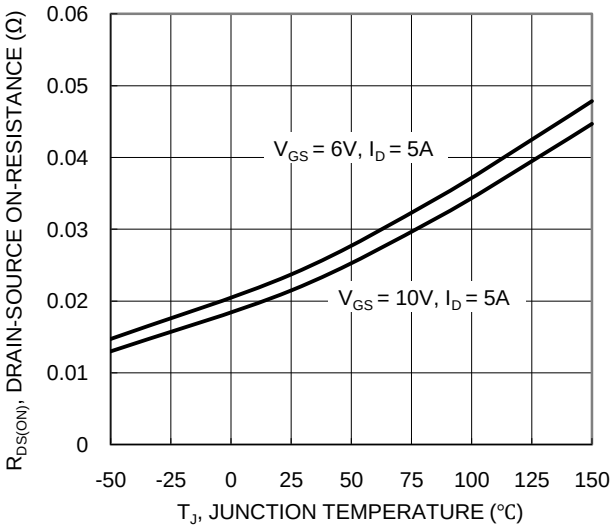


Figure 7.On-Resistance Variation with Junction Temperature

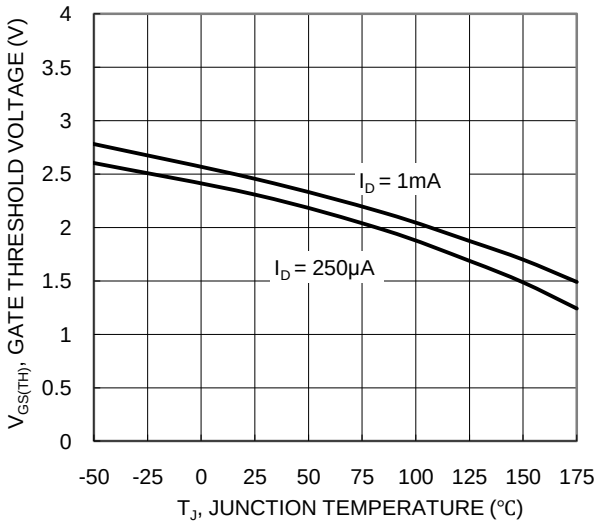


Figure 8. Gate Threshold Variation vs. Junction Temperature

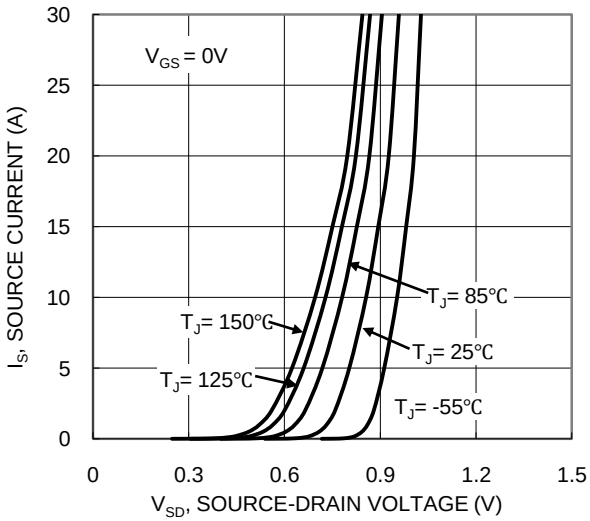


Figure 9. Diode Forward Voltage vs. Current

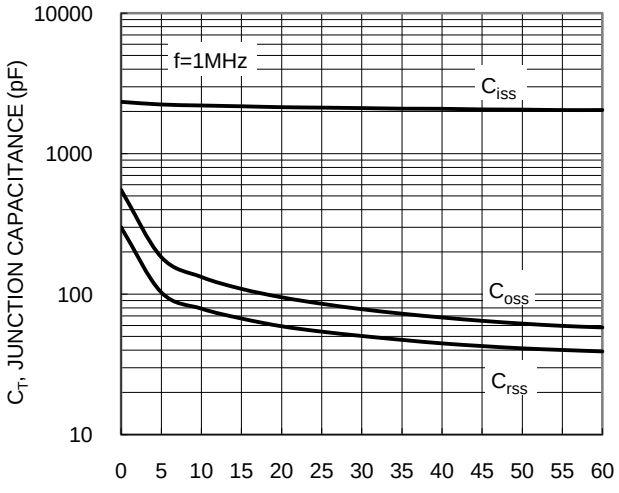


Figure 10. Typical Junction Capacitance

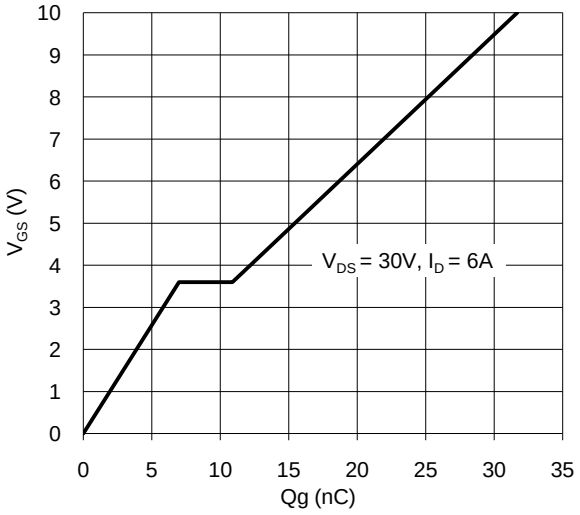


Figure 11. Gate Charge

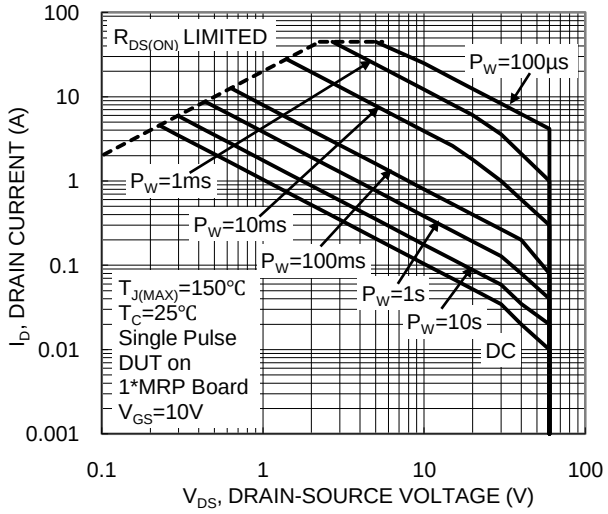


Figure 12. SOA, Safe Operation Area

P-Channel

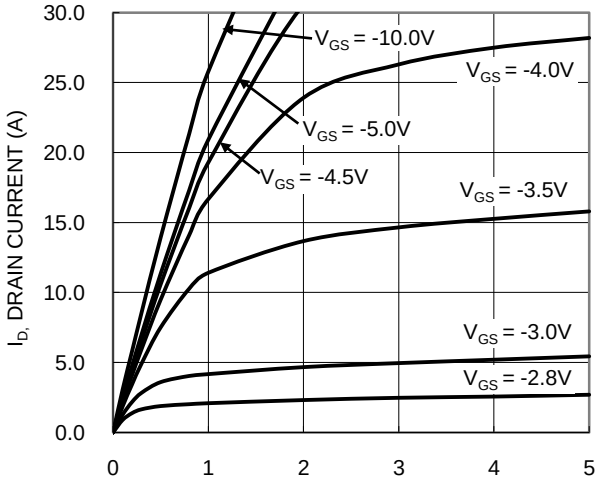


Figure 13. Typical Output Characteristic

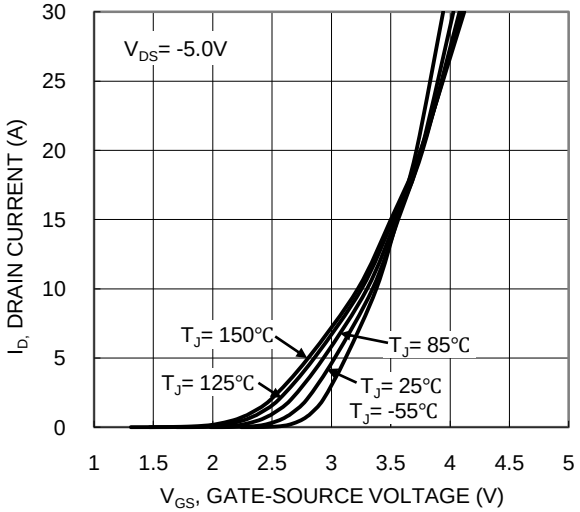


Figure 14. Typical Transfer Characteristic

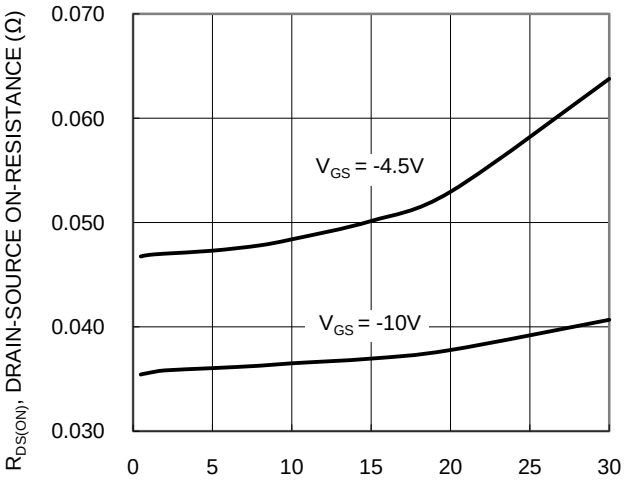


Figure 15. Typical On-Resistance vs. Drain Current and Gate Voltage

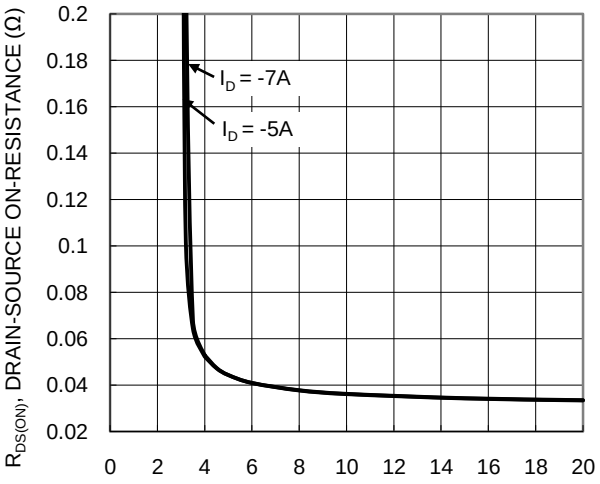


Figure 16. Typical Transfer Characteristic

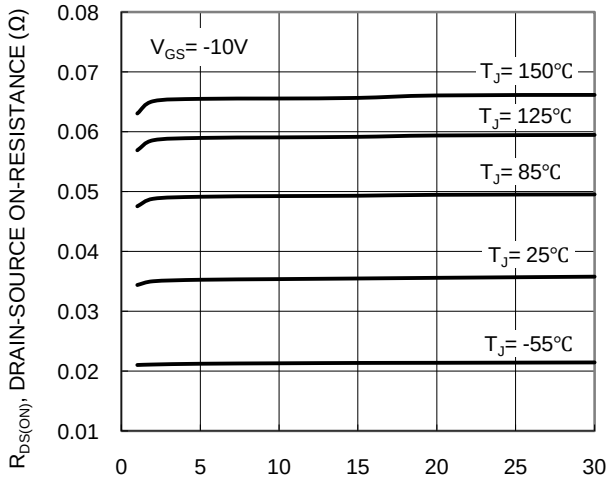


Figure 17. Typical On-Resistance vs. Drain Current and Temperature

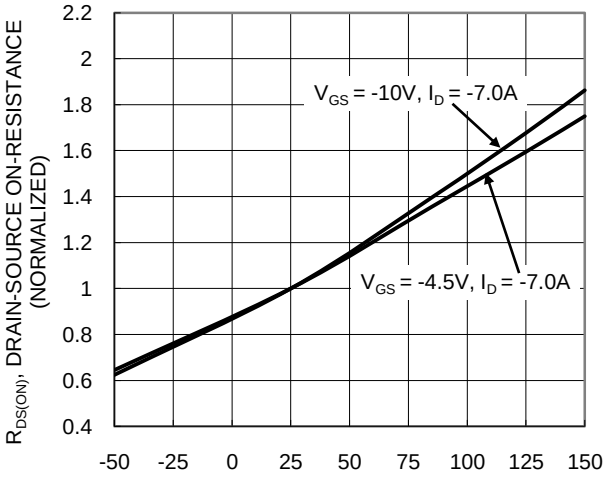


Figure 18. On-Resistance Variation with Temperature

P-Channel (Cont.)

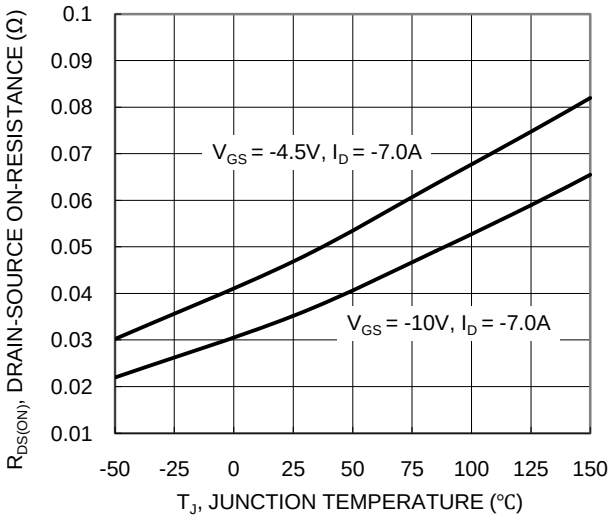


Figure 19. On-Resistance Variation with Temperature

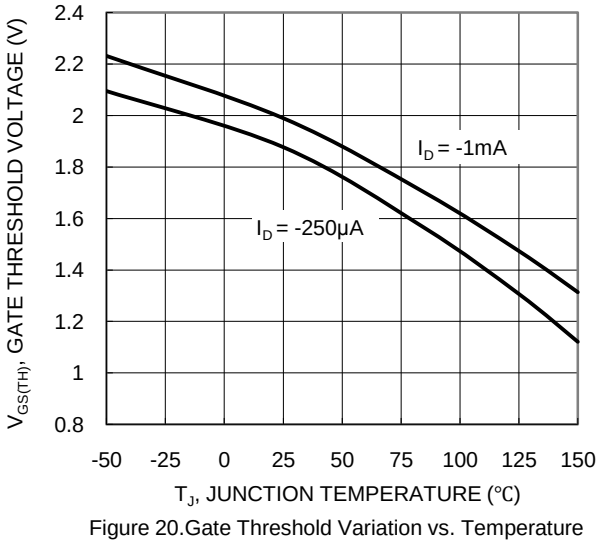


Figure 20.Gate Threshold Variation vs. Temperature

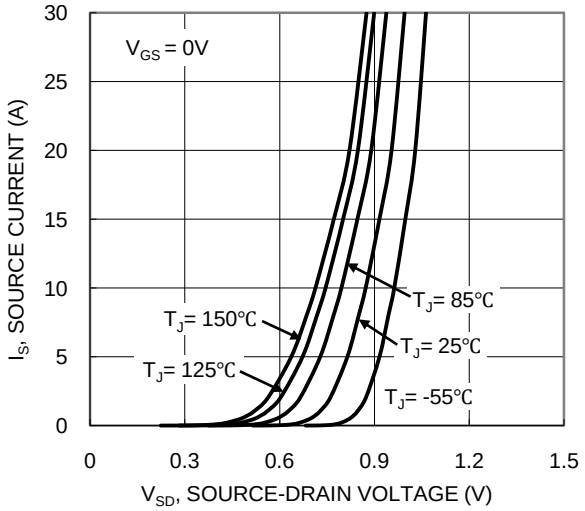


Figure 21. Diode Forward Voltage vs. Current

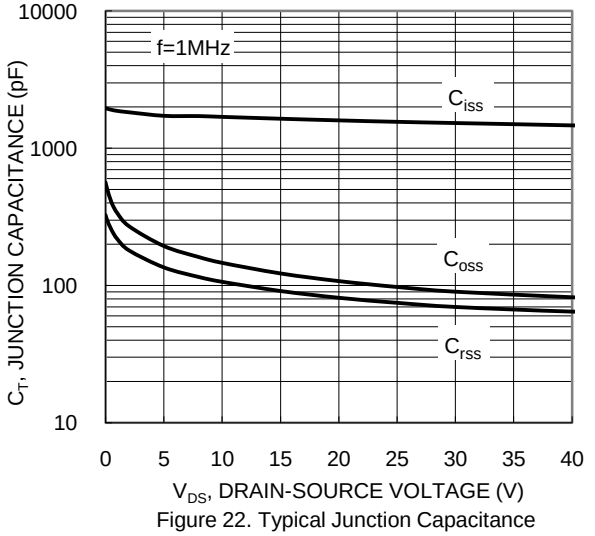


Figure 22. Typical Junction Capacitance

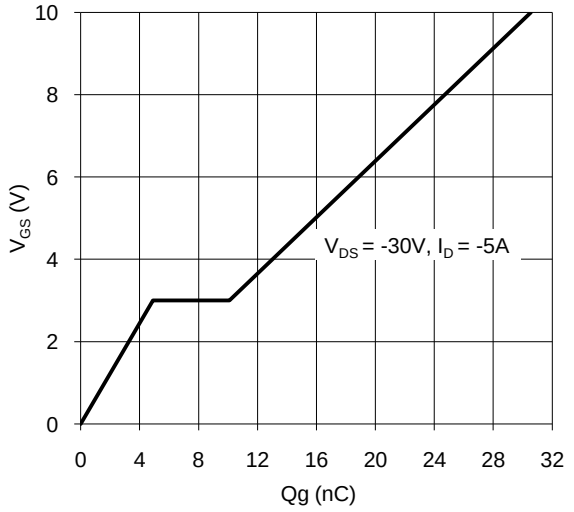


Figure 23. Gate Charge

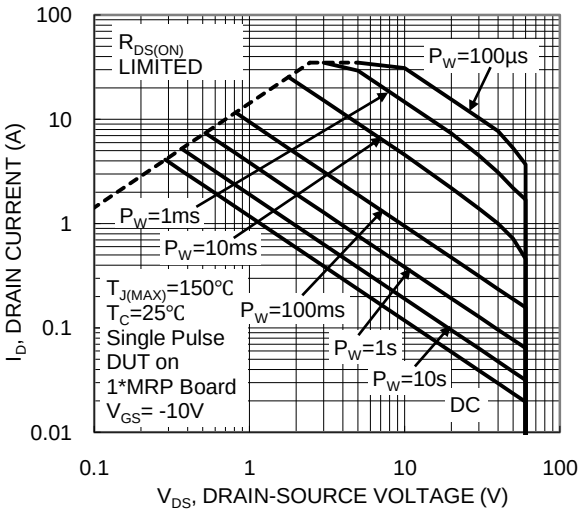


Figure 24. SOA, Safe Operation Area

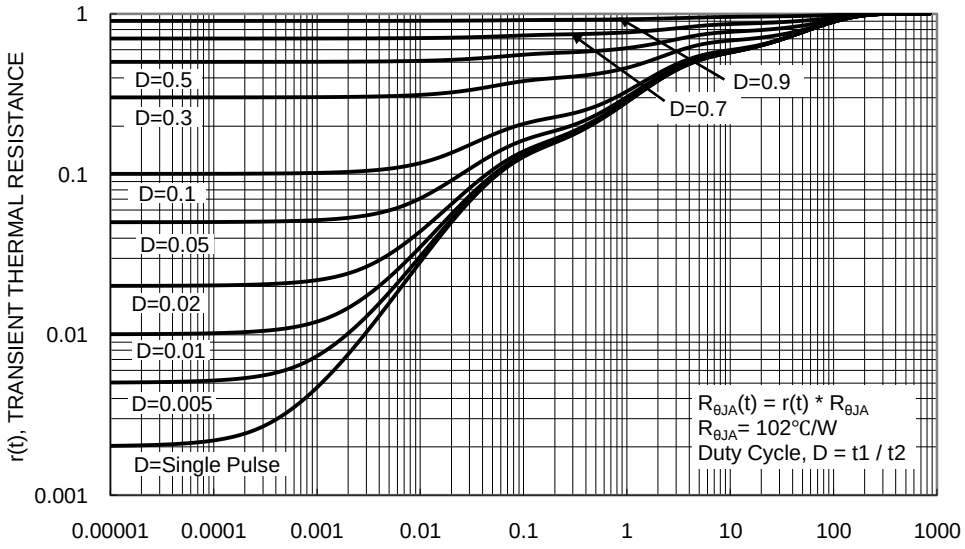
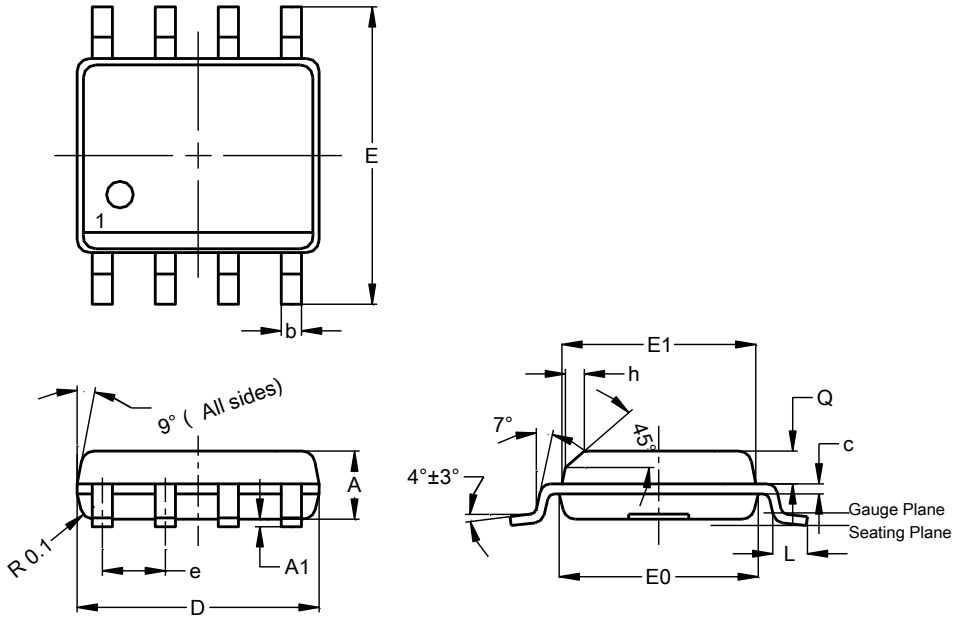


Figure 25. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8

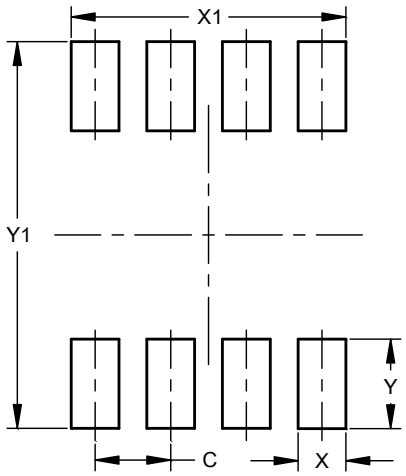


SO-8			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8



Dimensions	Value (in mm)
C	1.27
X	0.802
X1	4.612
Y	1.505
Y1	6.50

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