



COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	V _{(BR)DSS}	R _{DS(ON)}	Ι _D T _A = +25°C
01	Q1 30V	60mΩ @ V _{GS} = 10V	3.4A
QI		100mΩ @ V _{GS} = 4.5V	2.7A
Q2	-30V	95mΩ @ V _{GS} = -10V	-2.8A
Q2	-307	140mΩ @ V _{GS} = -4.5V	-2.3A

Description

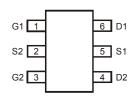
This new generation MOSFET has been designed to minimize the onstate resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Backlighting
- DC-DC Converters
- Power management functions



Top View



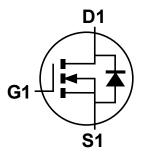
Top View

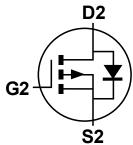
Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: TSOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram
- Terminals: Finish Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 3
- Weight: 0.013 grams (approximate)





Q1 N-Channel MOSFET

Q2 P-Channel MOSFET

Ordering Information (Note 4)

Part Number	Case	Packaging
DMG6602SVTX-7	TSOT26	3000 / Tape & Reel
DMG6602SVTX-13	TSOT26	10000 / Tape & Reel

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.

See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green"

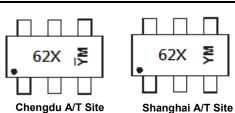
and Lead-free.

Notes:

3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



 $\begin{array}{l} 62X = Product Type Marking Code \\ YM = Date Code Marking for SAT (Shanghai Assembly/ Test site) \\ \overline{YM} = Date Code Marking for CAT (Chengdu Assembly/ Test site) \end{array}$

Y or \overline{Y} = Year (ex: A = 2013)

M = Month (ex: 9 = September

Date	Coue Rey						-					-	
	Year	201	0	2011		2012	20	13	2014		2015		2016
	Code	Х		Y		Z		4	В		С		D
	Month	Jan	Feb	Mar	Apr	Мау	Jun	Jul	Aug	Sep	Oct	Nov	Dec
	Code	1	2	3	4	5	6	7	8	9	0	N	D

Date Code Key



Maximum Ratings – Q1 (@T_A = +25°C, unless otherwise specified.)

Characteristi	Symbol	Value	Unit		
Drain-Source Voltage	V _{DSS}	30	V		
Gate-Source Voltage	V _{GSS}	±20	V		
Continuous Drain Current (Note 5) V_{GS} = 10V	Steady State	T _A = +25°C T _A = +70°C	Ι _D	3.4 2.7	А
Continuous Drain Current (Note 5) V_{GS} = 4.5V	I _D	2.7 2.2	А		
Maximum Continuous Body Diode Forward Curre	Is	1.5	А		
Pulsed Drain Current (Note 6)	I _{DM}	13.0	A		

Maximum Ratings – Q2 ($@T_A = +25^{\circ}C$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage	V _{DSS}	-30	V		
Gate-Source Voltage	V _{GSS}	±20	V		
Continuous Drain Current (Note 5) V_{GS} = -10V	Steady State	T _A = +25°C T _A = +70°C	۱ _D	-2.8 -2.4	А
Continuous Drain Current (Note 5) V_{GS} = -4.5V	۱ _D	-2.3 -2.1	А		
Maximum Continuous Body Diode Forward Curre	Is	-1.5	А		
Pulsed Drain Current (Note 6)	I _D	-11.2	A		

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note5)	PD	1.0	W
Thermal Resistance, Junction to Ambient $@T_A = +25^{\circ}C$ (Note 5)	R _{θJA}	124	°C/W
Operating and Storage Temperature Range	TJ, TSTG	-55 to +150	°C

Electrical Characteristics – Q1 (@T_A = +25°C, unless otherwise specified.)

					•	
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	30		—	V	$V_{GS} = 0V, I_D = 250 \mu A$
Zero Gate Voltage Drain Current	I _{DSS}	—	_	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
Gate-Source Leakage	I _{GSS}	—	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(th)}	0.5	1.2	1.8	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
			35	60		V_{GS} = 10V, I_{D} = 3.1A
Static Drain-Source On-Resistance	R _{DS} (ON)	—	50	100 200	mΩ	V _{GS} = 4.5V, I _D = 2A
			100			V _{GS} = 3.3V, I _D = 1.5A
Forward Transfer Admittance	Y _{fs}	_	4	—	S	V _{DS} = 5V, I _D = 3.1A
Diode Forward Voltage	V _{SD}	_	0.8	1	V	V _{GS} = 0V, I _S = 1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	234			
Output Capacitance	Coss	_	42	_	pF	V _{DS} = 15V, V _{GS} = 0V, f = 1.0MHz
Reverse Transfer Capacitance	Crss	_	40	—		
Gate Resistance	Rg	_	1.45	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (V _{GS} = 4.5V)	Qg	—	3.6	—		V _{DS} = 15V, V _{GS} = 4.5V, I _D = 3A
Total Gate Charge (V _{GS} = 10V)	Qg	_	7.3	—		
Gate-Source Charge	Q _{gs}	—	0.9	—	nC	V _{DS} = 15V, V _{GS} = 10V, I _D = 3A
Gate-Drain Charge	Q _{qd}		1.6	_		
Turn-On Delay Time	t _{D(on)}		3.6	—		
Turn-On Rise Time	tr	—	2.5	—	$V_{GS} = 10V, V_{DS} = 15V,$	
Turn-Off Delay Time	t _{D(off)}		16	—	ns	$R_G = 3\Omega, R_L = 1.7\Omega$
Turn-Off Fall Time	t _f	—	6	—	1	

Notes: 5. Device mounted on FR-4 with minimum recommended pad layout, single sided.

Repetitive rating, pulse width limited by junction temperature.
Short duration pulse test used to minimize self-heating effect.

8. Guaranteed by design. Not subject to production testing.

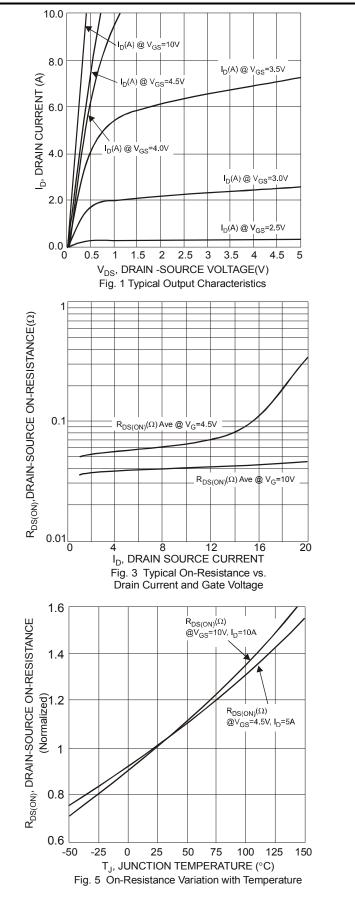


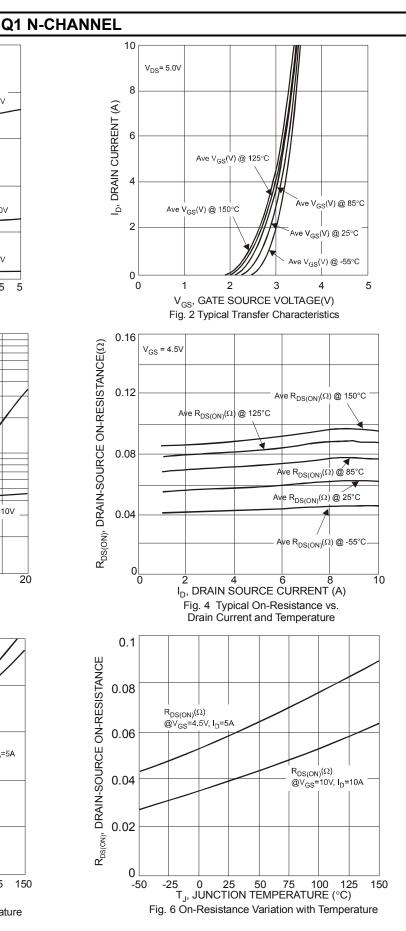
Electrical Characteristics – Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
Zero Gate Voltage Drain Current	I _{DSS}	—	—	-1.0	μA	$V_{DS} = -24V, V_{GS} = 0V$
Gate-Source Leakage	I _{GSS}	_	-	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(th)}	-0.5	-1.5	-2.2	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$
			75	95		V _{GS} = -10V, I _D = -2.7A
Static Drain-Source On-Resistance	R _{DS (ON)}		105	140	mΩ	V _{GS} = -4.5V, I _D = -2A
			140	200		V _{GS} = -3.3V, I _D = -1.5A
Forward Transfer Admittance	Y _{fs}	—	6	_	S	V _{DS} = -5V, I _D = -2.7A
Diode Forward Voltage	V _{SD}	—	-0.8	-1.0	V	V _{GS} = 0V, I _S = -1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iss}	—	410	_		
Output Capacitance	C _{oss}	—	50	—	pF	V _{DS} = -15V, V _{GS} = 0V, f = 1.0MHz
Reverse Transfer Capacitance	C _{rss}	—	45	—		
Gate Resistance	Rg	_	6.2	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (V _{GS} = -4.5V)	Qg	—	3.7	—		V _{DS} = -15V, V _{GS} = -4.5V, I _D = -3A
Total Gate Charge (V _{GS} = -10V)	Qg	—	7.8	—	nC	
Gate-Source Charge	Q _{gs}	—	1.1	—	nc	V _{DS} = -15V, V _{GS} = -10V, I _D = -3A
Gate-Drain Charge	Q _{gd}	_	1.3	—		
Turn-On Delay Time	t _{D(on)}	—	3.3	—		
Turn-On Rise Time	tr	—	3.0	—	20	V _{GS} = -10V, V _{DS} = -15V,
Turn-Off Delay Time	t _{D(off)}	_	14	_	ns	$R_G = 6\Omega, R_L = 15\Omega$
Turn-Off Fall Time	t _f	_	6.8	—		

Notes:7. Short duration pulse test used to minimize self-heating effect.8. Guaranteed by design. Not subject to production testing.

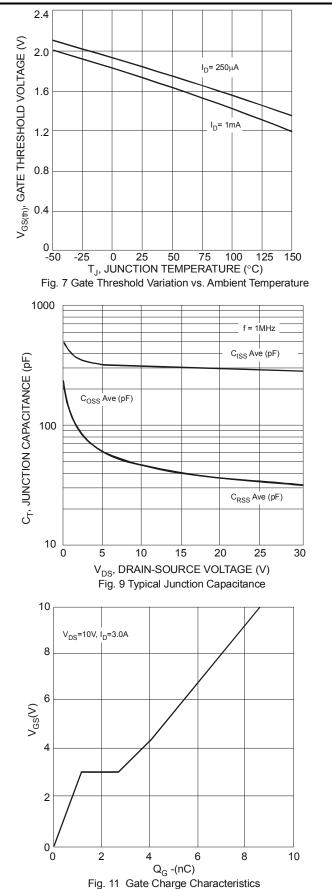




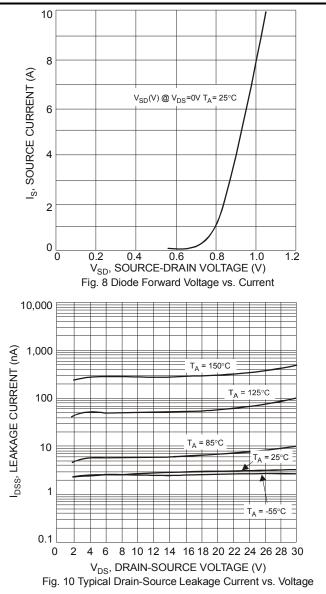


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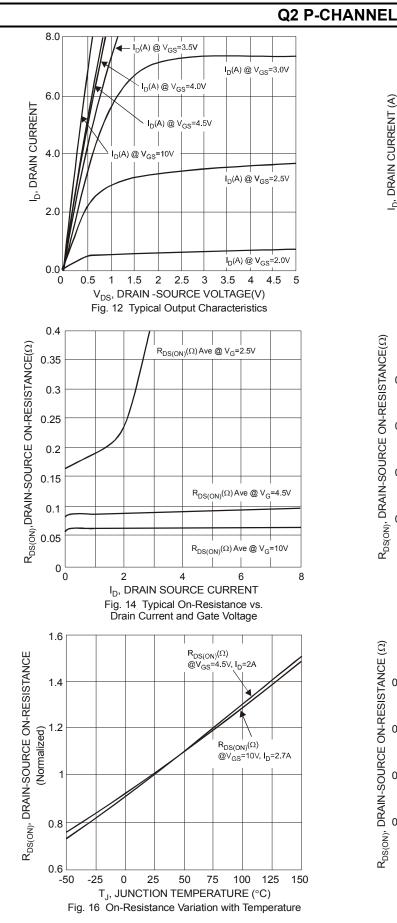




Q1 N-CHANNEL







8 V_{DS}= 5V Ave V_{GS}(V) @ 85°C Ave V_{GS}(V) @ 125°C 6 I_D, DRAIN CURRENT (A) Ave V_{GS}(V) @ 150°C 4 2 /e V_{GS}(V) @ 25°C Ave V_{GS}(V) @ -55°C 0 L 0 0.5 2 2.5 1 1.5 3 3.5 4 4.5 5 V_{GS}, GATE SOURCE VOLTAGE(V) Fig. 13 Typical Transfer Characteristics 0.2 $R_{DS(ON)}$, DRAIN-SOURCE ON-RESISTANCE(Ω) V_{GS}= 4.5V Ave $R_{DS(ON)}(\Omega)$ @ 125°C Ave R_{DS(ON)}(Ω) @ 150°C _ 0.16 0.12 Ave R_{DS(ON)}(Ω) @ 85°C 0.08 Ave R_{DS(ON)}(Ω) @ 25° 0.04 Ave R_{DS(ON)}(Ω) @ -55°C 0 2 4 6 8 0 I_D, DRAIN SOURCE CURRENT (A) Fig. 15 Typical On-Resistance vs. Drain Current and Temperature 0.2 $R_{\text{DS}(\text{ON})}$, DRAIN-SOURCE ON-RESISTANCE (Ω) $R_{DS(ON)}(\Omega)$ @V_{GS}=4.5V, I_D=2A 0.16 0.12 0.08 R_{DS(ON)}(Ω) @V_{GS}=10V, I_D=2.7A 0.04 0 -50 -25 0 25 50 75 100 125 150 T_., JUNCTION TEMPERATURE (°C)

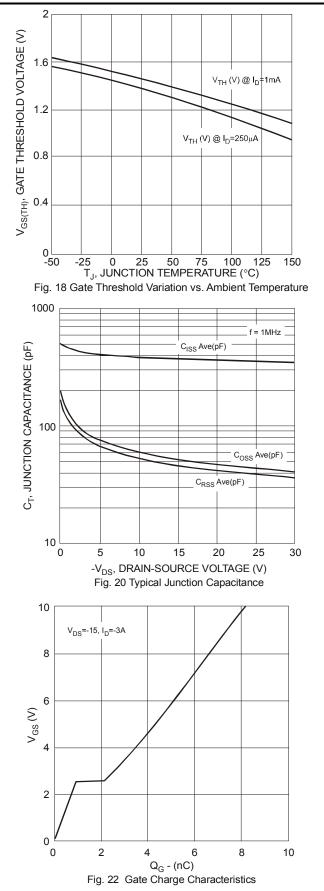
Fig. 17 On-Resistance Variation with Temperature

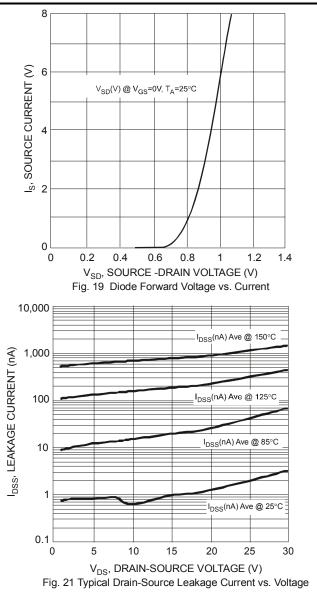
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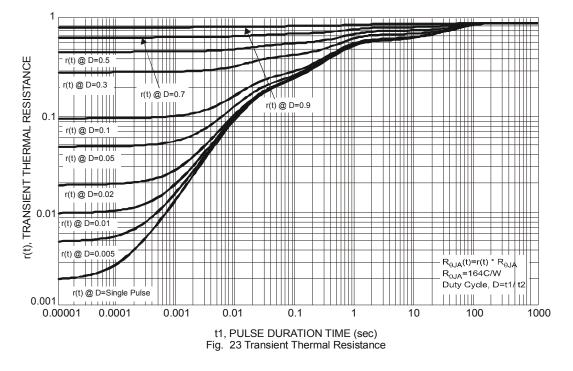


Q2 P-CHANNEL



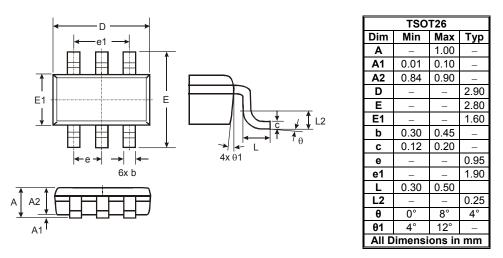






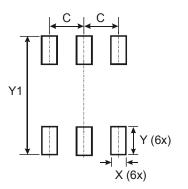
Package Outline Dimensions

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.



Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
С	0.950
Х	0.700
Y	1.000
Y1	3.199

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