



### 20V N-CHANNEL ENHANCEMENT MODE MOSFET PowerDI3333-8

## **Product Summary**

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> Max T <sub>C</sub> = +25°C (Note 9)		
20V	$4.6 \text{m}\Omega$ @ $V_{GS} = 4.5 \text{V}$	50A		
201	$8.7 \text{m}\Omega$ @ $V_{GS} = 2.5 \text{V}$	36A		

## **Description**

This MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

## **Applications**

- Backlighting
- **Power Management Functions**
- **DC-DC Converters**

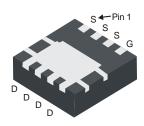
## **Features and Benefits**

- Low R<sub>DS(ON)</sub> ensures on state losses are minimized
- Small form factor thermally efficient package enables higher density end products
- Occupies just 33% of the board area occupied by SO-8 enabling smaller end product
- 100% UIS & Rg tested
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability
- An Automotive-Compliant Part is Available Under Separate Datasheet (DMN2005UFGQ)

#### **Mechanical Data**

- Case: PowerDI®3333-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 @3
- Weight: 0.072 grams (Approximate)

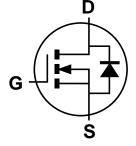
PowerDI3333-8



**Bottom View** 



Top View



**Equivalent Circuit** 

### **Ordering Information** (Note 4)

Part Number	Case	Packaging		
DMN2005UFG-7	PowerDI3333-8	2,000/Tape & Reel		
DMN2005UFG-13	PowerDI3333-8	3,000/Tape & Reel		

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.

- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/

## **Marking Information**



N05= Product Type Marking Code YYWW = Date Code Marking YY = Last Two Digits of Year (ex: 19 = 2019) WW = Week Code (01 to 53)



# 

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage	$V_{DSS}$	20	V		
Gate-Source Voltage	V <sub>GSS</sub>	±12	V		
Continuous Preis Correct (Notes C. 9. O.) V. 4. EV.	Steady State	$T_C = +25$ °C $T_C = +70$ °C	I <sub>D</sub>	50 40	А
Continuous Drain Current (Notes 6 & 9) V <sub>GS</sub> = 4.5V		$T_A = +25$ °C $T_A = +70$ °C	I <sub>D</sub>	18 14	А
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	130	Α		
Maximum Continuous Body Diode Forward Current (N	Is	2.6	Α		
Avalanche Current , L = 0.2mH	I <sub>AS</sub>	23.9	Α		
Repetitive Avalanche Energy, L = 0.2mH	E <sub>AS</sub>	58.4	mJ		

## Thermal Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Total Power Dissipation (Note 5)	T <sub>A</sub> = +25°C	P <sub>D</sub>	1.05	W
Thermal Resistance, Junction to Ambient (Note 5)  Steady State		$R_{\theta JA}$	120	°C/W
Total Power Dissipation (Note 6) $T_A = +25$ °C		P <sub>D</sub>	2.27	W
Thermal Resistance, Junction to Ambient (Note 6)  Steady State		$R_{\theta JA}$	55	°C/W
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	4.2	C/VV
Operating and Storage Temperature Range	T <sub>J,</sub> T <sub>STG</sub>	-55 to +150	°C	

Notes: 5.

<sup>5.</sup> Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.

<sup>6.</sup> Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.

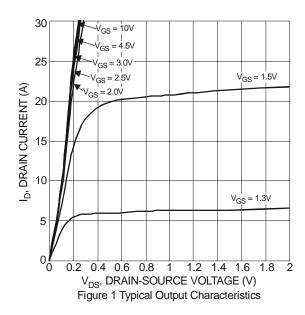


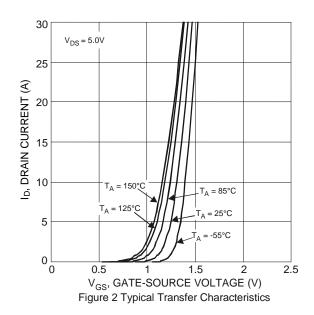
## Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	20	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C		_	_	10	μA	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V	
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±100	nA	$V_{GS} = \pm 12V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	$V_{GS(TH)}$	0.4	0.7	1.2	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
Static Drain-Source On-Resistance	,	_	4	4.6	0	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 13.5A	
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	_	4.9	8.7	mΩ	V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 13.5A	
Diode Forward Voltage	V <sub>SD</sub>	_	0.8	1.1	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 27A	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	C <sub>iss</sub>	_	6,495	_	pF		
Output Capacitance	Coss	_	546	_	pF	$V_{DS} = 10V, V_{GS} = 0V,$ f = 1MHz	
Reverse Transfer Capacitance	C <sub>rss</sub>	_	477	_	pF	TI = TIVITZ	
Gate Resistance	Rg	_	0.7	_	Ω	$V_{DS} = 0V$ , $V_{GS} = 0V$ , $f = 1MHz$	
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Qg	_	68.8	_	nC		
Total Gate Charge (V <sub>GS</sub> = 10V)	Qg	_	164	_	nC	101/1 074	
Gate-Source Charge	Q <sub>gs</sub>	_	10.4	_	nC	$V_{DS} = 16V, I_D = 27A$	
Gate-Drain Charge	Q <sub>gd</sub>	_	17.4	_	nC		
Turn-On Delay Time	t <sub>D(ON)</sub>	1	12.4	_	ns		
Turn-On Rise Time	t <sub>R</sub>	1	25.7	_	ns	$V_{GS} = 5V, V_{DS} = 10V,$ $R_{G} = 4.7\Omega, I_{D} = 13.5A$	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	1	114	_	ns		
Turn-Off Fall Time	t <sub>F</sub>	_	38	_	ns		
Body Diode Reverse Recovery Time	t <sub>RR</sub>		16.1	_	ns	$I_F = 13.5A$ , $di/dt = 100A/\mu s$	
Body Diode Reverse Recovery Charge	$Q_{RR}$		8.5	_	nC	$I_F = 13.5A$ , $di/dt = 100A/\mu s$	

Notes:

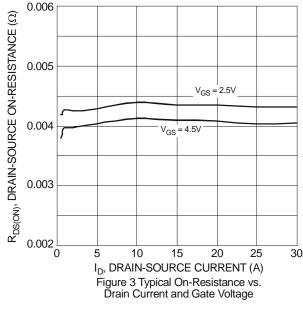
- 7. Short duration pulse test used to minimize self-heating effect. 8. Guaranteed by design. Not subject to product testing.
- 9. Limited by package.

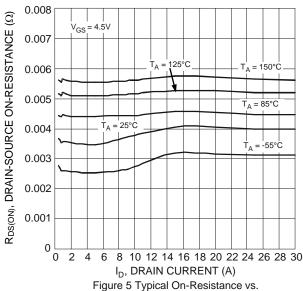


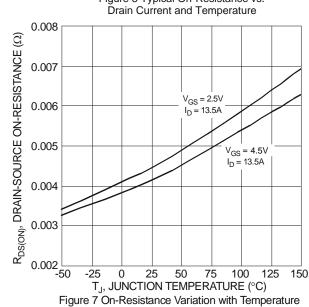


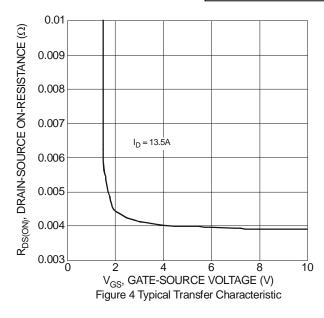












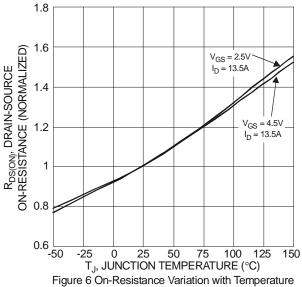
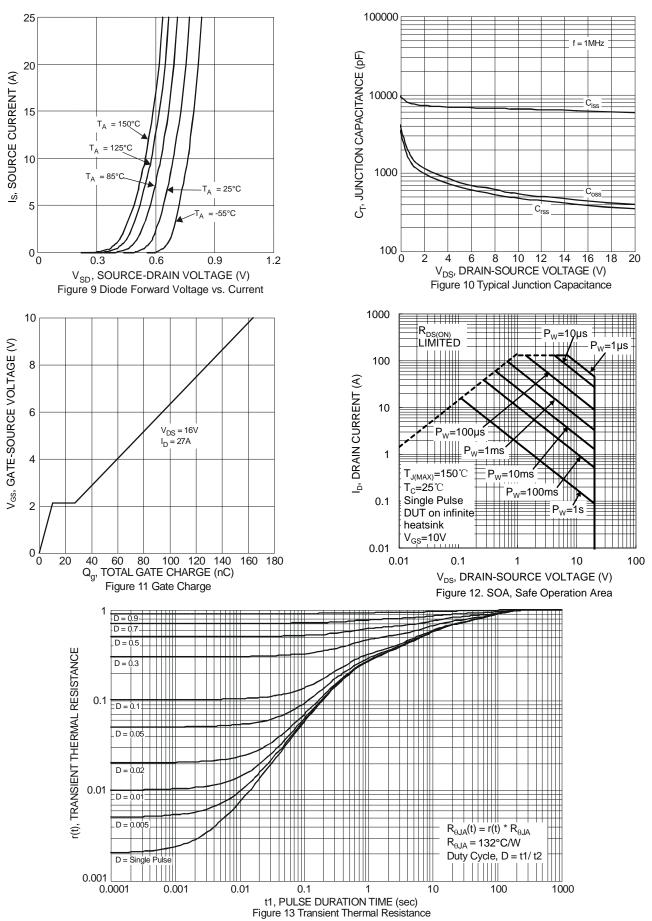


Figure 8 Gate Threshold Variation vs. Junction Temperature



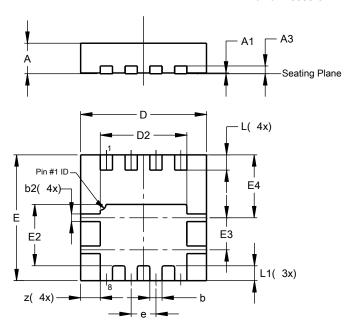




## **Package Outline Dimensions**

Please see http://www.diodes.com/package-outlines.html for the latest version.

#### PowerDI3333-8

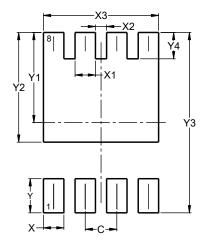


PowerDI3333-8						
Dim	Min	Max	Тур			
Α	0.75	0.85	0.80			
A1	0.00	0.05	0.02			
A3	_	_	0.203			
b	0.27	0.37	0.32			
b2	0.15	0.25	0.20			
D	3.25	3.35	3.30			
D2	2.22	2.32	2.27			
E	3.25	3.35	3.30			
E2	1.56	1.66	1.61			
E3	0.79	0.89	0.84			
E4	1.60	1.70	1.65			
е	_	_	0.65			
L	0.35	0.45	0.40			
L1	_	_	0.39			
Z	_	_	0.515			
All Dimensions in mm						

## **Suggested Pad Layout**

Please see http://www.diodes.com/package-outlines.html for the latest version.

#### PowerDI3333-8



Dimensions	Value (in mm)
C	0.650
Х	0.420
X1	0.420
X2	0.230
Х3	2.370
Υ	0.700
Y1	1.850
Y2	2.250
Y3	3.700
Υ4	0.540

March 2019

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