



#### 30V DUAL N-CHANNEL ENHANCEMENT MODE MOSFET

#### **Product Summary**

V <sub>(BR)DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub> T <sub>A</sub> = +25°C
30V	$15m\Omega$ @ $V_{GS}$ = $10V$	8.4A
	$18m\Omega$ @ $V_{GS} = 4.5V$	7.7A

#### **Description**

This new generation MOSFET has been designed to minimize the onstate resistance ( $R_{DS(ON)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

### **Applications**

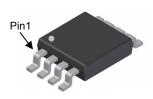
- DC-DC Converters
- Power Management Functions
- Backlighting

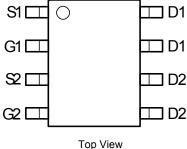
### **Features and Benefits**

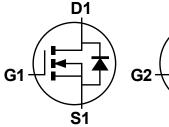
- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

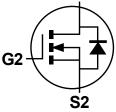
#### **Mechanical Data**

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound.
   UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish Tin Finish annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.074 grams (approximate)









**D2** 

Top View

Pin Configuration

**Equivalent Circuit** 

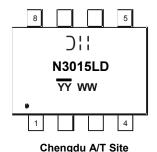
### Ordering Information (Note 4)

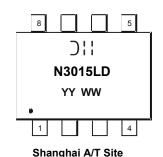
1			
	Part Number	Case	Packaging
	DMN3015LSD-13	SO-8	2,500/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

## Marking Information





);; = Manufacturer's Marking
N3015LD = Product Type Marking Code
YYWW = Date Code Marking
YY or YY = Year (ex: 14 = 2014)
WW = Week (01 - 53)

YY = Date Code Marking for SAT (Shanghai Assembly/ Test site)
YY = Date Code Marking for CAT (Chengdu Assembly/ Test site)



## **Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units		
Drain-Source Voltage	$V_{DSS}$	30	V		
Gate-Source Voltage	$V_{GSS}$	±20	V		
Continuous Drain Correct (Note CVV - 40V	Steady State	T <sub>A</sub> = +25°C T <sub>A</sub> = +70°C	I <sub>D</sub>	8.4 6.8	А
Continuous Drain Current (Note 6) V <sub>GS</sub> = 10V	t<10s	T <sub>A</sub> = +25°C T <sub>A</sub> = +70°C	I <sub>D</sub>	11.0 9.0	А
Maximum Body Diode Forward Current (Note 6)	Is	2.5	Α		
Pulsed Drain Current (10µs pulse, duty cycle = 1%)	I <sub>DM</sub>	80	Α		
Avalanche Current (Notes 7) L = 0.1mH	I <sub>AS</sub>	22	Α		
Avalanche Energy (Notes 7) L = 0.1mH	E <sub>AS</sub>	25	mJ		

# Thermal Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units	
Total Power Dissipation (Note 5)	T <sub>A</sub> = +25°C	$P_{D}$	1.2	W
Total Power Dissipation (Note 5)	T <sub>A</sub> = +70°C	PD	0.8	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	D	102	°C/W
Thermal Resistance, Junction to Ambient (Note 5)	t<10s	$R_{\theta JA}$	62	
Total Power Dissipation (Note 6)	$T_A = +25^{\circ}C$	D-	1.6	W
Total Power Dissipation (Note 6)	$T_A = +70^{\circ}C$	P <sub>D</sub>	1.0	
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	C	78	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	t<10s	$R_{\theta JA}$	47	
Thermal Resistance, Junction to Case (Note 6)	_	$R_{ heta JC}$	14.5	
Operating and Storage Temperature Range		T <sub>J,</sub> T <sub>STG</sub>	-55 to +150	°C

## **Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	30	_	_	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_	_	1	μΑ	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	1.3	_	2.5	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
Static Drain-Source On-Resistance			8	15	0	V <sub>GS</sub> = 10V, I <sub>D</sub> = 12A
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	_	12	18	mΩ	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10A
Diode Forward Voltage	V <sub>SD</sub>	_	0.7	1.0	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 1A
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C <sub>iss</sub>		1415			V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	Coss	_	119	_	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	_	82	_		
Gate Resistance	R <sub>G</sub>	_	2.6	3.2	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Qg		11.3	_		
Total Gate Charge (V <sub>GS</sub> = 10V)	Qg		25.1	_		45)(1 40)
Gate-Source Charge	Qgs		3.5	_	nC	V <sub>DS</sub> = 15V, I <sub>D</sub> = 12A
Gate-Drain Charge	$Q_{gd}$		3.6	_		
Turn-On Delay Time	t <sub>D(on)</sub>		4.8	_		
Turn-On Rise Time	t <sub>r</sub>		16.5	_	0	$V_{DD} = 15V, V_{GS} = 10V,$
Turn-Off Delay Time	t <sub>D(off)</sub>	_	26.1	_	nS	$R_L = 1.25\Omega$ , $R_G = 3\Omega$ ,
Turn-Off Fall Time	t <sub>f</sub>		5.6	_		
Body Diode Reverse Recovery Time	t <sub>rr</sub>		8.5	_	nS	I <sub>S</sub> = 12A, dI/dt = 500A/μs
Body Diode Reverse Recovery Charge	Qrr		7.0	_	nC	I <sub>S</sub> = 12A, dI/dt = 500A/μs

lotes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

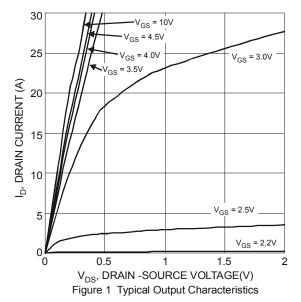
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

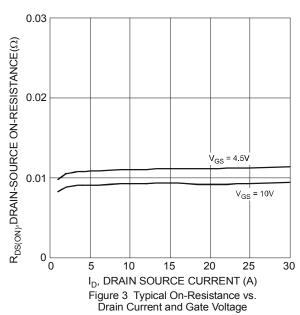
7. UIS in production with L = 0.1mH, starting  $T_A$  = +25°C.

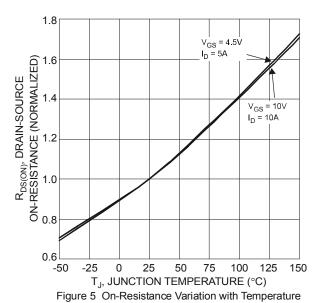
8. Short duration pulse test used to minimize self-heating effect.

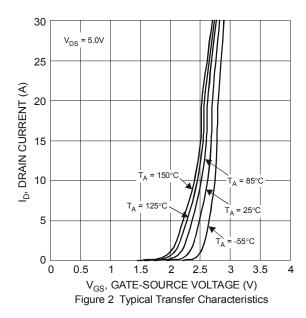
9. Guaranteed by design. Not subject to product testing.

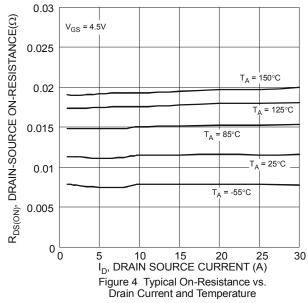


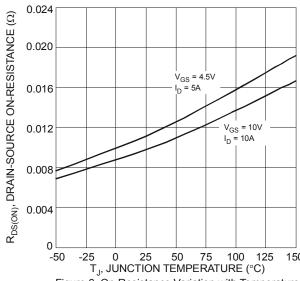














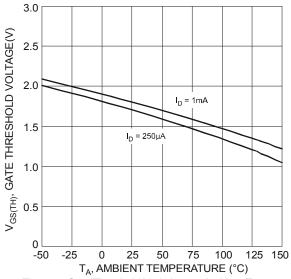
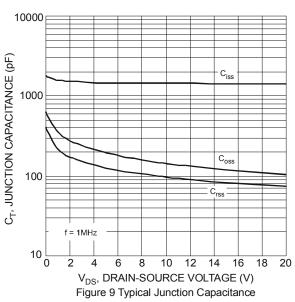
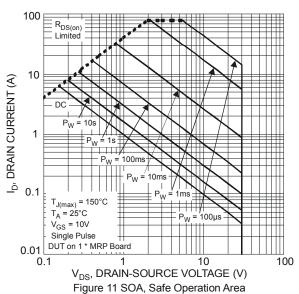
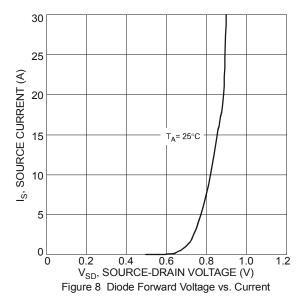
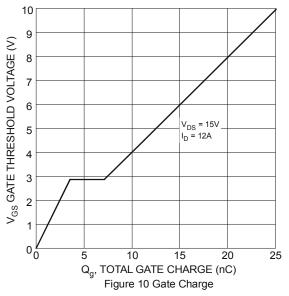


Figure 7 Gate Threshold Variation vs. Ambient Temperature

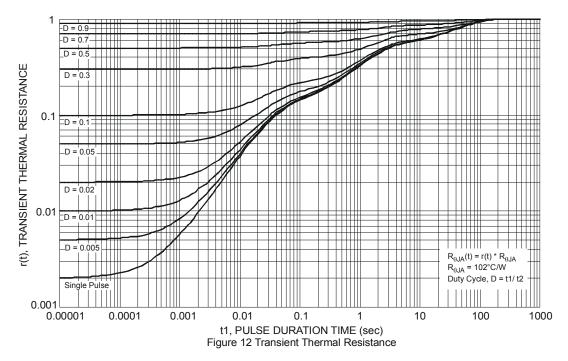






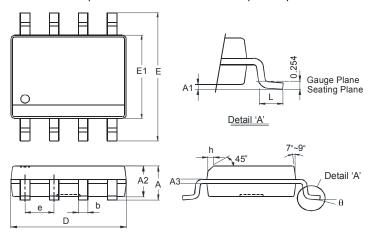






## **Package Outline Dimensions**

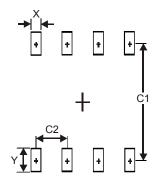
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



SO-8					
Dim	Min	Max			
Α	-	1.75			
A1	0.10	0.20			
A2	1.30	1.50			
A3	0.15	0.25			
b	0.3	0.5			
D	4.85	4.95			
Е	5.90	6.10			
E1	3.95				
е	e 1.27 Typ				
h	-	0.35			
L	0.62	0.82			
θ	0°	8°			
All Dimensions in mm					

## **Suggested Pad Layout**

 $Please see AP02001 \ at \ http://www.diodes.com/datasheets/ap02001.pdf \ for \ the \ latest \ version.$ 



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27



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