

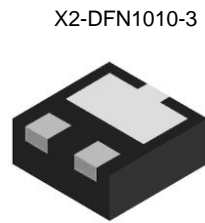
Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D $T_A = +25^\circ C$
30V	65m Ω @ $V_{GS} = 10V$	3.4A
	75m Ω @ $V_{GS} = 4.5V$	3.0A

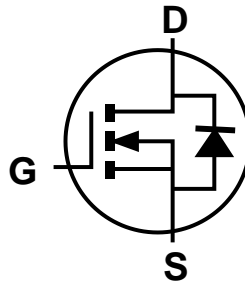
Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

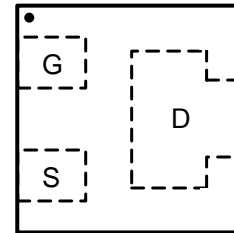
- Power Management Functions
- Backlighting
- Load Switch



Bottom View



Equivalent Circuit



Pin-out Top View

Features and Benefits

- Low On-Resistance
- Low Input/Output Leakage
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

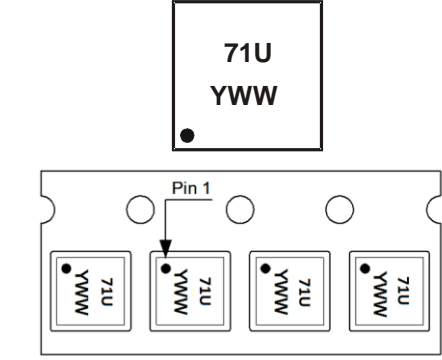
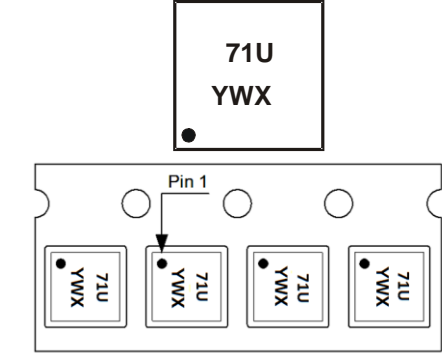
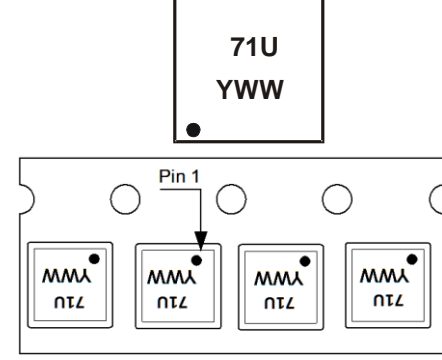
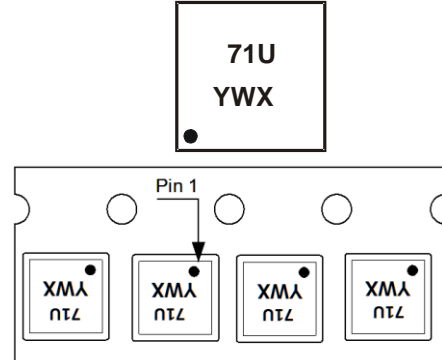
- Case: X2-DFN1010-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish — NiPdAu over Copper Leadframe; Solderable per MIL-STD-202, Method 208 **e4**
- Weight: 0.0015 Grams (Approximate)

Ordering Information (Note 4)

Part Number	Case	Tape Width (mm)	Tape Pitch (mm)	Packaging
DMN3071LFR4-7	X2-DFN1010-3	8	4	3000/Tape & Reel
DMN3071LFR4-7R	X2-DFN1010-3	8	4	3000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

<p>DMN3071LFR4-7</p>	<p>Site 1:</p>  <p>71U = Product Type Marking Code YWW = Date Code Marking Y = Year (ex: G = 2019) WW = Number of Week</p> <p>Site 2:</p>  <p>71U = Product Type Marking Code YWX = Date Code Marking Y = Year (ex: 9 = 2019) W = Week (ex: a = week 27; z represents week 52 and 53) X = Internal Code (ex: U = Monday)</p>
<p>DMN3071LFR4-7R</p>	<p>Site 1:</p>  <p>71U = Product Type Marking Code YWW = Date Code Marking Y = Year (ex: G = 2019) WW = Number of Week</p> <p>Site 2:</p>  <p>71U = Product Type Marking Code YWX = Date Code Marking Y = Year (ex: 9 = 2019) W = Week (ex: a = week 27; z represents week 52 and 53) X = Internal Code (ex: U = Monday)</p>

Marking Information (Cont.)

Site 1:

Year	2018	2019	2020	2021	2022	2023	2024	2025
Code	F	G	H	I	J	K	L	M

Site 2:

Year	2018	2019	2020	2021	2022	2023	2024	2025
Code	8	9	0	1	2	3	4	5

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	30	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current (Note 6) V _{GS} = 10V	Steady State	T _A = +25°C T _A = +100°C	I _D	3.4 2.7	A
Maximum Continuous Body Diode Forward Current (Note 6)			I _S	1.5	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I _{DM}	15	A

Thermal Characteristics

Characteristic			Symbol	Value	Unit
Total Power Dissipation (Note 5)			P _D	0.5	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State		R _{θJA}	221	°C/W
Total Power Dissipation (Note 6)			P _D	1.1	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State		R _{θJA}	107	°C/W
Operating and Storage Temperature Range			T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	30	—	—	V	V _{GS} = 0V, I _D = 250µA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	µA	V _{DS} = 30V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	1.0	—	2.5	V	V _{DS} = V _{GS} , I _D = 250µA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	—	65 75	mΩ	V _{GS} = 10V, I _D = 3.2A V _{GS} = 4.5V, I _D = 3.2A
Diode Forward Voltage	V _{SD}	—	0.8	1.2	V	V _{GS} = 0V, I _S = 1A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iSS}	—	190	—	pF	V _{DS} = 15V, V _{GS} = 0V f = 1.0MHz
Output Capacitance	C _{oss}	—	36	—		
Reverse Transfer Capacitance	C _{rSS}	—	26	—		
Gate Resistance	R _g	—	4.2	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (V _{GS} = 4.5V)	Q _g	—	2.1	—	nC	V _{DS} = 15V, I _D = 4A
Total Gate Charge (V _{GS} = 10V)	Q _g	—	4.5	—		
Gate-Source Charge	Q _{gs}	—	0.5	—		
Gate-Drain Charge	Q _{gd}	—	0.8	—		
Turn-On Delay Time	t _{D(ON)}	—	1.7	—	ns	V _{DS} = 15V, V _{GS} = 10V, R _G = 3Ω, I _D = 4A
Turn-On Rise Time	t _R	—	5.7	—		
Turn-Off Delay Time	t _{D(OFF)}	—	6.0	—		
Turn-Off Fall Time	t _F	—	1.6	—		
Reverse Recovery Time	t _{RR}	—	4.2	—	ns	I _F = 4A, di/dt = 100A/µs
Reverse Recovery Charge	Q _{RR}	—	0.5	—	nC	

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on 1" x 1" FR-4 PCB with high coverage 2oz. Copper, single sided.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to production testing.

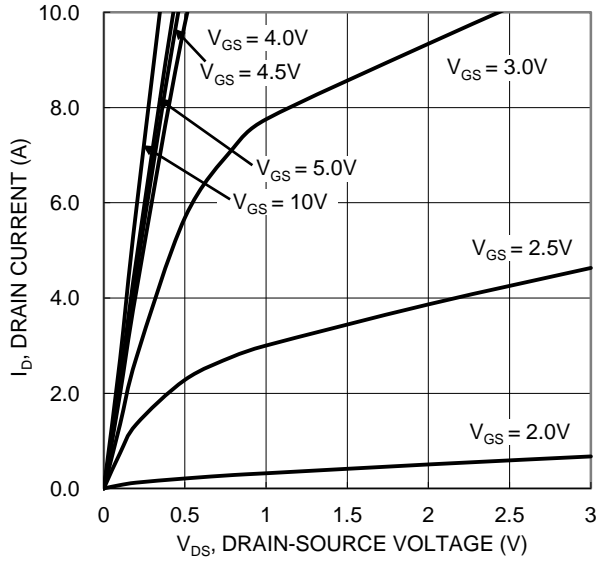


Figure 1. Typical Output Characteristic

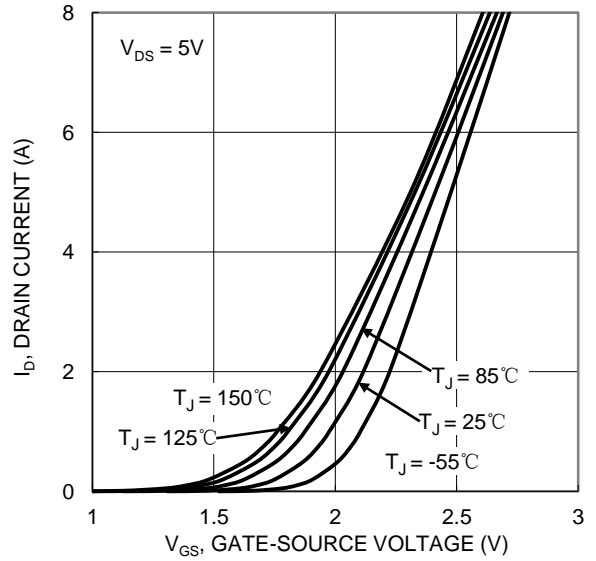


Figure 2. Typical Transfer Characteristic

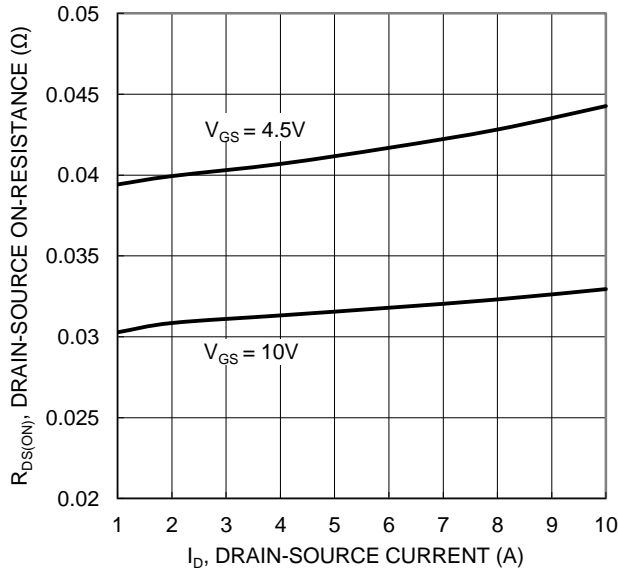


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

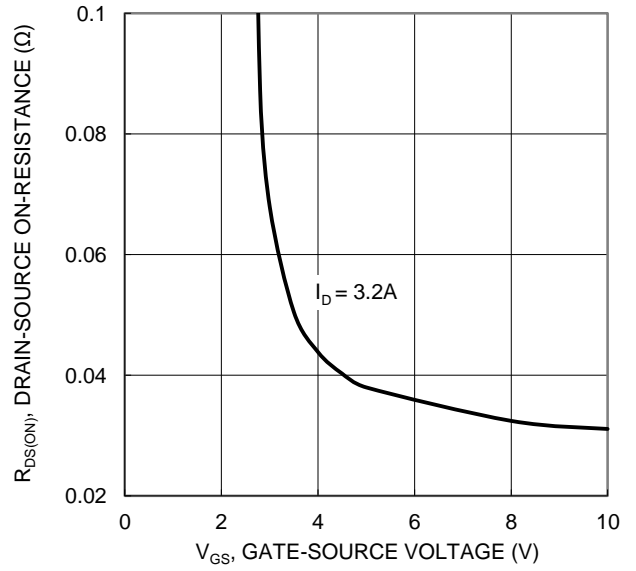


Figure 4. Typical Transfer Characteristic

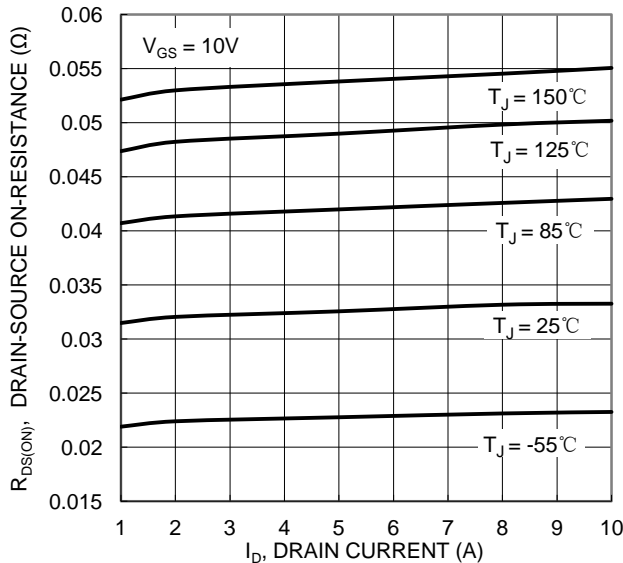


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

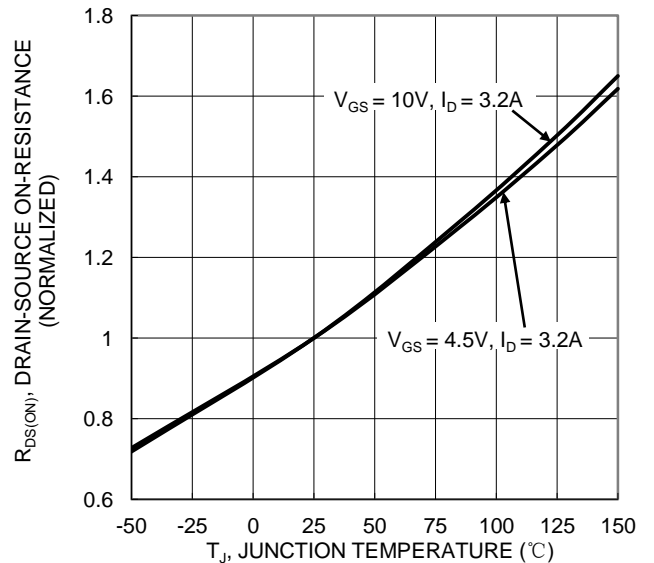


Figure 6. On-Resistance Variation with Junction Temperature

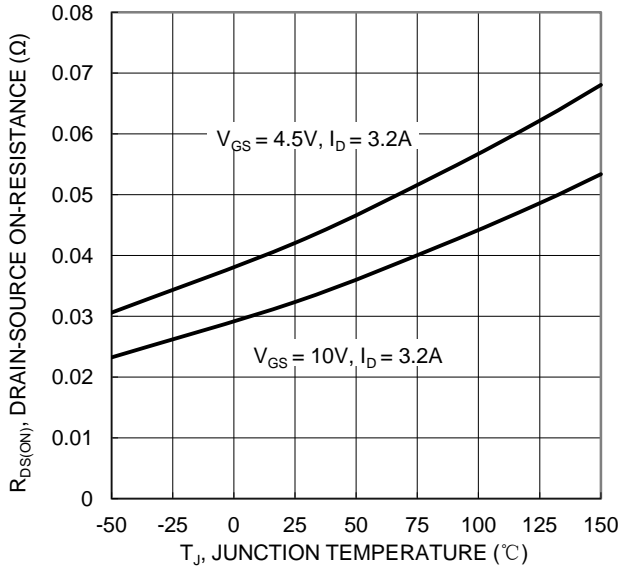


Figure 7. On-Resistance Variation with Junction Temperature

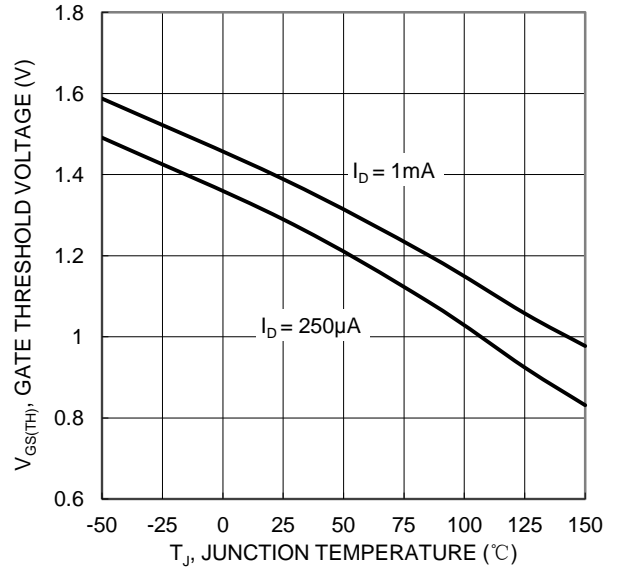


Figure 8. Gate Threshold Variation vs. Junction Temperature

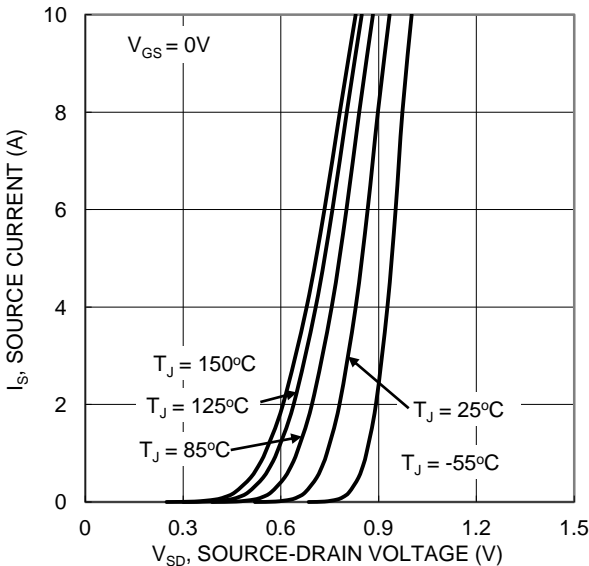


Figure 9. Diode Forward Voltage vs. Current

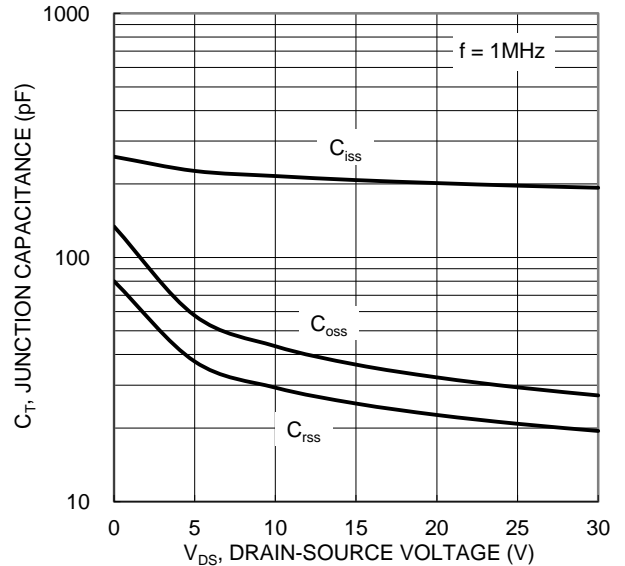


Figure 10. Typical Junction Capacitance

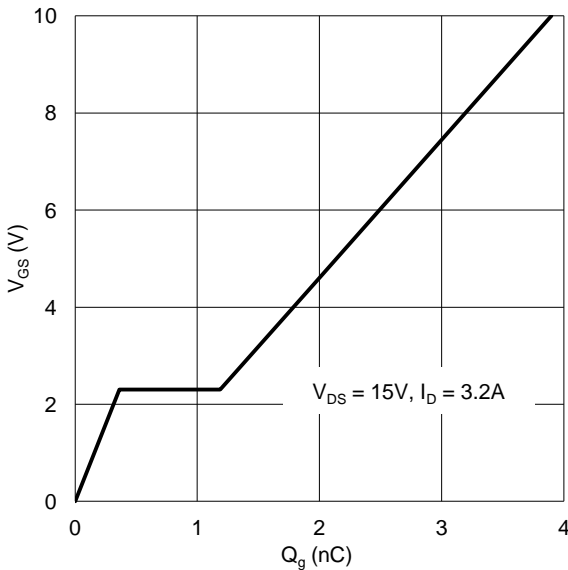


Figure 11. Gate Charge

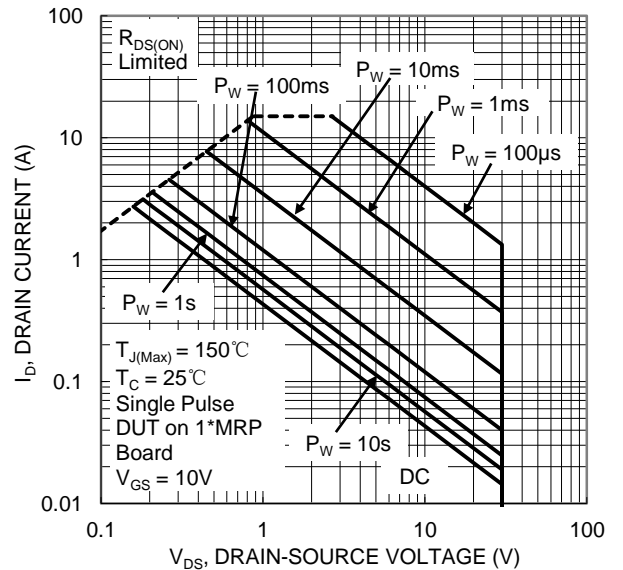


Figure 12. SOA, Safe Operation Area

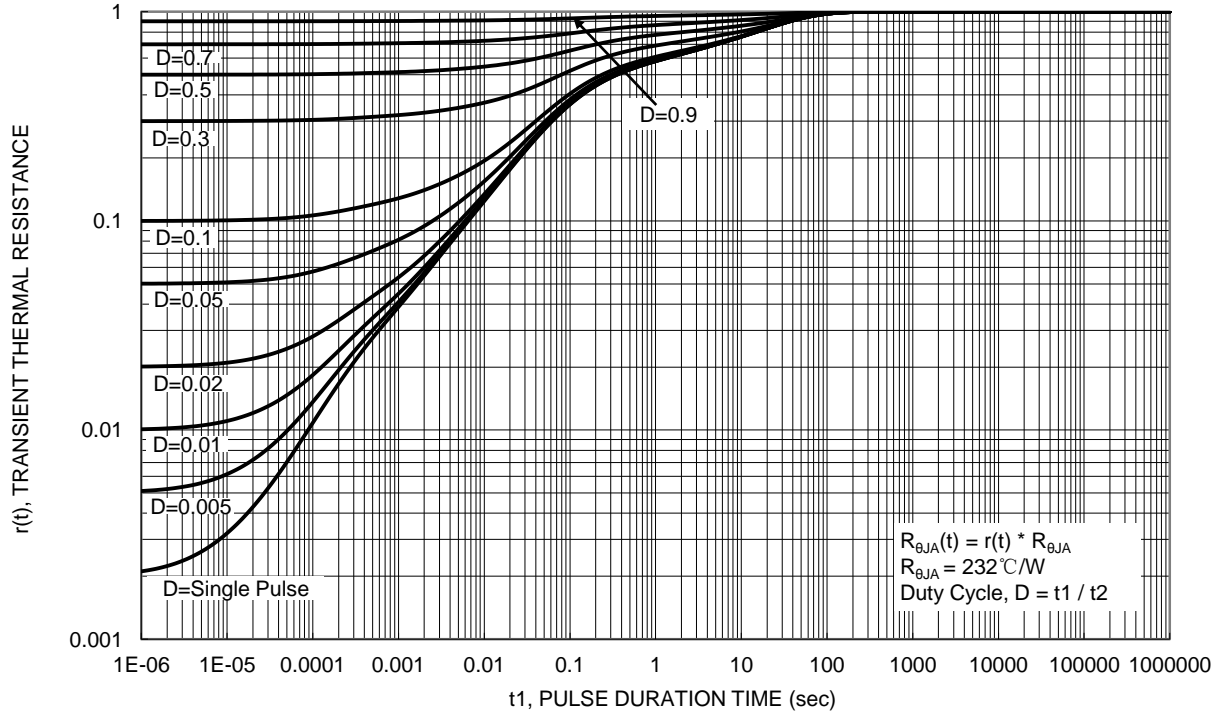
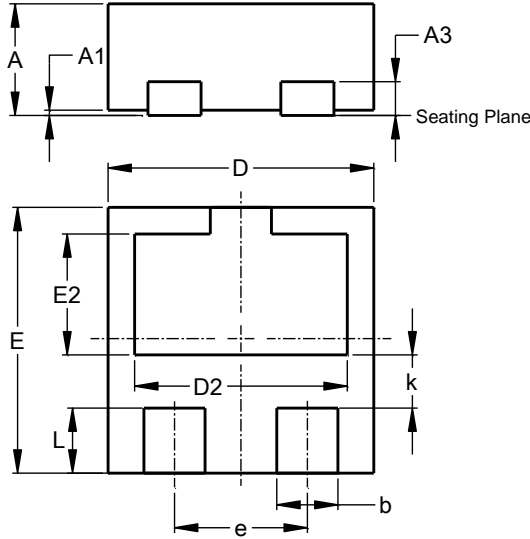


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DFN1010-3

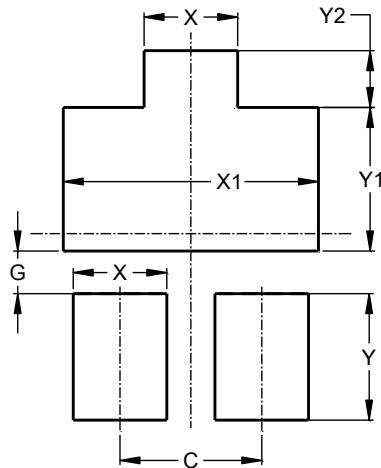


X2-DFN1010-3			
Dim	Min	Max	Typ
A	-	0.40	0.39
A1	0.00	0.05	0.02
A3	-	-	0.13
b	0.18	0.28	0.23
D	0.95	1.05	1.00
D2	0.70	0.90	0.80
E	0.95	1.05	1.00
E2	0.36	0.56	0.46
e	-	-	0.50
k	-	-	0.20
L	0.195	0.295	0.245
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DFN1010-3



Dimensions	Value (in mm)
C	0.500
G	0.150
X	0.330
X1	0.900
Y	0.445
Y1	0.505
Y2	0.200

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