

## Product Summary

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX @ T <sub>A</sub> = +25°C
-20V	495mΩ @ V <sub>GS</sub> = -4.5V	-0.77A
	690mΩ @ V <sub>GS</sub> = -2.5V	-0.67A
	960mΩ @ V <sub>GS</sub> = -1.8V	-0.57A

## Description and Applications

This MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Portable Electronics

## Features and Benefits

- Footprint of just 0.6mm<sup>2</sup> – 13 Times Smaller than SOT23
- 0.4mm Profile – Ideal for Low Profile Applications
- Low Gate Threshold Voltage
- Fast Switching Speed
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative. <https://www.diodes.com/quality/product-definitions/>**

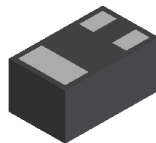
## Mechanical Data

- Case: X2-DFN1006-3
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 @4
- Weight: 0.001 grams (Approximate)

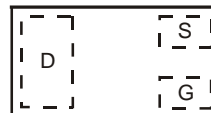


ESD PROTECTED

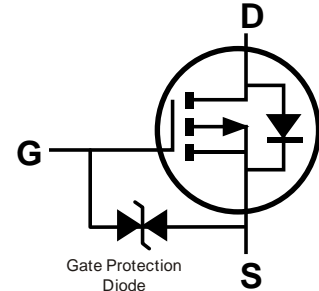
X2-DFN1006-3



Bottom View



Top View  
Internal Schematic



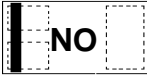
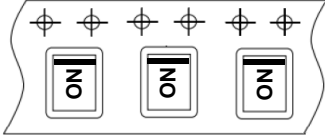
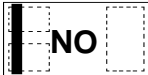
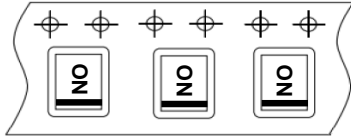
Equivalent Circuit

## Ordering Information (Note 4)

Part Number	Marking	Reel Size (inches)	Tape Width (mm)	Tape Pitch (mm)	Quantity per Reel
DMP21D0UFB4-7R	NO	7	8	4	3,000
DMP21D0UFB4-7B	NO	7	8	2	10,000

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

**Marking Information**

<p>DMP21D0UFB4-7R</p>	<div style="text-align: center;">  <p>Top View Bar Denotes Gate and Source Side</p> </div> <div style="text-align: center;">  </div> <div style="text-align: right; margin-top: 20px;"> <p>NO = Part Marking Code</p> </div>
<p>DMP21D0UFB4-7B</p>	<div style="text-align: center;">  <p>Top View Bar Denotes Gate and Source Side</p> </div> <div style="text-align: center;">  </div> <div style="text-align: right; margin-top: 20px;"> <p>NO = Part Marking Code</p> </div>

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V <sub>DSS</sub>	-20	V
Gate-Source Voltage		V <sub>GSS</sub>	±8	V
Continuous Drain Current	Steady State	I <sub>D</sub>	T <sub>A</sub> = +25°C (Note 5)	-0.77
			T <sub>A</sub> = +85°C (Note 5)	-0.55
			T <sub>A</sub> = +25°C (Note 6)	-1.17
Pulsed Drain Current (Note 7)		I <sub>DM</sub>	-5.0	A

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P <sub>D</sub>	0.43	W
Power Dissipation (Note 6)	P <sub>D</sub>	0.99	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	293	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	R <sub>θJA</sub>	126	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

- Notes:
- 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  - 6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1 inch square copper plate.
  - 7. Device mounted on minimum recommended pad layout test board, 10µs pulse duty cycle = 1%.

**Thermal Characteristics**

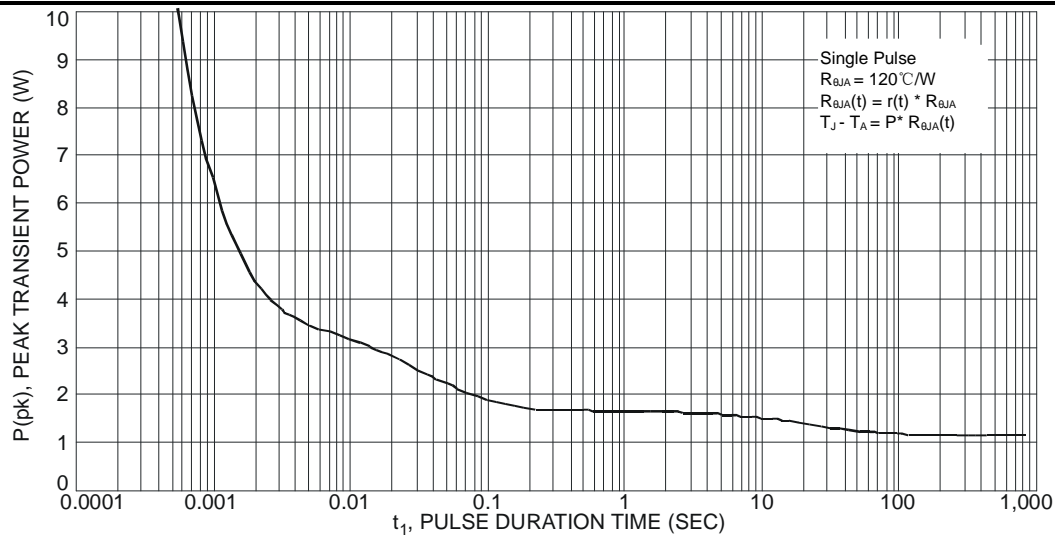


Fig. 1 Single Pulse Maximum Power Dissipation

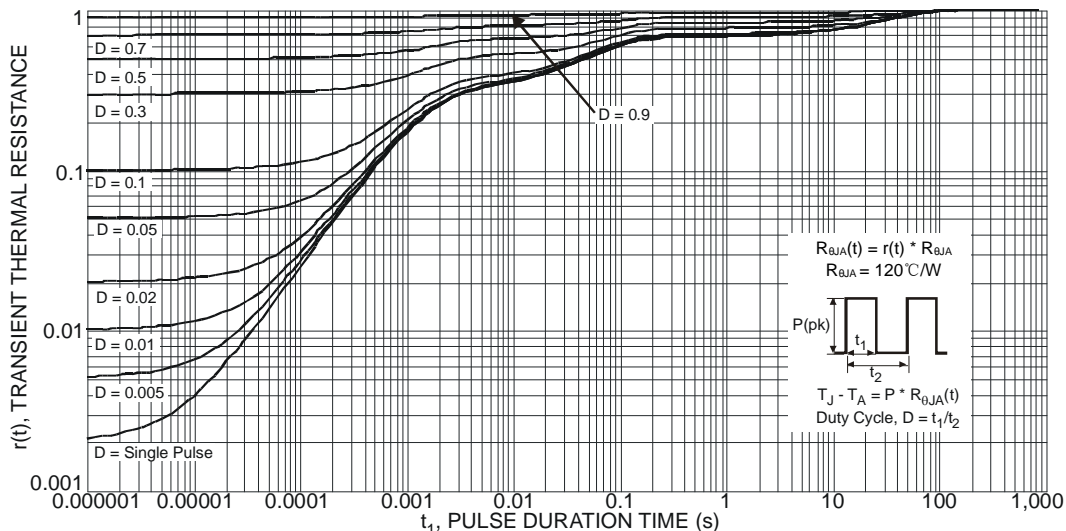


Fig. 2 Transient Thermal Response

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 8)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-20	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	I <sub>DSS</sub>	—	—	-1	μA	V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±10	μA	V <sub>GS</sub> = ±8V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 8)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	-0.5	-0.7	-1.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	—	495	mΩ	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -400mA
				690		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -300mA
				960		V <sub>GS</sub> = -1.8V, I <sub>D</sub> = -100mA
Forward Transfer Admittance	Y <sub>FS</sub>	50	—	—	ms	V <sub>DS</sub> = -3V, I <sub>D</sub> = -300mA
Diode Forward Voltage	V <sub>SD</sub>	—	—	-1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -300mA
<b>DYNAMIC CHARACTERISTICS (Note 9)</b>						
Input Capacitance	C <sub>iss</sub>	—	76.5	—	pF	V <sub>DS</sub> = -10V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	13.7	—	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	—	10.7	—	pF	
Gate Resistance	R <sub>g</sub>	—	195	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge	Q <sub>g</sub>	—	1.5	—	nC	V <sub>GS</sub> = -8V, V <sub>DS</sub> = -15V, I <sub>D</sub> = -1A
Total Gate Charge	Q <sub>g</sub>	—	1.0	—	nC	V <sub>GS</sub> = -4.5V, V <sub>DS</sub> = -15V, I <sub>D</sub> = -1A
Gate-Source Charge	Q <sub>gs</sub>	—	0.2	—	nC	
Gate-Drain Charge	Q <sub>gd</sub>	—	0.3	—	nC	
Turn-On Delay Time	t <sub>D(ON)</sub>	—	7.1	—	ns	V <sub>DS</sub> = -10V, -I <sub>D</sub> = 1A V <sub>GS</sub> = -4.5V, R <sub>g</sub> = 6Ω
Turn-On Rise Time	t <sub>r</sub>	—	8.0	—	ns	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	31.7	—	ns	
Turn-Off Fall Time	t <sub>f</sub>	—	18.5	—	ns	

Notes: 8. Short duration pulse test used to minimize self-heating effect.  
9. Guaranteed by design. Not subject to product testing.

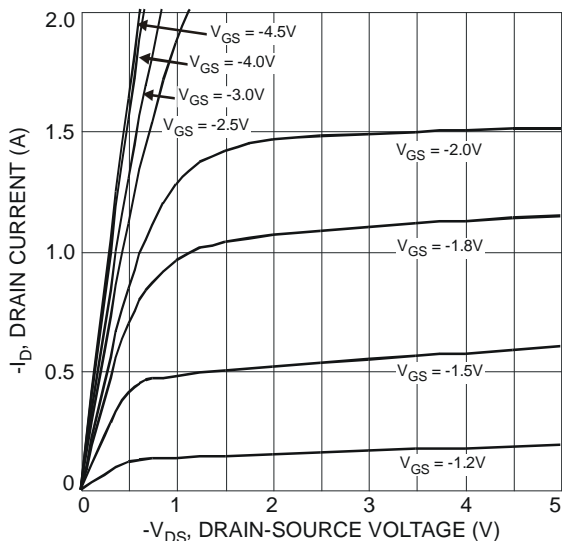
**Typical Characteristics**


Fig. 3 Typical Output Characteristic

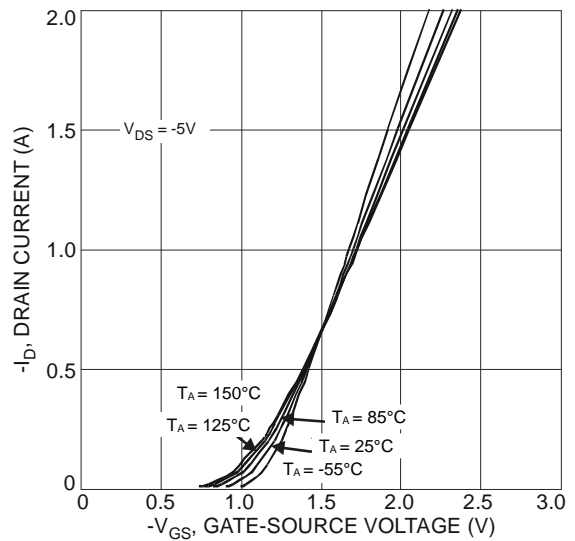
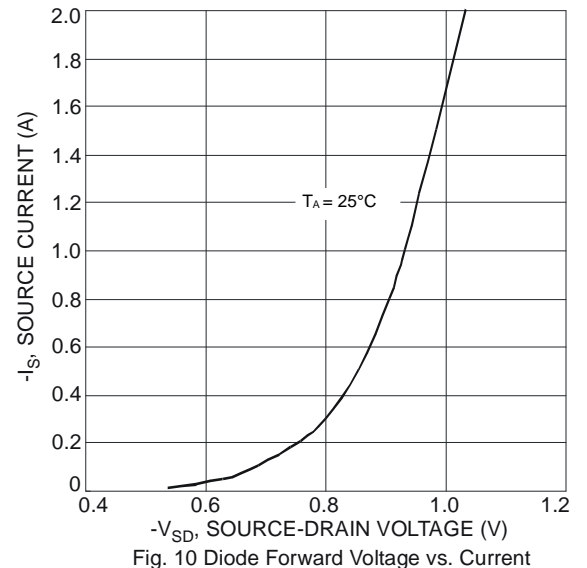
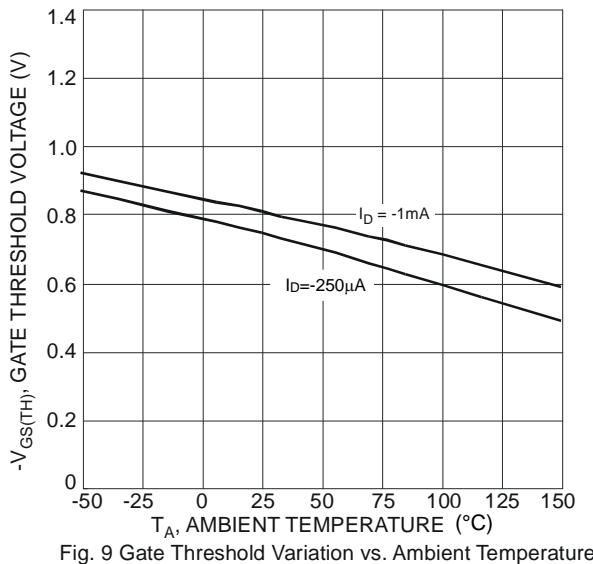
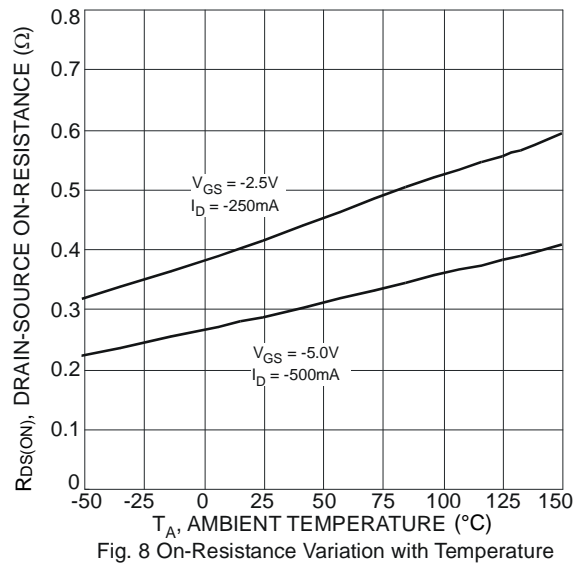
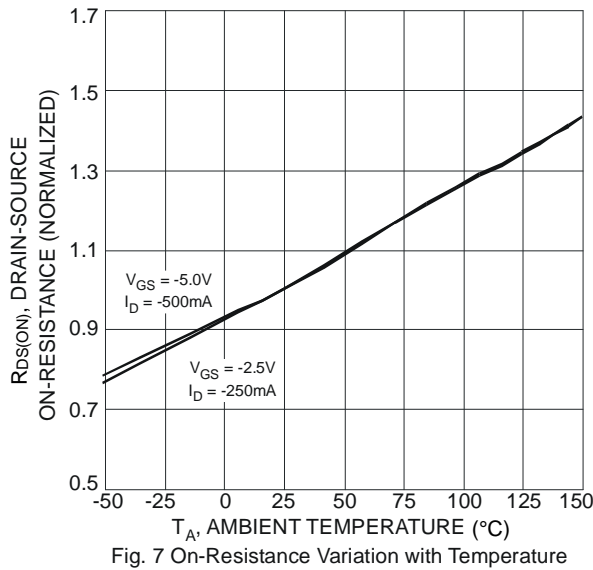
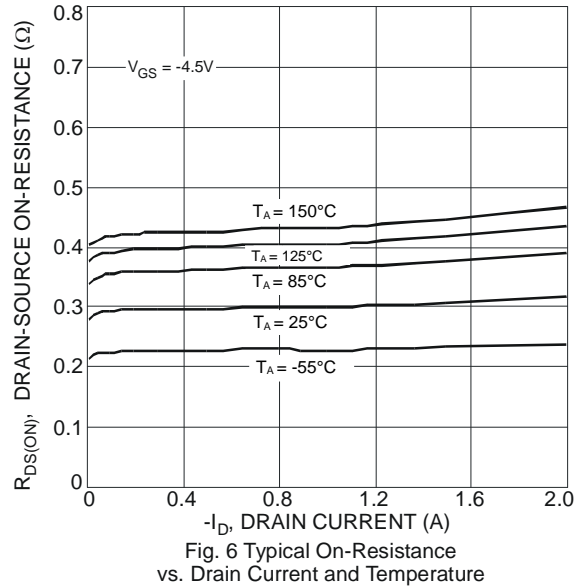
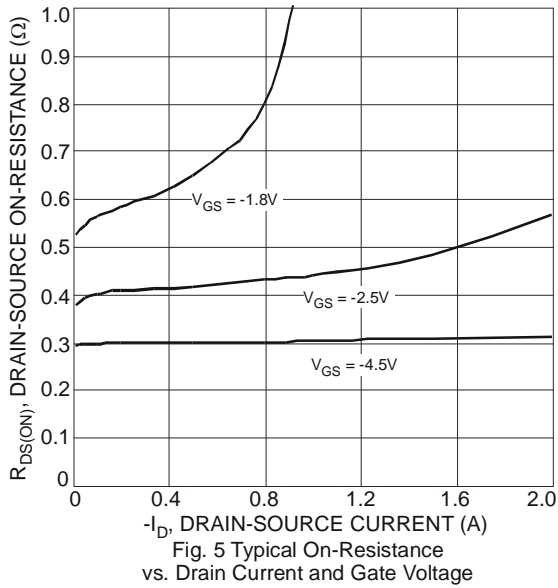


Fig. 4 Typical Transfer Characteristic

**Typical Characteristics** (continued)



**Typical Characteristics** (continued)

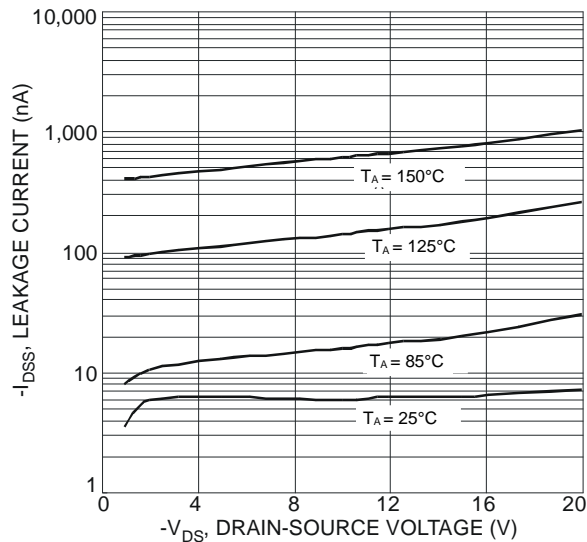


Fig. 11 Typical Leakage Current vs. Drain-Source Voltage

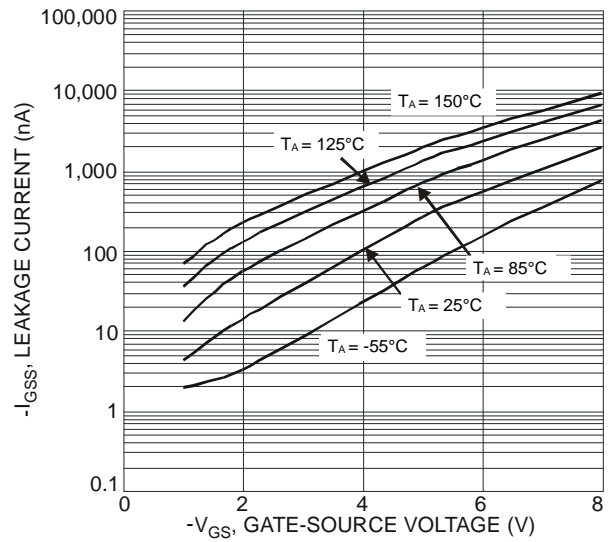


Fig. 12 Leakage Current vs. Gate-Source Voltage

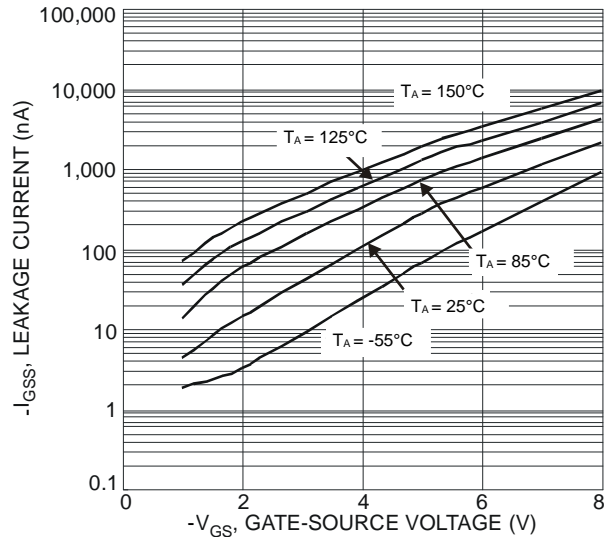


Fig. 13 Leakage Current vs. Gate-Source Voltage

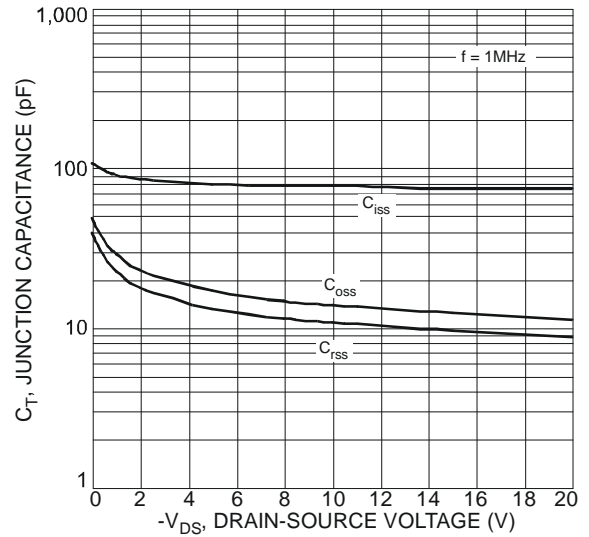


Fig. 14 Typical Junction Capacitance

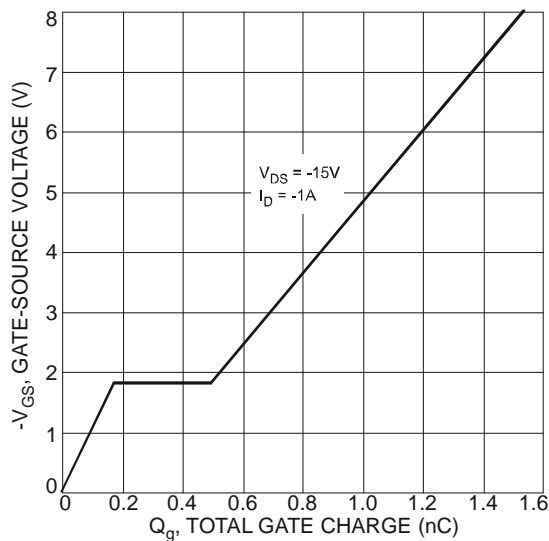
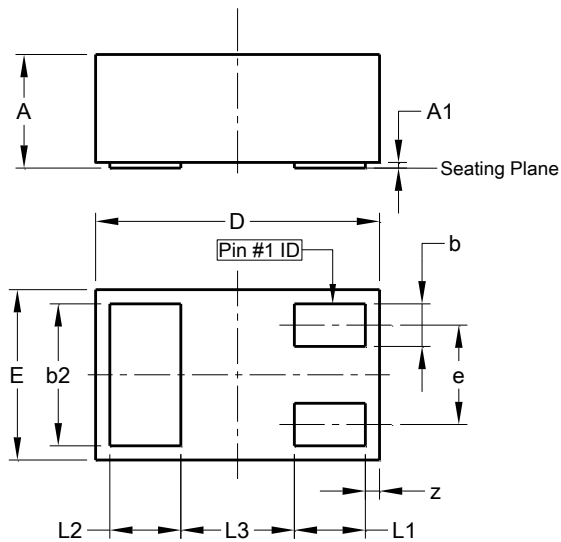


Fig. 15 Gate-Charge Characteristics

**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**X2-DFN1006-3**

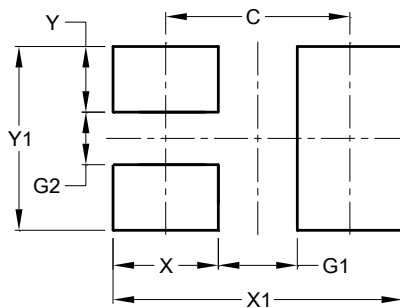


X2-DFN1006-3			
Dim	Min	Max	Typ
A	—	0.40	—
A1	0.00	0.05	0.03
b	0.10	0.20	0.15
b2	0.45	0.55	0.50
D	0.95	1.05	1.00
E	0.55	0.65	0.60
e	—	—	0.35
L1	0.20	0.30	0.25
L2	0.20	0.30	0.25
L3	—	—	0.40
z	0.02	0.08	0.05
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

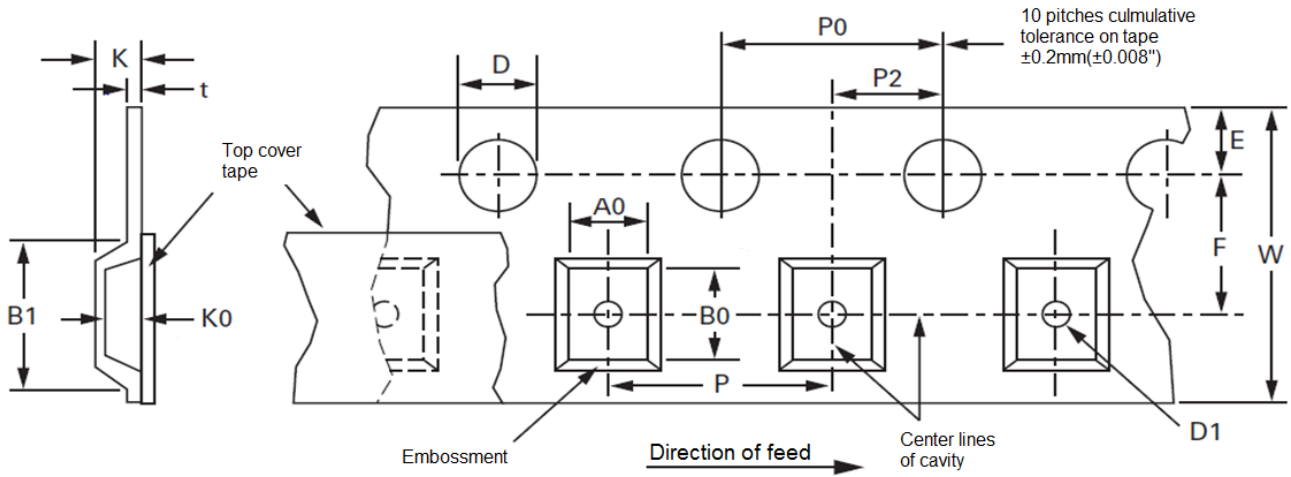
**X2-DFN1006-3**



Dimensions	Value (in mm)
C	0.70
G1	0.30
G2	0.20
X	0.40
X1	1.10
Y	0.25
Y1	0.70

## Embossed Carrier Tape Specifications

Please see <http://www.diodes.com/package-outlines.html> for the latest version.



Tape Width (W)	Dimension	Value (mm)	Dimension	Value (mm)	Dimension	Value (mm)
8mm	B1	4.5 max.	F	3.5±0.05	P2	2.0±0.05
	D	1.5+0.10 -0.0	K	2.4 max.	t	0.40 max.
	D1	0.35 min.	P	4.0±0.10 2.0±0.05(-7B)	W	8±0.30
	E	1.75±0.10	P0	4.0±0.10		
	A0 B0 K0	Determined by component size. The clearance between the component and the cavity must comply to the rotational and lateral movement requirement provided in figures in the "Maximum Component Movement in Tape Pocket" section.				



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