

## Product Summary

BV <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub> T <sub>C</sub> = +25°C
-60V	50mΩ @ V <sub>GS</sub> = -10V	-26A
	70mΩ @ V <sub>GS</sub> = -4.5V	-22A

## Description and Applications

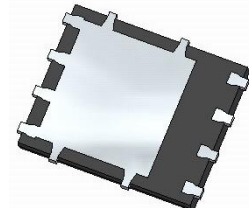
This new generation 60V P-Channel Enhancement Mode MOSFET is designed to minimize R<sub>DS(ON)</sub> and yet maintain superior switching performance. This device is ideal for use in Notebook battery power management and loadswitch.

- Notebook Battery Power Management
- DC-DC Converters
- Loadswitch

PowerDI5060-8



Top View



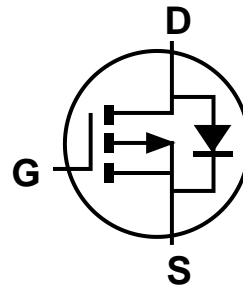
Bottom View

## Features and Benefits

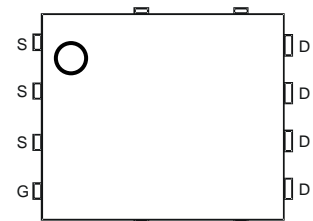
- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low R<sub>DS(ON)</sub> – Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- <1.1mm Package Profile – Ideal for Thin Applications
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

## Mechanical Data

- Case: PowerDI<sup>®</sup> 5060-8
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish - Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208 (E3)
- Weight: 0.097 grams (Approximate)



Internal Schematic

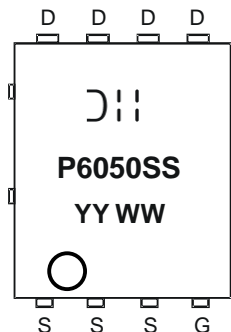

 Top View  
 Pin Configuration

## Ordering Information (Note 4)

Part Number	Case	Packaging
DMP6050SPS-13	PowerDI5060-8	2500 / Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information



= Manufacturer's Marking  
 P6050SS = Product Type Marking Code  
 YYWW = Date Code Marking  
 YY = Last Two Digits of Year (ex: 18 = 2018)  
 WW = Week Code (01 to 53)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	-60	V	
Gate-Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current (Note 6) V <sub>GS</sub> = -10V	I <sub>D</sub>	T <sub>A</sub> = +25°C	-5.7	A
		T <sub>A</sub> = +70°C	-4.5	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	-45	A	
Maximum Continuous Body Diode Forward Current (Note 6)	I <sub>S</sub>	-2.4	A	
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)	I <sub>SM</sub>	-45	A	
Avalanche Current (Note 8) L = 0.1mH	I <sub>AS</sub>	-25	A	
Repetitive Avalanche Energy (Note 8) L = 0.1mH	E <sub>AS</sub>	32	mJ	

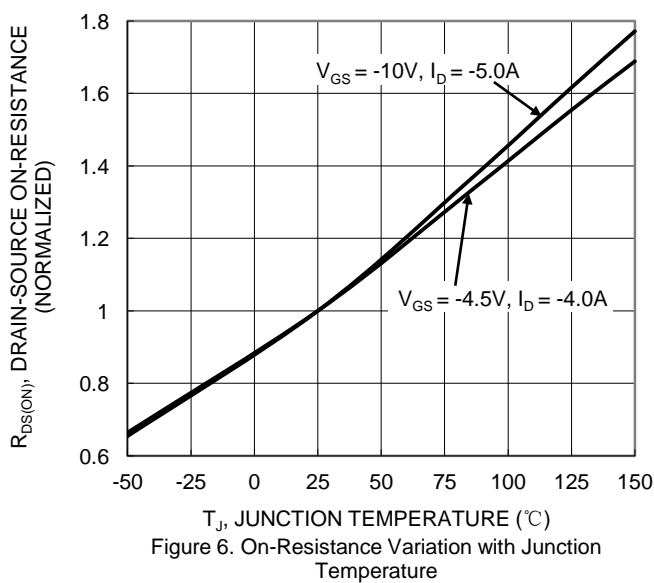
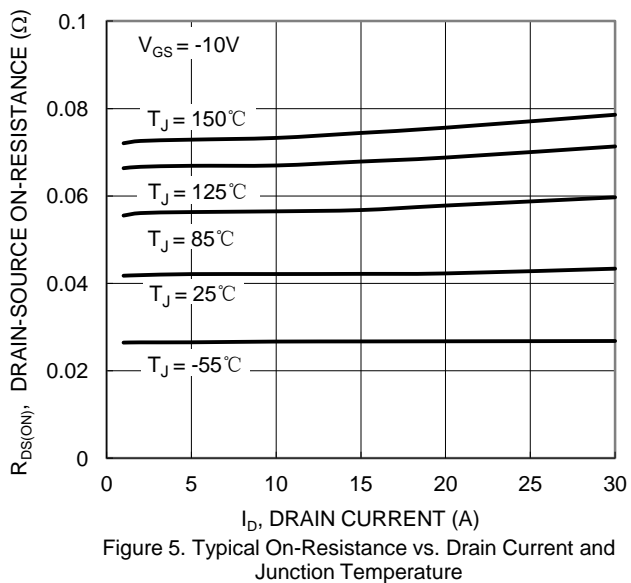
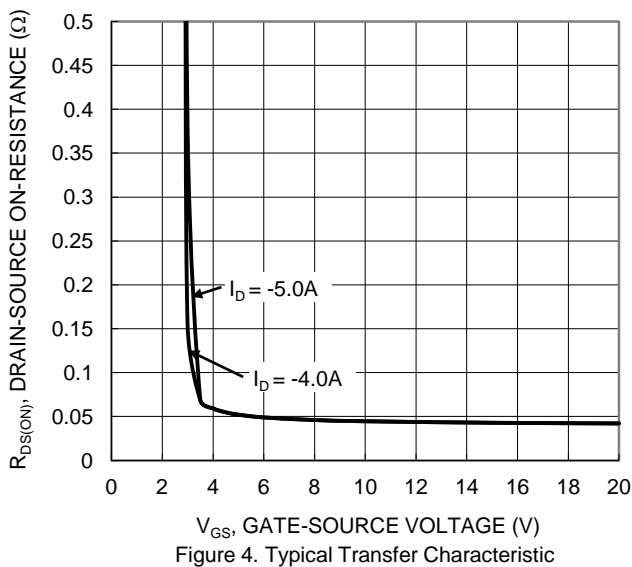
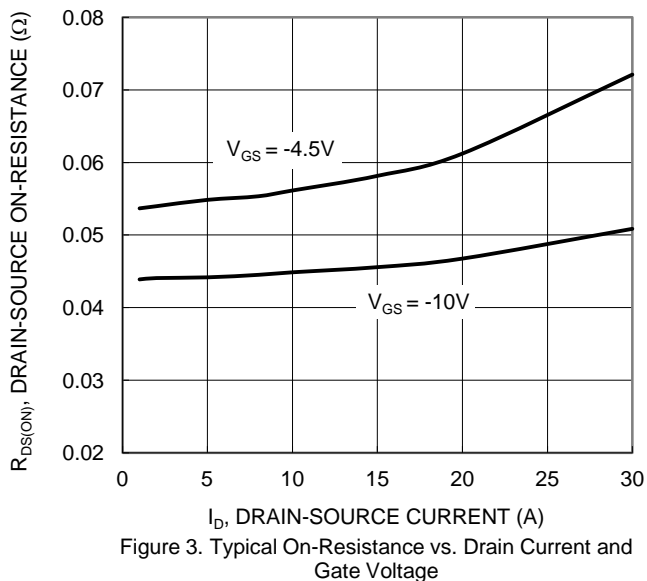
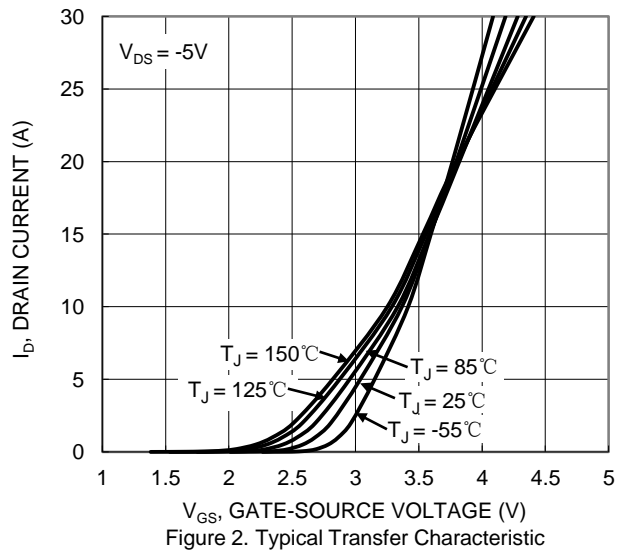
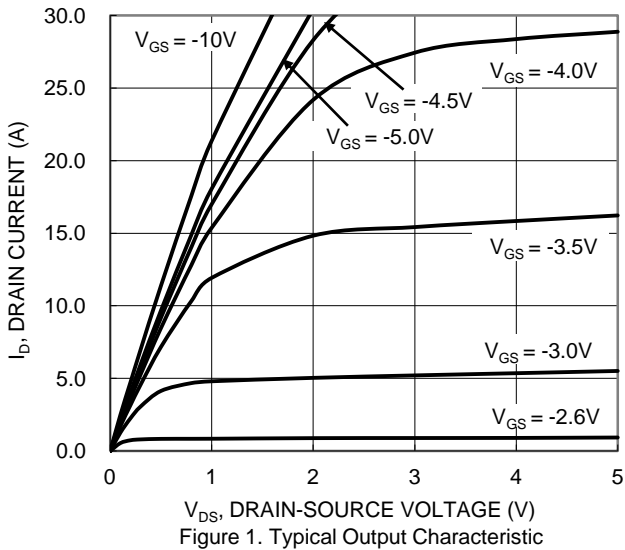
**Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P <sub>D</sub>	1.3	W
Thermal Resistance, Junction to Ambient @ T <sub>A</sub> = +25°C (Note 5)	R <sub>θJA</sub>	95	°C/W
Power Dissipation (Note 6)	P <sub>D</sub>	2.4	W
Thermal Resistance, Junction to Ambient @ T <sub>A</sub> = +25°C (Note 6)	R <sub>θJA</sub>	52	°C/W
Thermal Resistance, Junction to Case @ T <sub>C</sub> = +25°C (Note 7)	R <sub>θJC</sub>	2.4	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 9)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250µA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	-1	µA	V <sub>DS</sub> = -60V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 9)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	-1.0	—	-3.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250µA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	43	50	mΩ	V <sub>GS</sub> = -10V, I <sub>D</sub> = -5A
		—	53	70		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4A
Diode Forward Voltage	V <sub>SD</sub>	—	-0.7	-1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1A
<b>DYNAMIC CHARACTERISTICS (Note 10)</b>						
Input Capacitance	C <sub>ISS</sub>	—	2163	—	pF	V <sub>DS</sub> = -30V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>OSS</sub>	—	88	—	pF	
Reverse Transfer Capacitance	C <sub>RSS</sub>	—	58	—	pF	
Gate Resistance	R <sub>g</sub>	—	13	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = -10V)	Q <sub>g</sub>	—	30	—	nC	V <sub>DS</sub> = -30V, I <sub>D</sub> = -5A
Total Gate Charge (V <sub>GS</sub> = -4.5V)	Q <sub>g</sub>	—	14	—	nC	
Gate-Source Charge	Q <sub>gs</sub>	—	5	—	nC	
Gate-Drain Charge	Q <sub>gd</sub>	—	4.6	—	nC	
Turn-On Delay Time	t <sub>D(ON)</sub>	—	4.7	—	ns	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -30V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = -5A
Turn-On Rise Time	t <sub>r</sub>	—	2.7	—	ns	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	73	—	ns	
Turn-Off Fall Time	t <sub>f</sub>	—	25	—	ns	
Body Diode Reverse Recovery Time	t <sub>RR</sub>	—	18	—	ns	I <sub>F</sub> = -5A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q <sub>RR</sub>	—	12	—	nC	I <sub>F</sub> = -5A, di/dt = 100A/µs

- Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
  7. Thermal resistance from junction to soldering point (on the exposed drain pad).
  8. I<sub>AS</sub> and E<sub>AS</sub> ratings are based on low frequency and duty cycles to keep T<sub>J</sub> = +25°C.
  9. Short duration pulse test used to minimize self-heating effect.
  10. Guaranteed by design. Not subject to product testing.



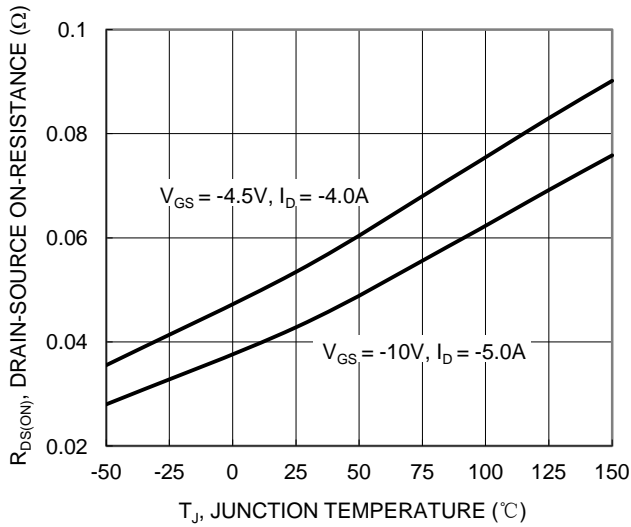


Figure 7. On-Resistance Variation with Junction Temperature

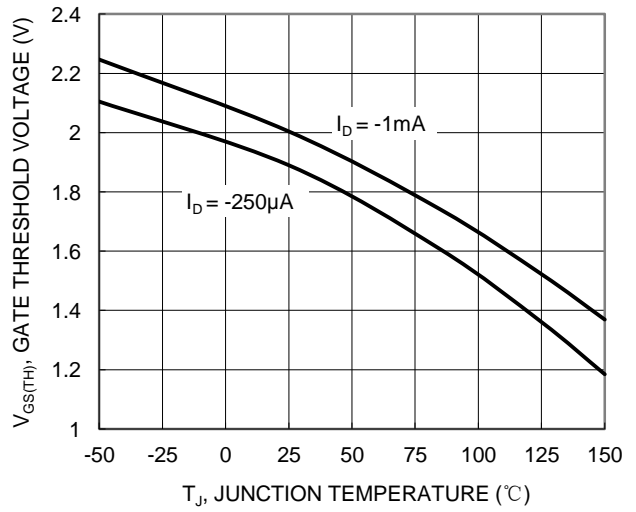


Figure 8. Gate Threshold Variation vs. Junction Temperature

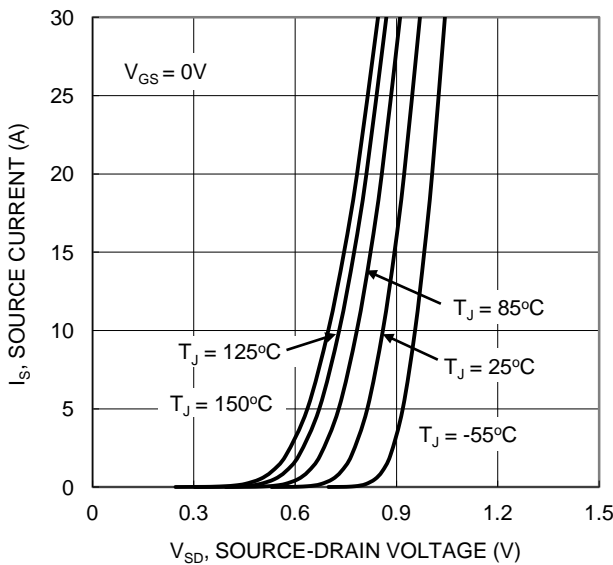


Figure 9. Diode Forward Voltage vs. Current

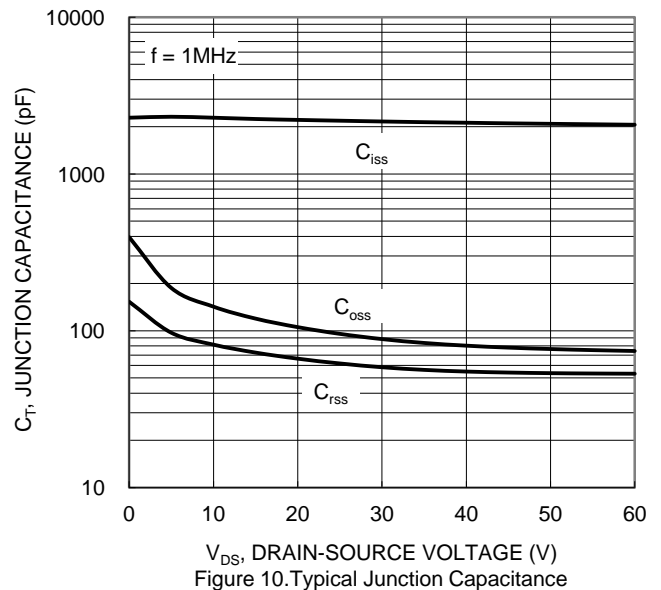


Figure 10. Typical Junction Capacitance

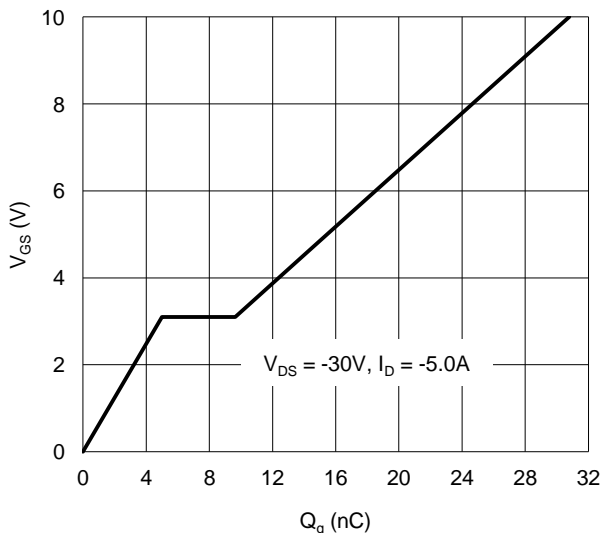


Figure 11. Gate Charge

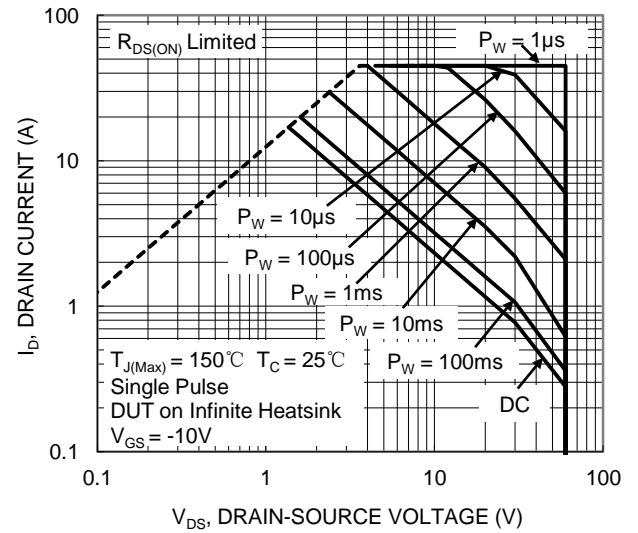


Figure 12. SOA, Safe Operation Area

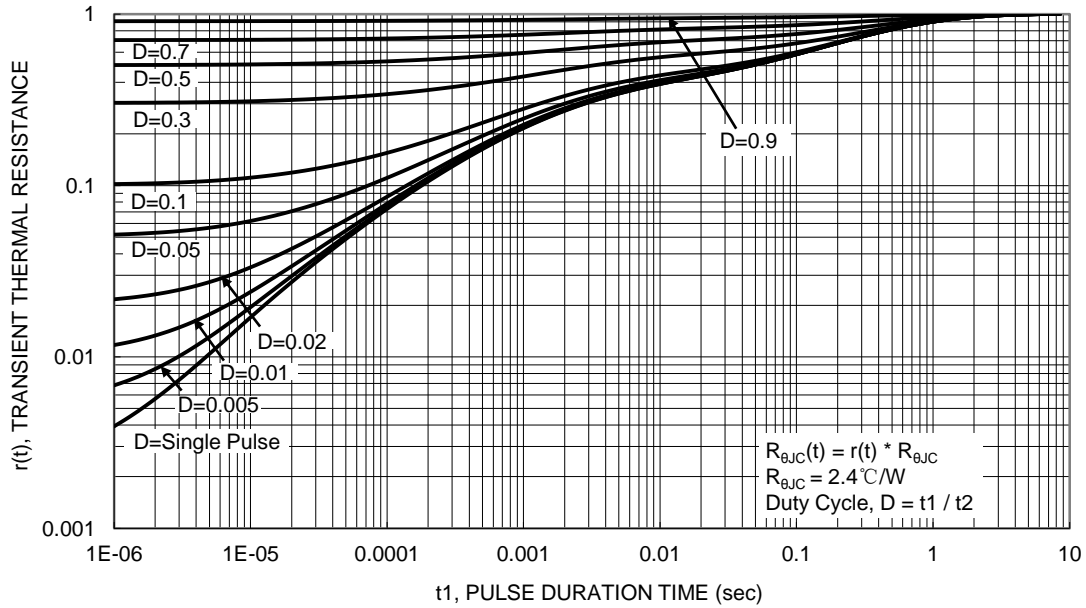
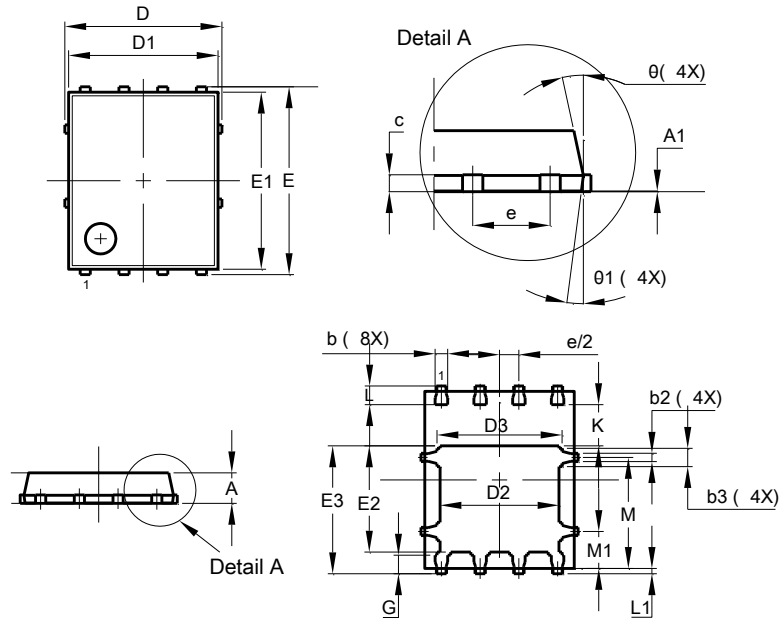


Figure 13. Transient Thermal Resistance

**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**PowerDI5060-8**

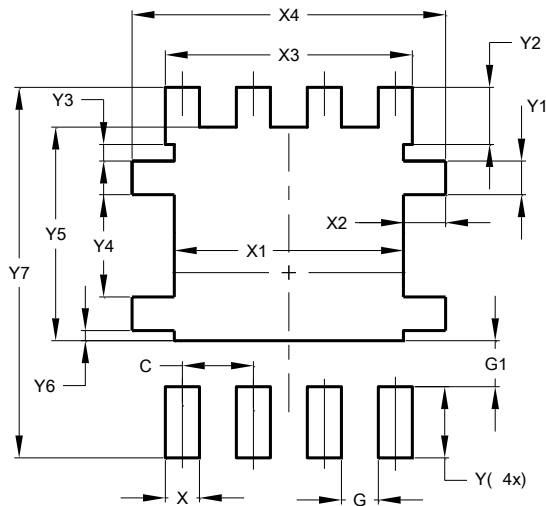


PowerDI5060-8			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0.00	0.05	—
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	—	—
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**PowerDI5060-8**



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

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