

## Product Summary

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> T <sub>C</sub> = +25°C
-40V	15mΩ @ V <sub>GS</sub> = -10V	-55A
	23mΩ @ V <sub>GS</sub> = -4.5V	-50A

## Description

This MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

## Applications

- Reverse Polarity Protection
- Motor Control
- Power Management

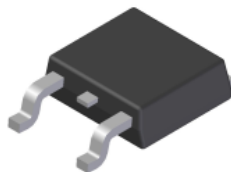
## Features and Benefits

- Rated to +175°C – Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switch (UIS) Test in Production
- Low On-Resistance
- Fast Switching Speed
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)**
- Qualified to AEC-Q101 Standards for High Reliability**
- An Automotive-Compliant Part is Available Under Separate Datasheet ([DMPH4013SK3Q](#))**

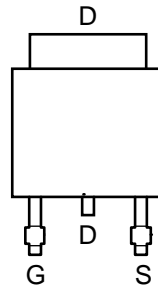
## Mechanical Data

- Case: TO252 (DPAK)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Matte Tin Finish Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.33 grams (Approximate)

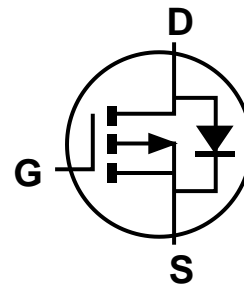
TO252 (DPAK)



Top View



Top View  
Pin-Out



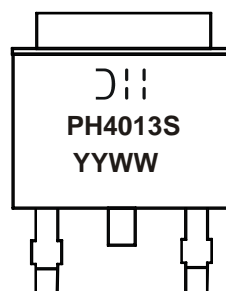
Equivalent Circuit

## Ordering Information (Note 4)

Part Number	Case	Packaging
DMPH4013SK3-13	TO252 (DPAK)	2,500/Tape & Reel

- Notes:
- EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
  - See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  - Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  - For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information



- = Manufacturer's Marking
- PH4013S = Product Type Marking Code
- YYWW = Date Code Marking
- YY = Year (ex: 18 = 2018)
- WW = Week (01 to 53)

**Maximum Ratings** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			$V_{DSS}$	-40	V
Gate-Source Voltage			$V_{GSS}$	$\pm 20$	V
Continuous Drain Current (Note 6) $V_{GS} = -10\text{V}$	Steady State	$T_C = +25^\circ\text{C}$ $T_C = +100^\circ\text{C}$	$I_D$	-55 -40	A
Pulsed Drain Current (10 $\mu\text{s}$ Pulse, Duty Cycle = 1%)			$I_{DM}$	-120	A
Maximum Body Diode Forward Current (Note 6)			$I_S$	-3.6	A
Pulsed Drain Current (10 $\mu\text{s}$ Pulse, Duty Cycle = 1%)			$I_{SM}$	-120	A
Avalanche Current, $L = 0.1\text{mH}$ (Note 7)			$I_{AS}$	-40	A
Avalanche Energy, $L = 0.1\text{mH}$ (Note 7)			$E_{AS}$	69	mJ

**Thermal Characteristics** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Total Power Dissipation (Note 5)			$P_D$	2.1	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady state		$R_{\theta JA}$	71	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)			$P_D$	3.7	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady state		$R_{\theta JA}$	41	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case			$R_{\theta JC}$	1.7	
Operating and Storage Temperature Range			$T_J, T_{STG}$	-55 to +175	$^\circ\text{C}$

**Electrical Characteristics** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 8)</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	-40	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	-1	$\mu\text{A}$	$V_{DS} = -40\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
<b>ON CHARACTERISTICS (Note 8)</b>						
Gate Threshold Voltage	$V_{GS(TH)}$	-1.0	—	-3.0	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	10	15	m $\Omega$	$V_{GS} = -10\text{V}, I_D = -10\text{A}$
		—	15	23		$V_{GS} = -4.5\text{V}, I_D = -8\text{A}$
Diode Forward Voltage	$V_{SD}$	—	-0.7	-1.2	V	$V_{GS} = 0\text{V}, I_S = -1\text{A}$
<b>DYNAMIC CHARACTERISTICS (Note 9)</b>						
Input Capacitance	$C_{iss}$	—	4004	—	pF	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	$C_{oss}$	—	309	—		
Reverse Transfer Capacitance	$C_{rss}$	—	229	—		
Gate Resistance	$R_g$	—	3.5	—	$\Omega$	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ( $V_{GS} = -4.5\text{V}$ )	$Q_g$	—	31	—	nC	$V_{DS} = -20\text{V}, I_D = -10\text{A}$
Total Gate Charge ( $V_{GS} = -10\text{V}$ )	$Q_g$	—	67	—		
Gate-Source Charge	$Q_{gs}$	—	13.2	—		
Gate-Drain Charge	$Q_{gd}$	—	11	—		
Turn-On Delay Time	$t_{D(ON)}$	—	9.9	—	ns	$V_{GS} = -10\text{V}, V_{DD} = -20\text{V},$ $R_G = 3\Omega, I_D = -10\text{A}$
Turn-On Rise Time	$t_R$	—	32	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	46	—		
Turn-Off Fall Time	$t_F$	—	53	—		
Reverse Recovery Time	$t_{RR}$	—	19.5	—	ns	$I_F = -10\text{A}, di/dt = -100\text{A}/\mu\text{s}$
Reverse Recovery Charge	$Q_{RR}$	—	11.6	—	nC	$I_F = -10\text{A}, di/dt = -100\text{A}/\mu\text{s}$

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
  - $I_{AS}$  and  $E_{AS}$  ratings are based on low frequency and duty cycles to keep  $T_J = +25^\circ\text{C}$ .
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to product testing.

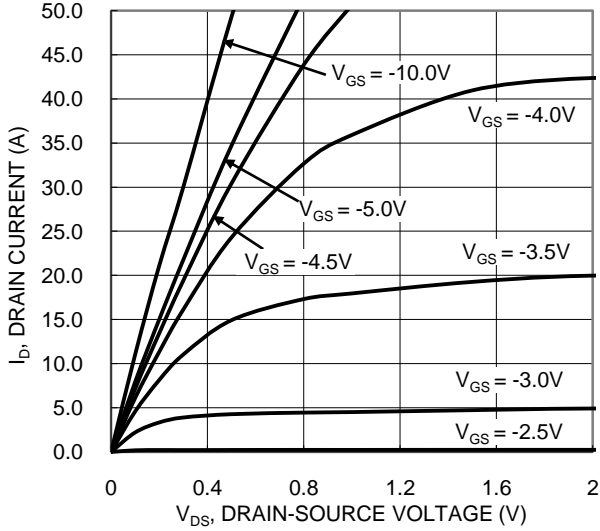


Figure 1. Typical Output Characteristic

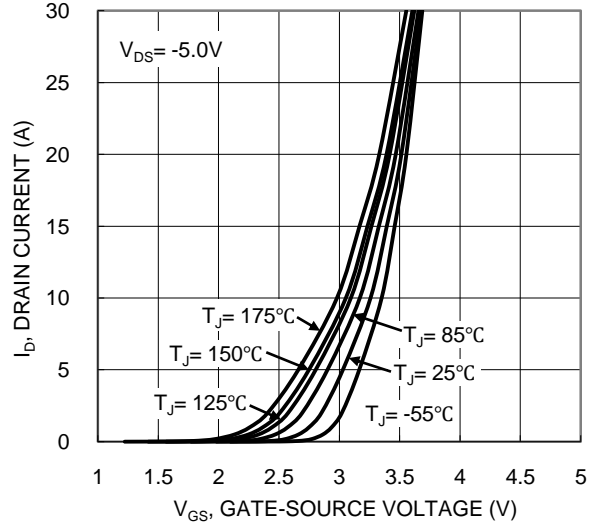


Figure 2. Typical Transfer Characteristic

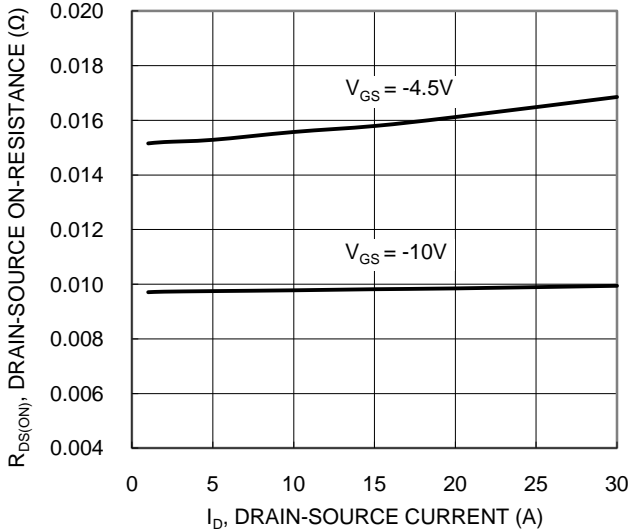


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

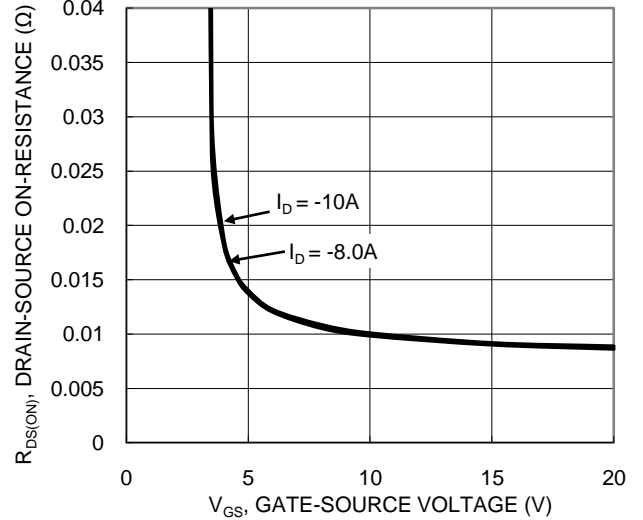


Figure 4. Typical Transfer Characteristic

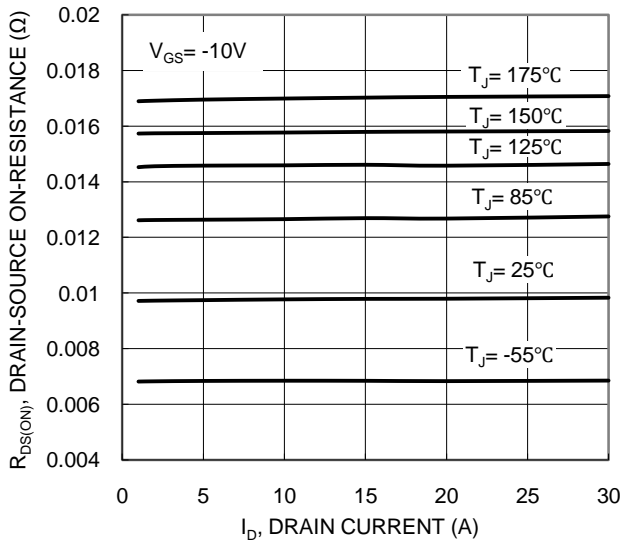


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

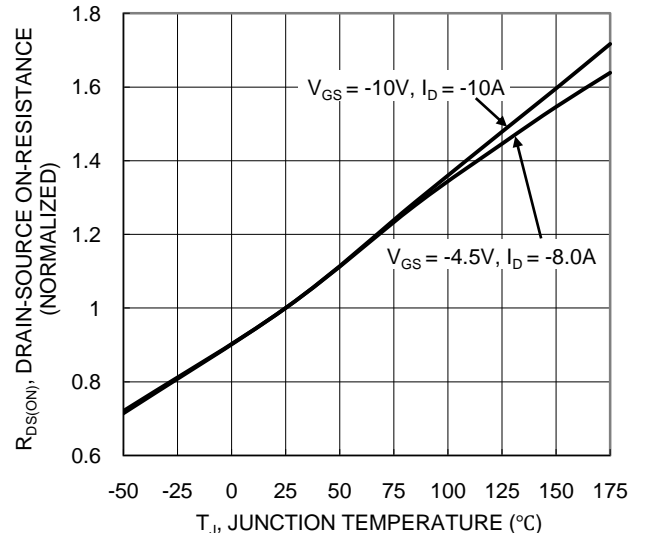


Figure 6. On-Resistance Variation with Temperature

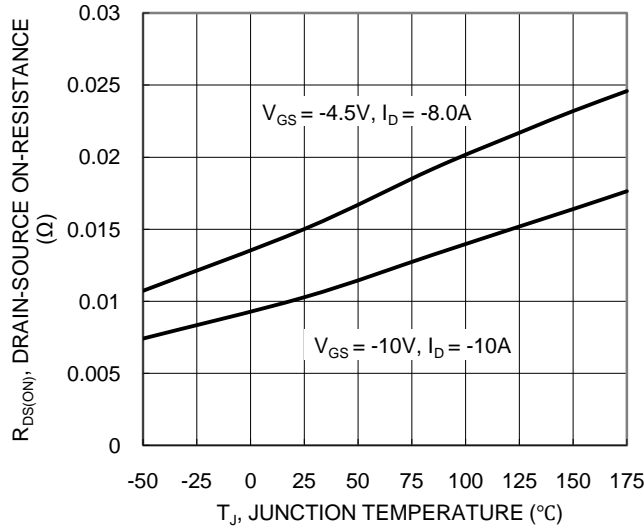


Figure 7. On-Resistance Variation with Temperature

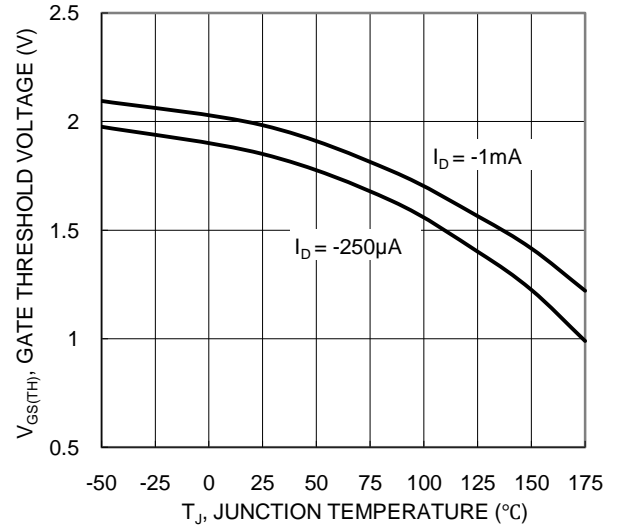


Figure 8. Gate Threshold Variation vs. Temperature

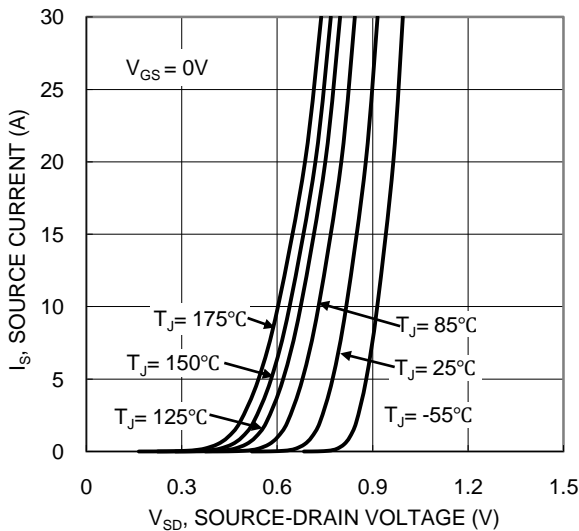


Figure 9. Diode Forward Voltage vs. Current

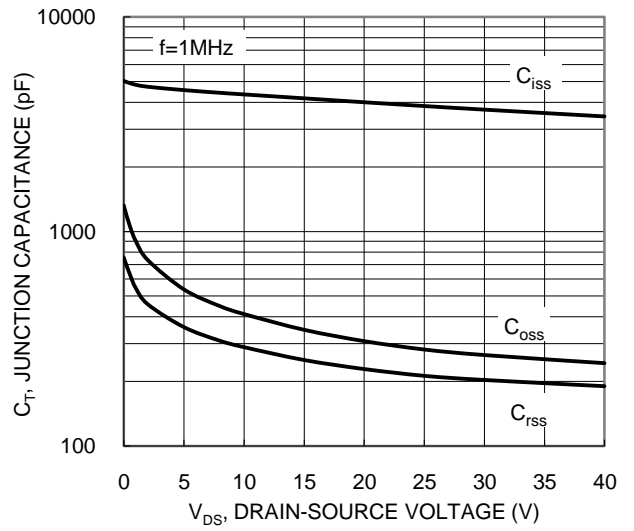


Figure 10. Typical Junction Capacitance

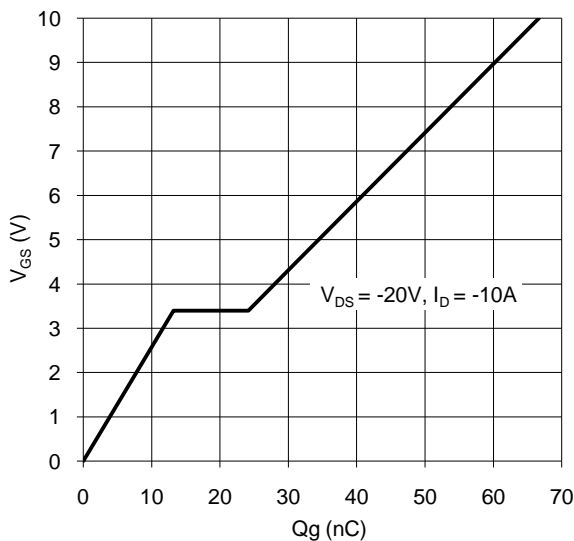


Figure 11. Gate Charge

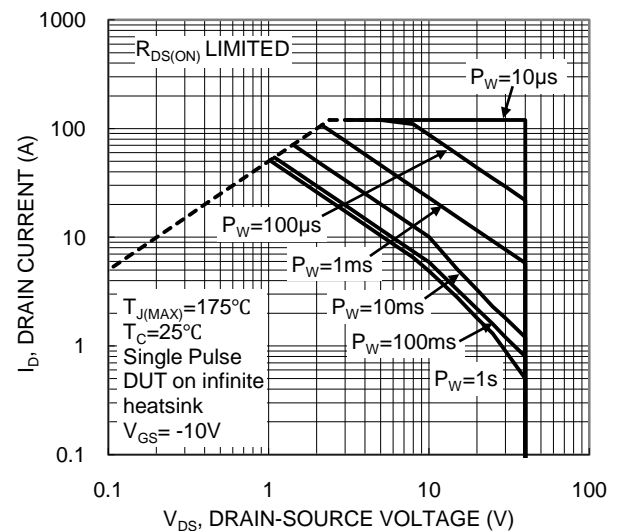


Figure 12. SOA, Safe Operation Area

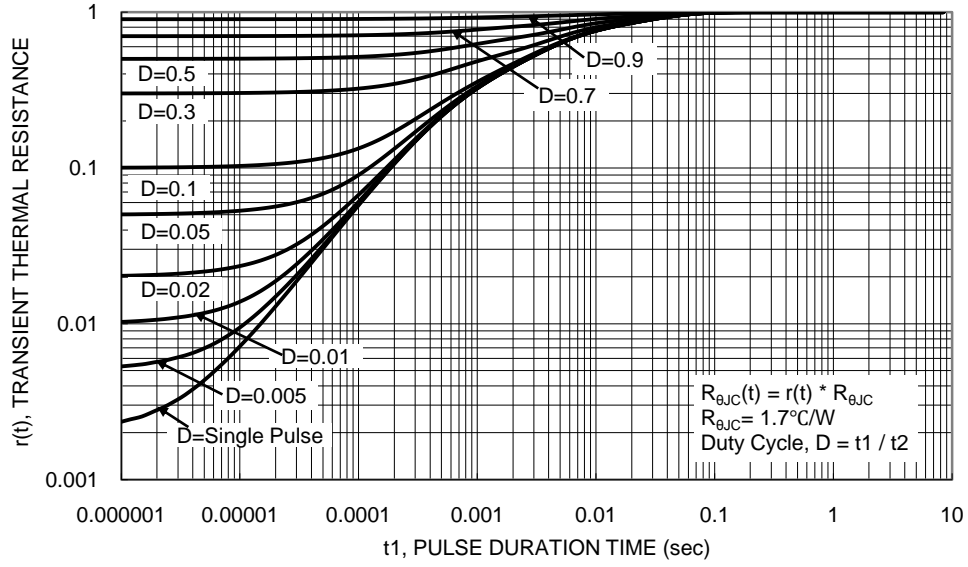
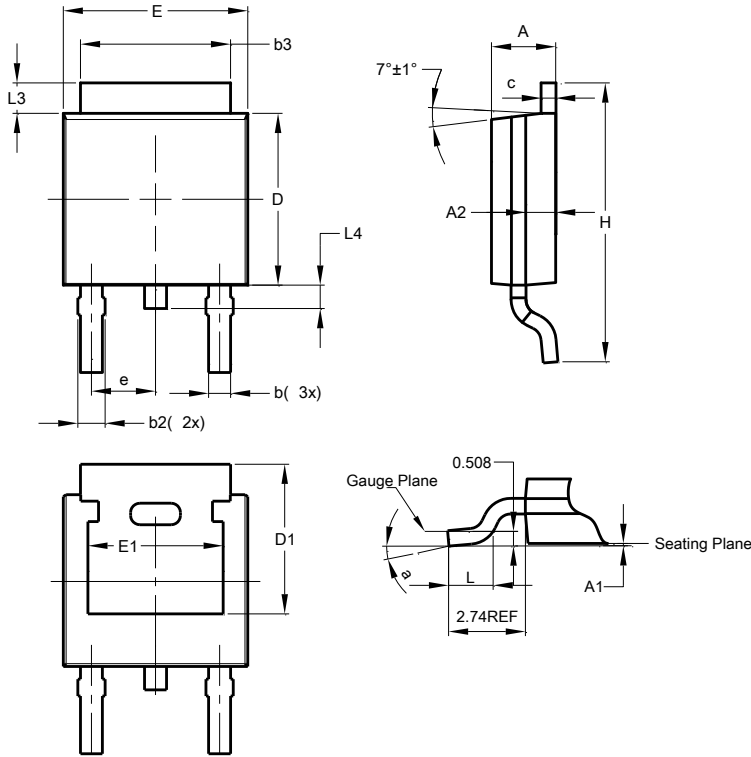


Figure 13. Transient Thermal Resistance

**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**TO252 (DPAK)**

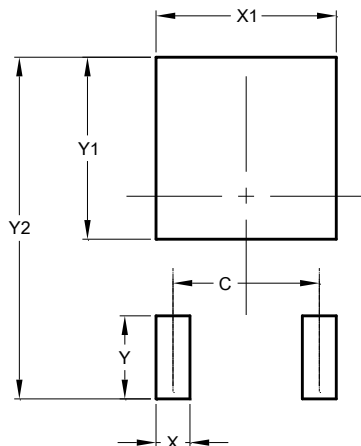


TO252 (DPAK)			
Dim	Min	Max	Typ
A	2.19	2.39	2.29
A1	0.00	0.13	0.08
A2	0.97	1.17	1.07
b	0.64	0.88	0.783
b2	0.76	1.14	0.95
b3	5.21	5.46	5.33
c	0.45	0.58	0.531
D	6.00	6.20	6.10
D1	5.21	-	-
e	-	-	2.286
E	6.45	6.70	6.58
E1	4.32	-	-
H	9.40	10.41	9.91
L	1.40	1.78	1.59
L3	0.88	1.27	1.08
L4	0.64	1.02	0.83
a	0°	10°	-
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**TO252 (DPAK)**



Dimensions	Value (in mm)
C	4.572
X	1.060
X1	5.632
Y	2.600
Y1	5.700
Y2	10.700

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