DUAL 30V N-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI5060-8 (Type S)

Product Summary

Device	BV_{DSS}	$R_{DS(ON)}$	I_D T_C = +25°C
Q1	30V	11.1mΩ @ V_{GS} = 10V	35A
		14.0mΩ @ V_{GS} = 4.5V	27A
Q2	30V	6.0mΩ @ V_{GS} = 10V	50A
		10.0mΩ @ V_{GS} = 4.5V	35A

Features and Benefits

- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Description and Applications

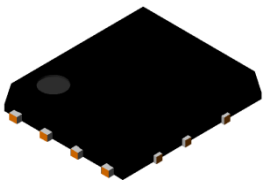
This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Notebook Battery Power Management
- DC-DC Converters
- Loadswitch

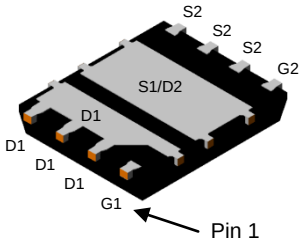
Mechanical Data

- Case: PowerDI®5060-8 (Type S)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – 100% Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Terminal Connections: See Diagram Below
- Weight: 0.097 grams (Approximate)

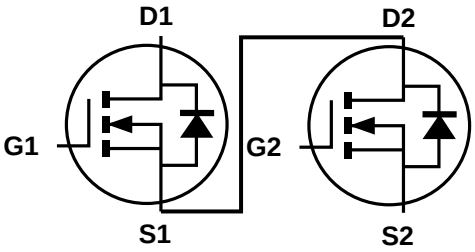
PowerDI5060-8 (Type S)



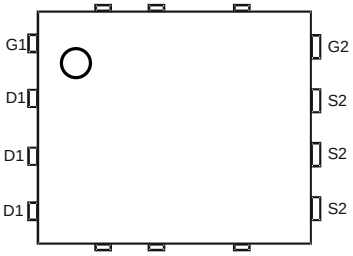
Top View



Bottom View



Q1 N-Channel MOSFET Q2 N-Channel MOSFET



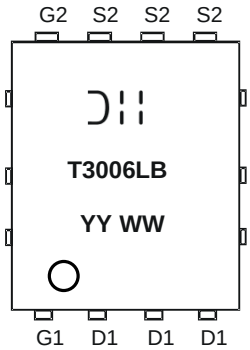
Top View
Pin Configuration

Ordering Information (Note 4)

Part Number	Case	Packaging
DMT3006LPB-13	PowerDI5060-8 (Type S)	2500 / Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



= Manufacturer's Marking
T3006LB = Product Type Marking Code
YYWW = Date Code Marking
YY = Year (ex: 18 = 2018)
WW = Week (01 to 53)

PowerDI is a registered trademark of Diodes Incorporated.

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Q1 Value	Q2 Value	Unit
Drain-Source Voltage			V_{DSS}	30	30	V
Gate-Source Voltage			V_{GSS}	±20	±20	V
Continuous Drain Current (Note 7) V_{GS} = 10V	Steady State	T_C = +25°C T_C = +70°C	I_D	35 27	50 40	A
Continuous Drain Current (Note 6) V_{GS} = 10V	Steady State	T_A = +25°C T_A = +70°C	I_D	11 9	14 11	A
Maximum Body Diode Forward Current (Note 7)			I_S	40	50	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	80	100	A
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)			I_{SM}	80	100	A
Avalanche Current (Note 8) L = 0.1mH			I_{AS}	19	23	A
Avalanche Energy (Note 8) L = 0.1mH			E_{AS}	18	28	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	1.1	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	116	°C/W
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	1.7	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	72	°C/W
Total Power Dissipation (Note 7)		P_D	30	W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	4	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics Q1 N-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 24V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = 20V, V_{DS} = 0V V_{GS} = -16V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.0	—	3.0	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	6.7	11.1	mΩ	V_{GS} = 10V, I_D = 11.5A
		—	11.0	14.0		V_{GS} = 4.5V, I_D = 7A
Diode Forward Voltage	V_{SD}	—	0.8	1.2	V	V_{GS} = 0V, I_S = 10A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	841	—	pF	V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	349	—		
Reverse Transfer Capacitance	C_{rss}	—	51	—		
Gate Resistance	R_G	—	1.2	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = 10V)	Q_G	—	12.6	—	nC	V_{DS} = 15V, I_D = 14.4A
Total Gate Charge (V_{GS} = 4.5V)	Q_G	—	6.3	—		
Gate-Source Charge	Q_{GS}	—	1.7	—		
Gate-Drain Charge	Q_{GD}	—	3.1	—		
Turn-On Delay Time	$t_{D(ON)}$	—	4.6	—	ns	V_{GS} = 10V, V_{DD} = 15V, R_G = 1Ω, I_D = 10A
Turn-On Rise Time	t_R	—	3.3	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	10.2	—		
Turn-Off Fall Time	t_F	—	1.8	—		
Body Diode Reverse Recovery Time	t_{RR}	—	15.6	—	ns	I_F = 10A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q_{RR}	—	5.8	—	nC	I_F = 10A, di/dt = 100A/µs

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Thermal resistance from junction to soldering point (on the exposed drain pad).
8. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

Electrical Characteristics Q2 N-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 24V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = +20V, V_{DS} = 0V V_{GS} = -16V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.0	—	3.0	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	5.0	6.0	mΩ	V_{GS} = 10V, I_D = 20A
			7.5	10.0		V_{GS} = 4.5V, I_D = 10A
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	V_{GS} = 0V, I_S = 2A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	1,155	—	pF	V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	456	—		
Reverse Transfer Capacitance	C_{rss}	—	72	—		
Gate Resistance	R_G	—	2.1	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = 10V)	Q_G	—	16.7	—	nC	V_{DD} = 15V, I_D = 9A
Total Gate Charge (V_{GS} = 4.5V)	Q_G	—	8.4	—		
Gate-Source Charge	Q_{GS}	—	2.2	—		
Gate-Drain Charge	Q_{GD}	—	3.5	—		
Turn-On Delay Time	$t_{D(ON)}$	—	3.5	—	ns	V_{DD} = 15V, V_{GS} = 10V, R_G = 3Ω, I_D = 9A
Turn-On Rise Time	t_R	—	5.5	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	13.5	—		
Turn-Off Fall Time	t_F	—	4.6	—		
Reverse Recovery Time	t_{RR}	—	19.3	—	ns	I_F = 1.5A, di/dt = 100A/μs
Reverse Recovery Charge	Q_{RR}	—	8.6	—	nC	

Notes: 9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

Typical Characteristics - Q1 N-Channel

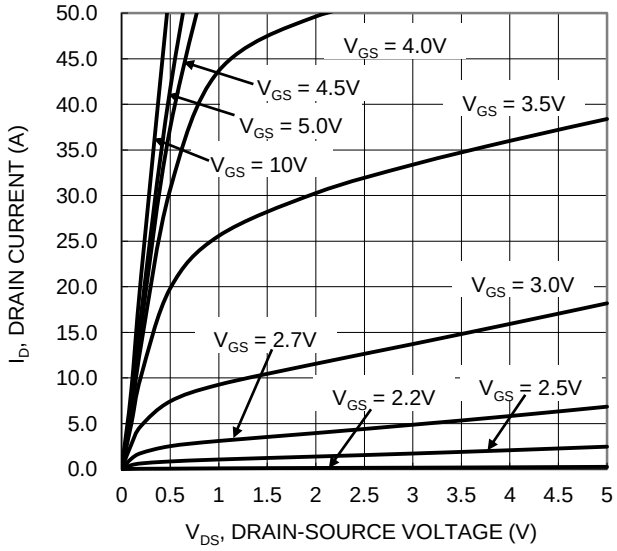


Figure 1. Typical Output Characteristic

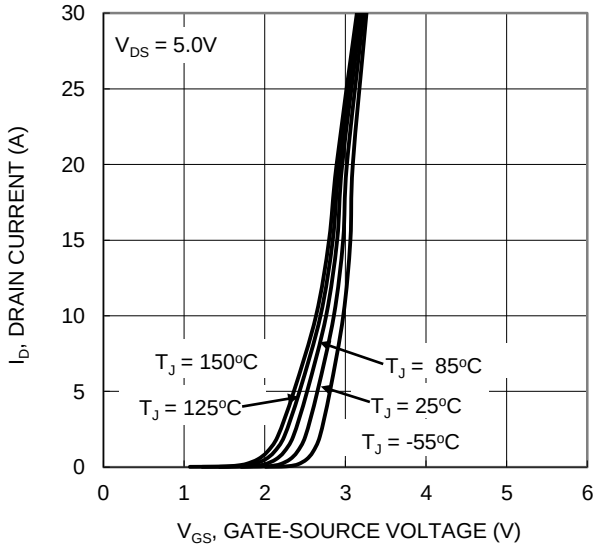


Figure 2. Typical Transfer Characteristic

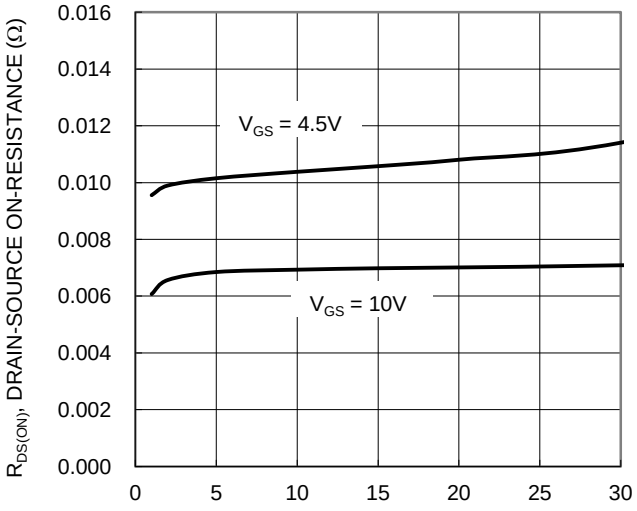


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

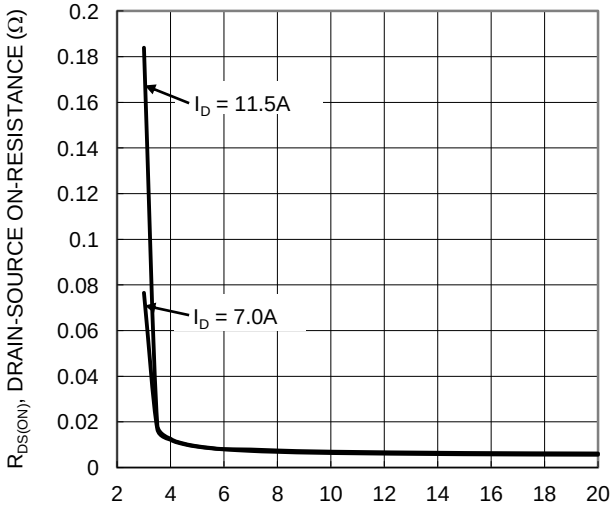


Figure 4. Typical Transfer Characteristic

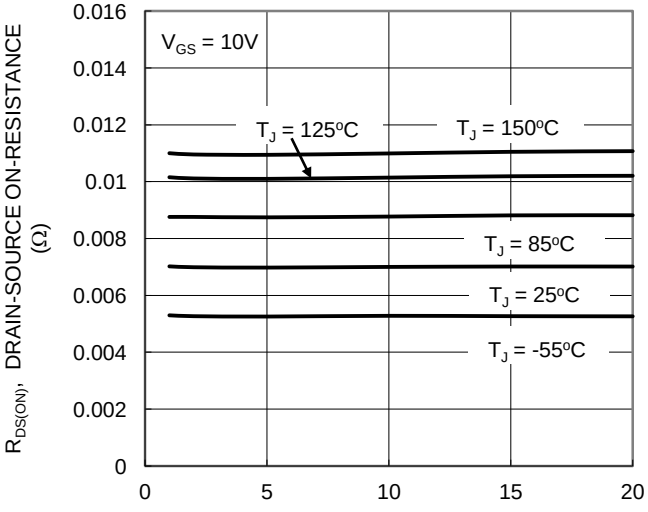


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

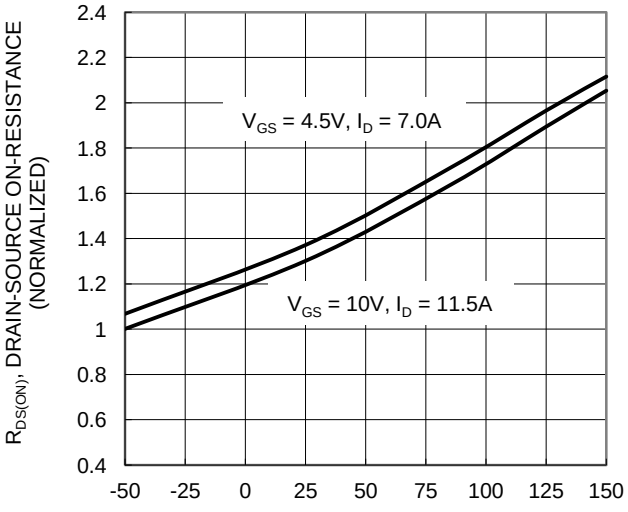


Figure 6. On-Resistance Variation with Temperature

Typical Characteristics - Q1 N-Channel (Cont.)

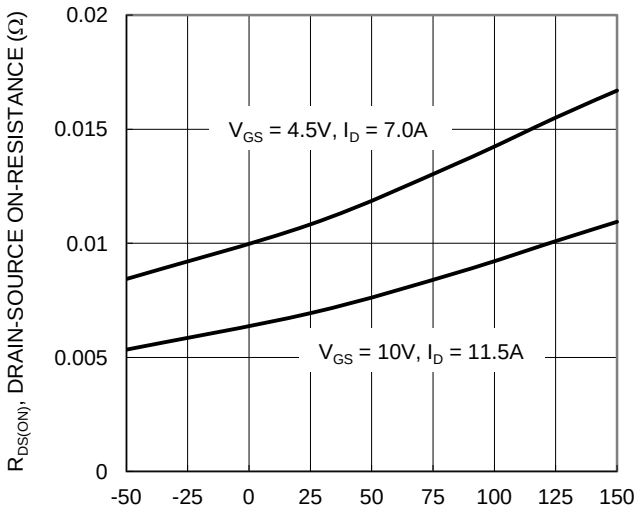


Figure 7. On-Resistance Variation with Temperature

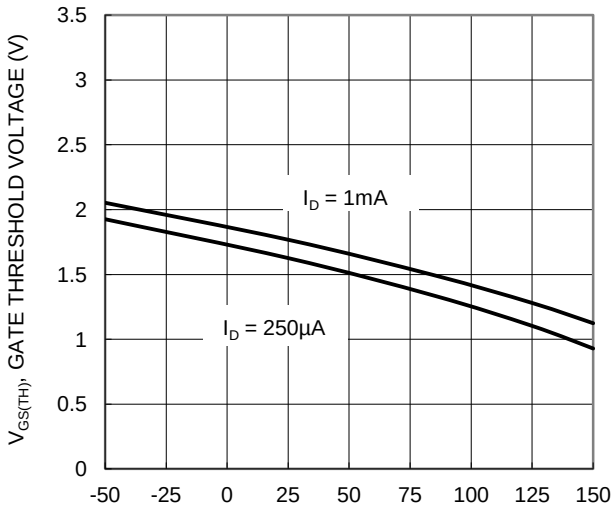


Figure 8.Gate Threshold Variation vs. JunctionTemperature

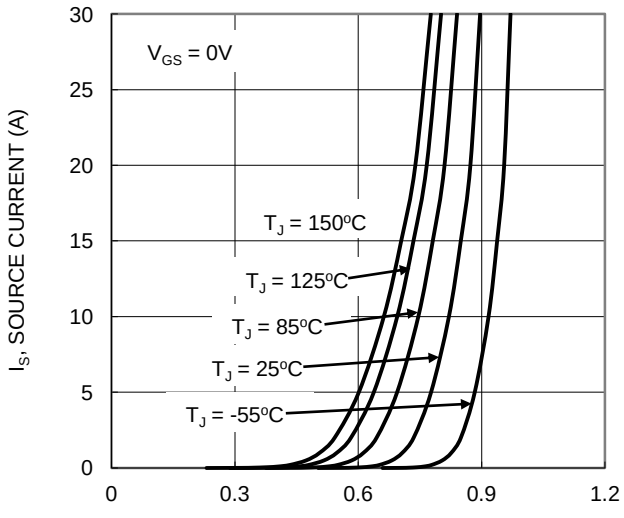


Figure 9. Diode Forward Voltage vs. Current

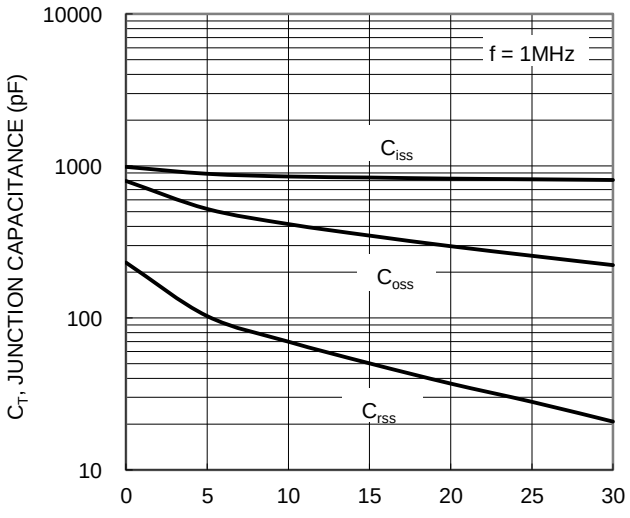


Figure 10. Typical Junction Capacitance

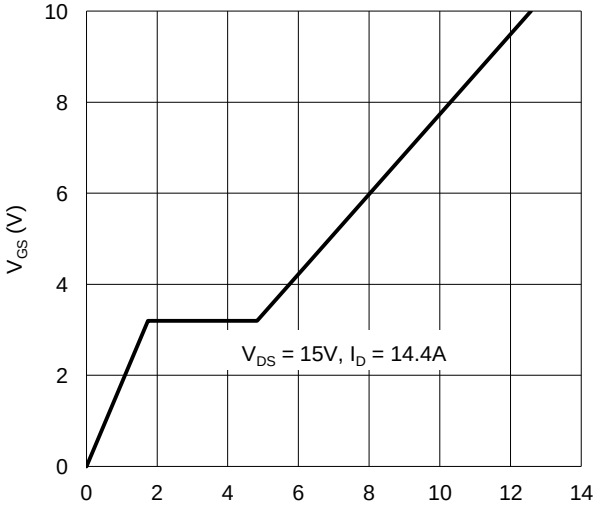


Figure 11. Gate Charge

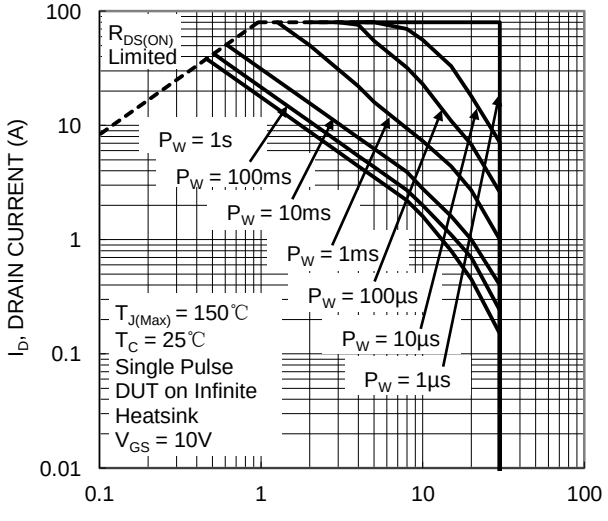


Figure 12. SOA, Safe Operation Area

Typical Characteristics - Q2 N-Channel

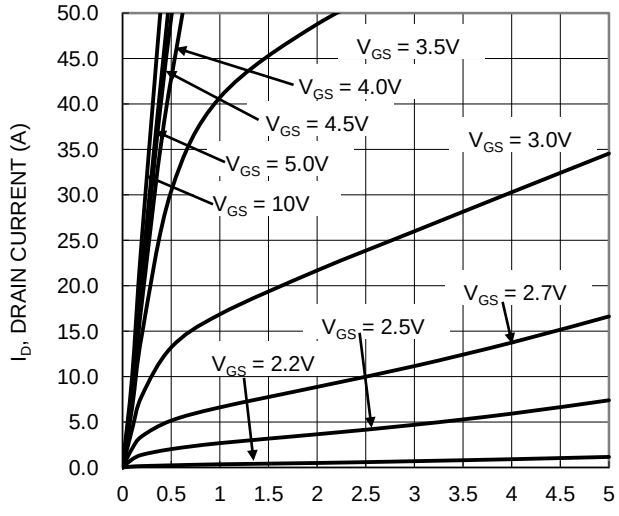


Figure 13. Typical Output Characteristic

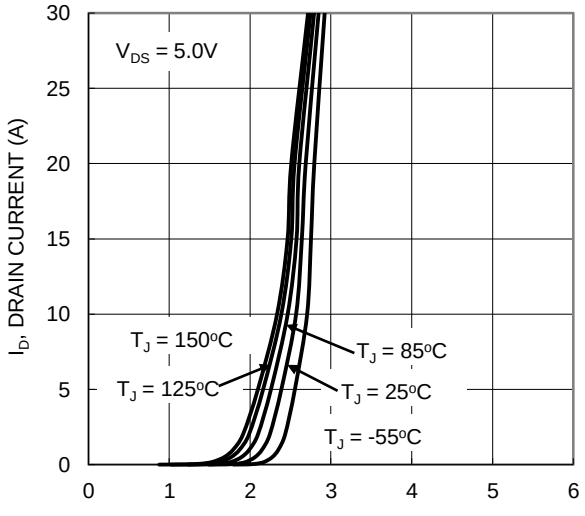


Figure 14. Typical Transfer Characteristic

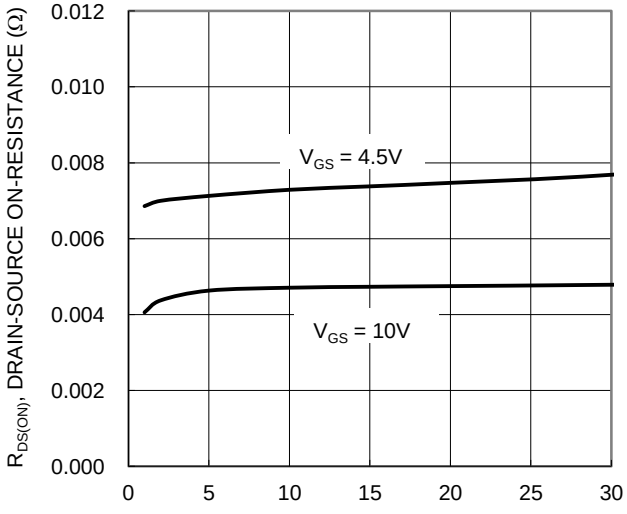


Figure 15. Typical On-Resistance vs. Drain Current and Gate Voltage

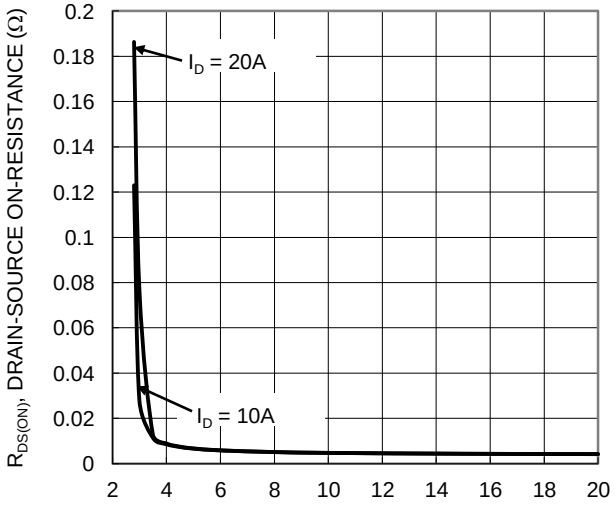


Figure 16. Typical Transfer Characteristic

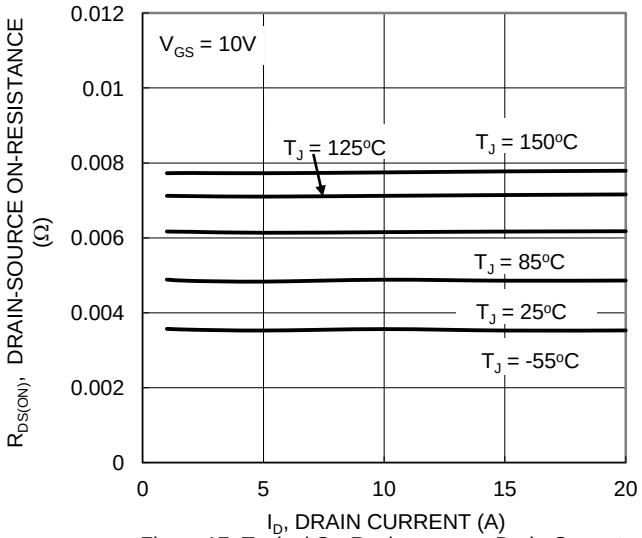


Figure 17. Typical On-Resistance vs. Drain Current and Temperature

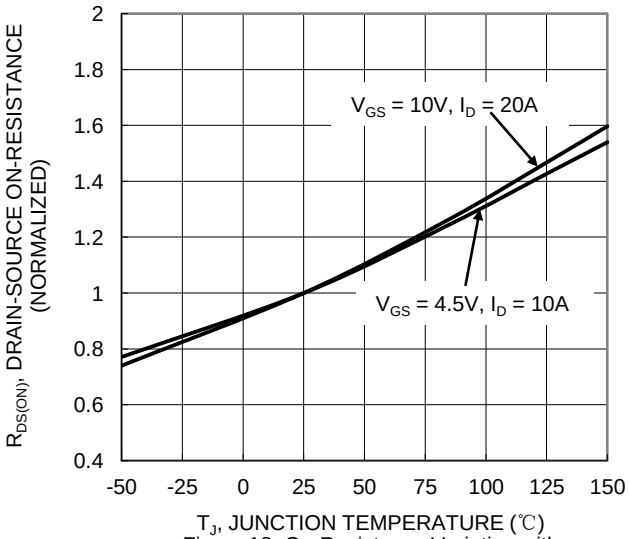


Figure 18. On-Resistance Variation with Temperature

Typical Characteristics - Q2 N-Channel (Cont.)

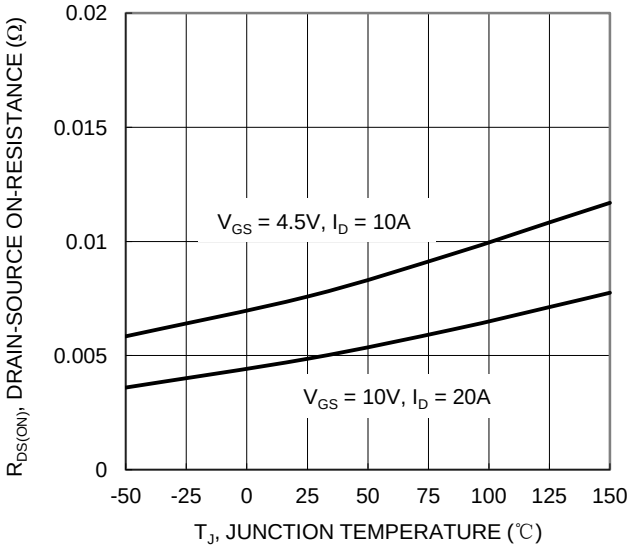


Figure 19. On-Resistance Variation with Temperature

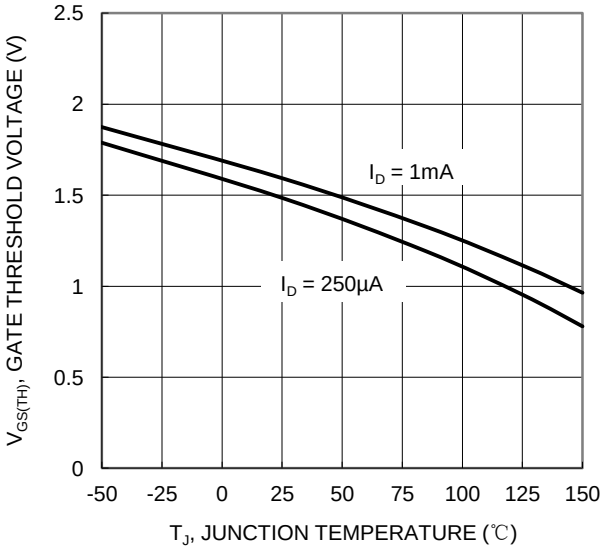


Figure 20. Gate Threshold Variation vs. JunctionTemperature

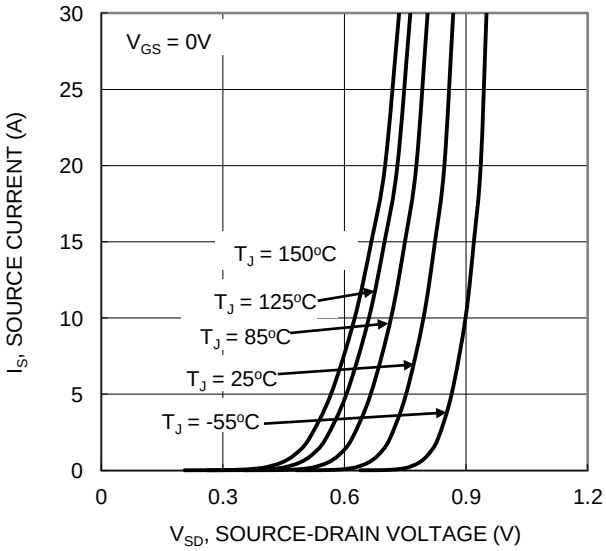


Figure 21. Diode Forward Voltage vs. Current

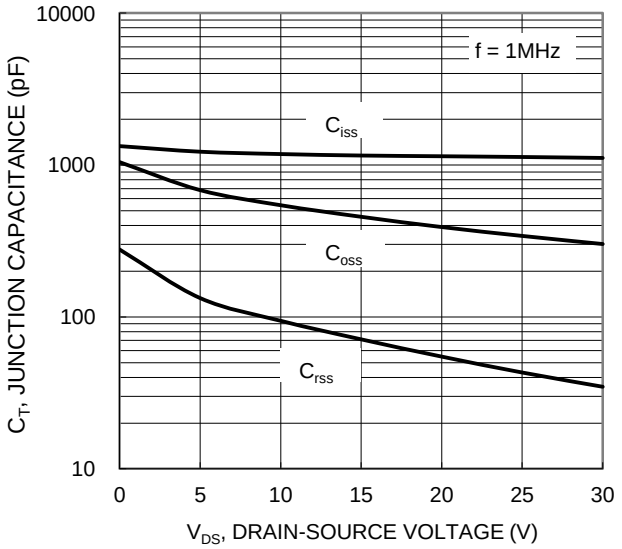


Figure 22. Typical Junction Capacitance

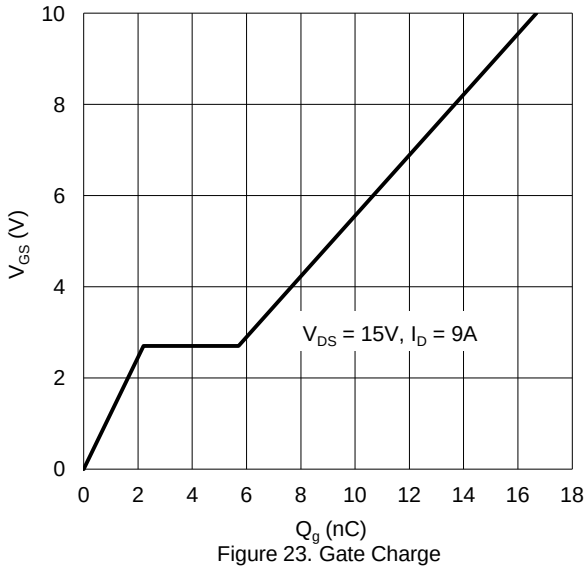


Figure 23. Gate Charge

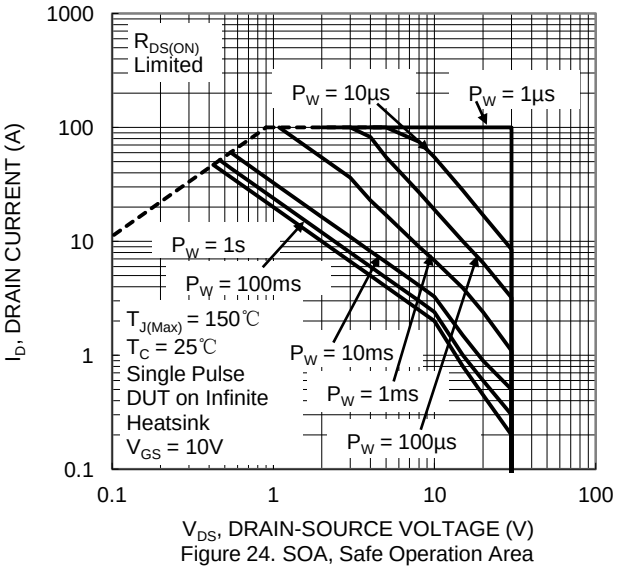


Figure 24. SOA, Safe Operation Area

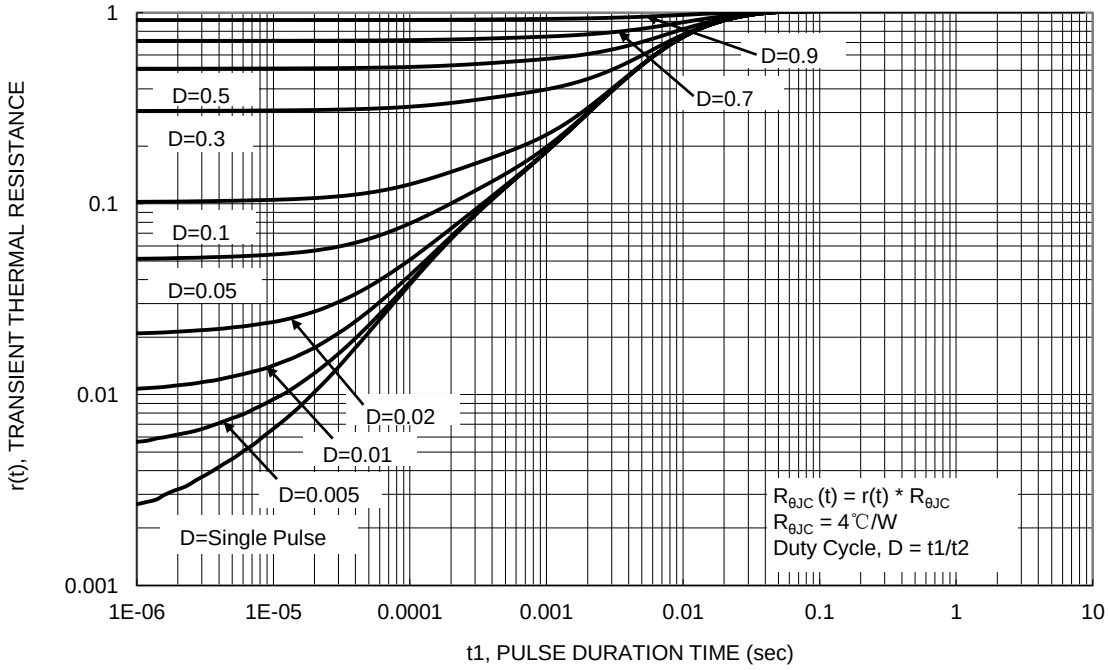
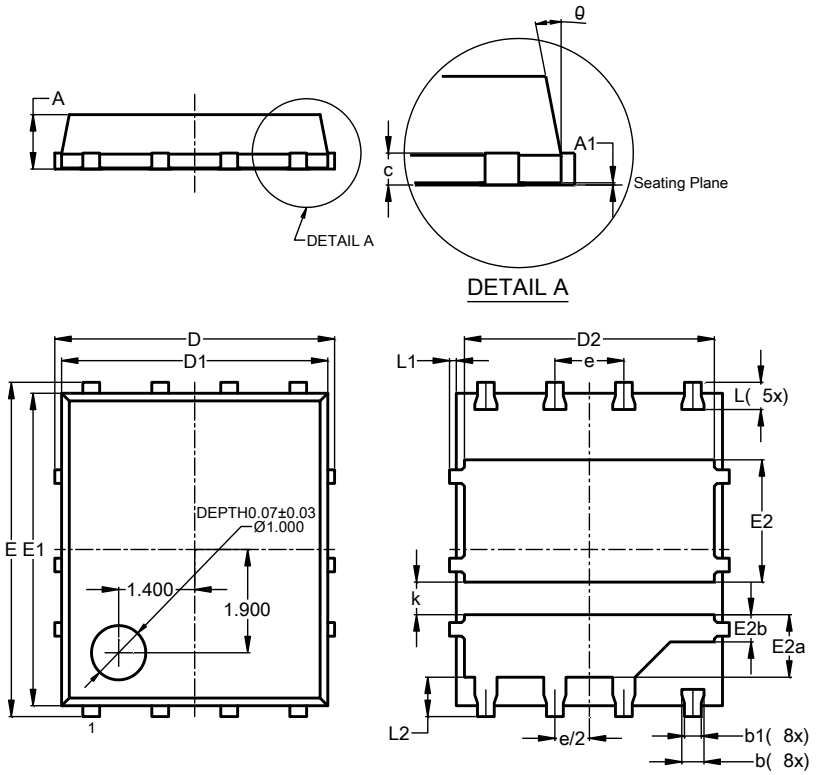


Figure 25. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8 (Type S)

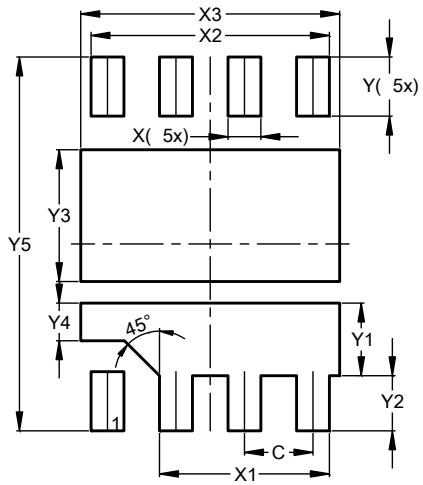


PowerDI5060-8 (Type S)			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0.00	0.05	--
b	0.33	0.46	0.41
b1	0.23	0.36	0.31
c	0.230	0.330	0.254
D	--	--	5.15
D1	4.70	5.10	4.90
D2	4.50	4.70	4.60
E	--	--	6.15
E1	5.55	5.95	5.75
E2	2.15	2.35	2.25
E2a	1.05	1.25	1.15
E2b	0.45	0.55	0.50
e	1.27BSC		
k	0.50	0.70	0.60
L	0.40	0.60	0.50
L1	0.00	0.20	0.125
L2	0.625	0.825	0.725
θ	10°	12°	11°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8 (Type S)



Dimensions	Value (in mm)
C	1.270
X	0.610
X1	3.150
X2	4.420
X3	4.800
Y	1.100
Y1	1.350
Y2	1.025
Y3	2.450
Y4	0.700
Y5	6.950

IMPORTANT NOTICE

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