Description

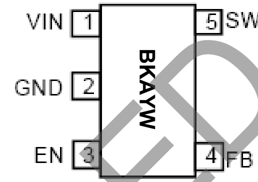
The PAM2305D is a step-down current-mode, DC-DC converter. At heavy load, the constant frequency PWM control per forms excellent stability and transient response. To ensure the longest battery life in portable applications, the PAM2305D provides a power-saving Pulse-Skipping Modulation (PSM) mode to reduce quiescent current under light load operation to save power.

The PAM2305D supports a range of input voltages from 2.5V to 5.5V, allowing the use of a single Li+/Li-polymer cell, multiple Alkaline/NiMH cell, USB, and other standard power sources. The output voltage is adjustable from 0.6V to the input voltage. All versions employ internal power switch and synchronous rectifier to minimize external part count and realize high efficiency. During shutdown, the input is disconnected from the output and the shutdown current is less than 0.1µA. Other key features include under-voltage lockout to prevent deep battery discharge.

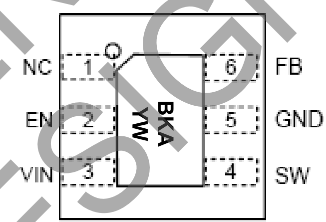
The PAM2305D is available in TSOT25, DFN2x2-6 pin and QFN3x3-16 pin packages.

Pin Assignments

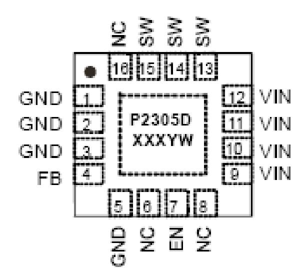
Top View
TSOT25



Top View
DFN 2x2 6L



Top View
QFN 3x3 16L



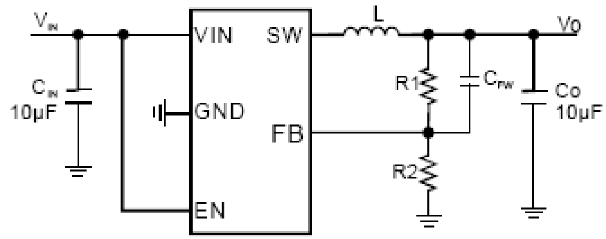
Features

- Efficiency up to 96%
- Only 40µA (Typ) Quiescent Current
- Output Current: Up to 1A
- Internal Synchronous Rectifier
- 1.5MHz Switching Frequency
- Soft Start
- Under-Voltage Lockout
- Short Circuit Protection
- Thermal Shutdown
- 5-Pin Small TSOT25, DFN2x2-6 Pin and QFN3x3-16 Pin Packages
- Pb-Free Packages

Applications

- Cellular Phone
- Portable Electronics
- Wireless Devices
- Cordless Phone
- Computer Peripherals
- Battery Powered Widgets
- Electronic Scales
- Digital Frame

Typical Applications Circuit

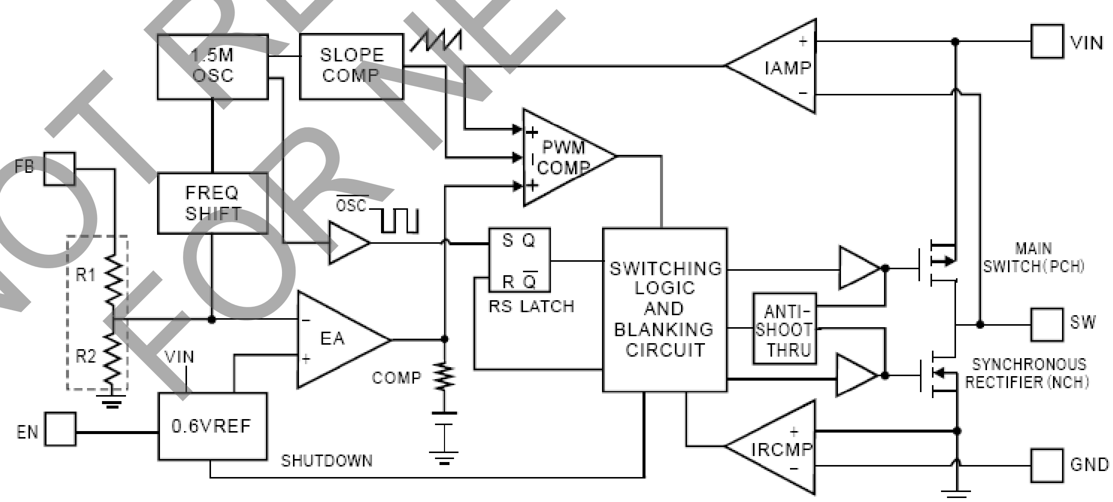


$$V_O = 0.6 \times \left(1 + \frac{R1}{R2}\right)$$

Pin Descriptions

Pin Name	Package Name			Function
	TSOT25	DFN2x2-6L	QFN3x3-16L	
VIN	1	3	9, 10, 11, 12	Chip main power supply pin.
GND	2	5	1, 2, 3, 5	Ground.
EN	3	2	7	Enable Control Input. Force this pin voltage above 1.5V, enables the chip, and below 0.3V shuts down the device.
FB	4	6	4	Feedback voltage to internal error amplifier, the threshold voltage is 0.6V.
SW	5	4	13, 14, 15	The drains of the internal main and synchronous power MOSFET.
NC	—	1	6, 8, 16	No connection.

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Parameter	Rating	Unit
Input Voltage	-0.3 to +6.0	V
EN, FB Pin Voltage	-0.3 to V_{IN}	V
SW Pin Voltage	-0.3 to (V_{IN} +0.3)	V
Junction Temperature	+150	°C
Storage Temperature Range	-65 to +150	°C
Soldering Temperature	300, 5s	°C

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Parameter	Rating	Unit
Supply Voltage	2.5 to 5.5	V
Operation Temperature Range	-40 to +85	°C
Junction Temperature Range	-40 to +125	

Thermal Information

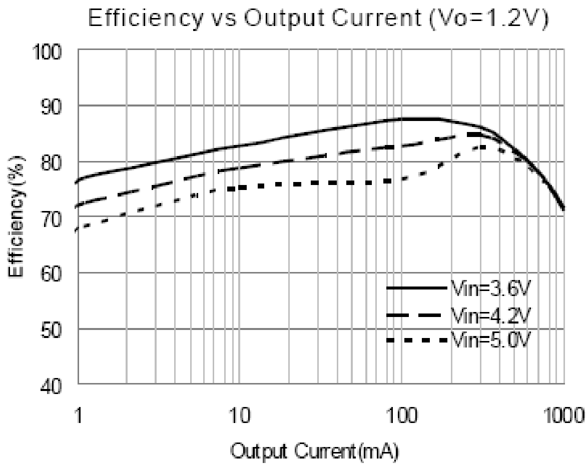
Parameter	Package	Symbol	Max	Unit
Thermal Resistance (Junction to Case)	TSOT25 (Note 1)	θ_{JC}	130	°C/W
	DFN2x2-6		25	
	QFN3x3-16		14	
Thermal Resistance (Junction to Ambient)	TSOT25	θ_{JA}	250	
	DFN2x2-6		68	
	QFN3x3-16		35	
Internal Power Dissipation	TSOT25	P_D	400	mW
	DFN2x2-6		980	
	QFN3x3-16		1470	

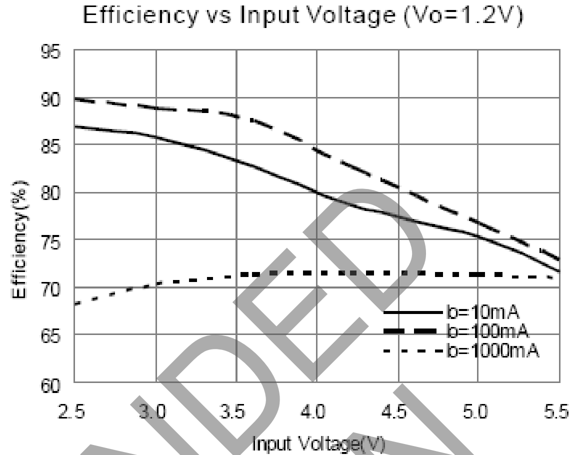
Note: 1. The maximun output current for TSOT25 package is limited by internal power dissipation capacity as described in Application Information here inafter.

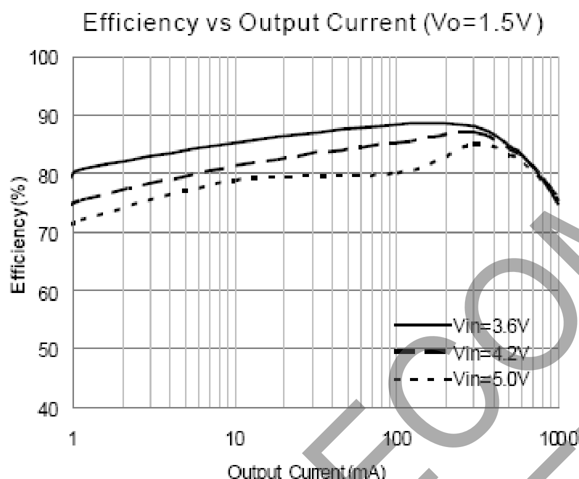
Electrical Characteristics (@T_A = +25°C, V_{IN} = 3.6V, V_O = 1.8V, C_{IN} = 10µF, C_{OUT} = 10µF, L = 4.7µH, unless otherwise specified.)

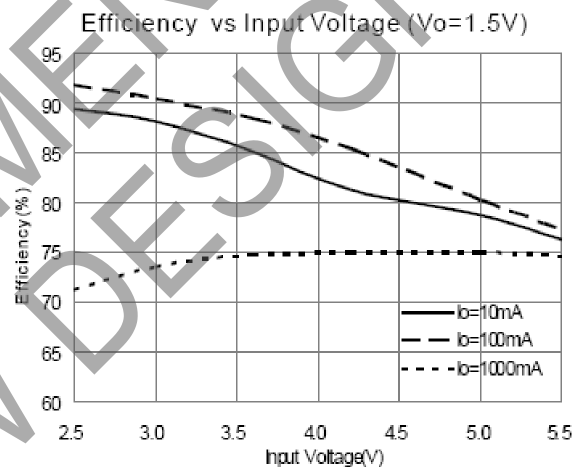
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Voltage Range	V_{IN}	—		2.5	—	5.5	V
Regulated Feedback Voltage	V_{FB}	Io = 100mA		0.588	0.6	0.612	V
Reference Voltage Line Regulation	ΔV_{FB}	—		—	0.3	—	%/V
Regulated Output Voltage Accuracy	V_O	I_O = 100mA		-3	—	+3	%
Peak Inductor Current	I_{PK}	V_{IN} = 3V,V_{FB} = 0.5V or V_O = 90%		—	1.5	—	A
Output Voltage Line Regulation	LNR	V_{IN} = 2.5V to 5V, I_O = 10mA		—	0.2	0.5	%/V
Output Voltage Load Regulation	LDR	I_O = 1mA to 800mA		—	1.5	—	%
Quiescent Current	I_Q	No load		—	40	70	µA
Shutdown Current	I_{SD}	V_{EN} = 0V		—	0.1	1	µA
Oscillator Frequency	f_{OSC}	V_O = 100%		1.2	1.5	1.8	MHz
		V_{FB} = 0V or V_O = 0V		—	500	—	kHz
Drain-Source On-State Resistance	$R_{DS(ON)}$	I_{DS} = 100mA	P MOSFET	—	0.3	0.45	Ω
			N MOSFET	—	0.35	0.5	Ω
SW Leakage Current	I_{LSW}	—		—	±0.01	1	µA
EN Threshold High	V_{EH}	—		1.5	—	—	V
EN Threshold Low	V_{EL}	—		—	—	0.3	V
EN Leakage Current	I_{EN}	—		—	±0.01	—	µA
Over Temperature Protection	OTP	—		—	+150	—	°C
OTP Hysteresis	OTH	—		—	+30	—	°C

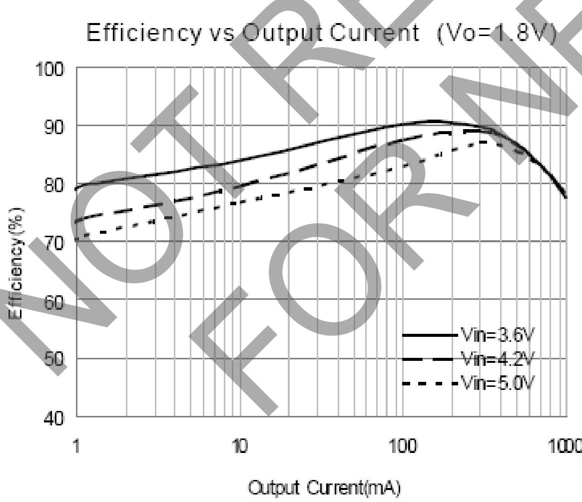
Typical Performance Characteristics (@T_A = +25°C, C_{IN} = 10µF, C_O = 10µF, L = 4.7µH, unless otherwise specified.)

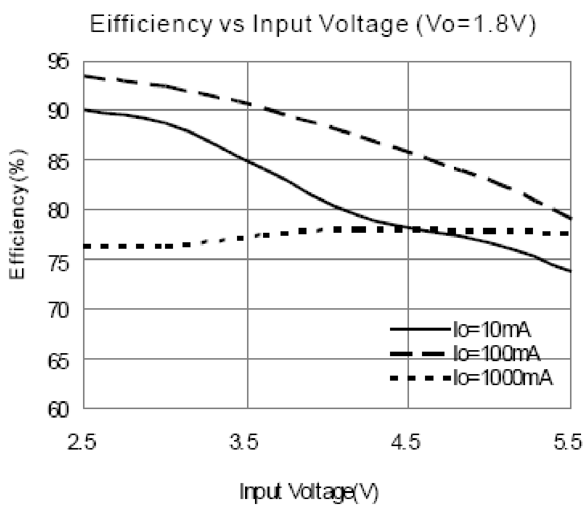




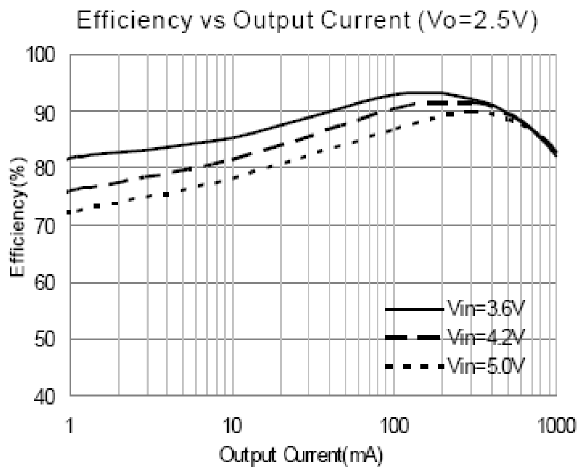


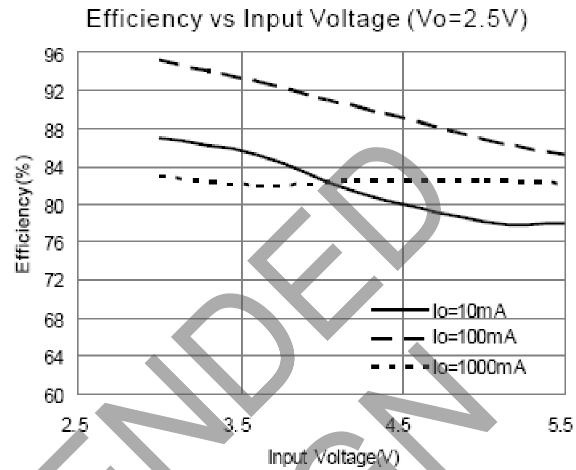


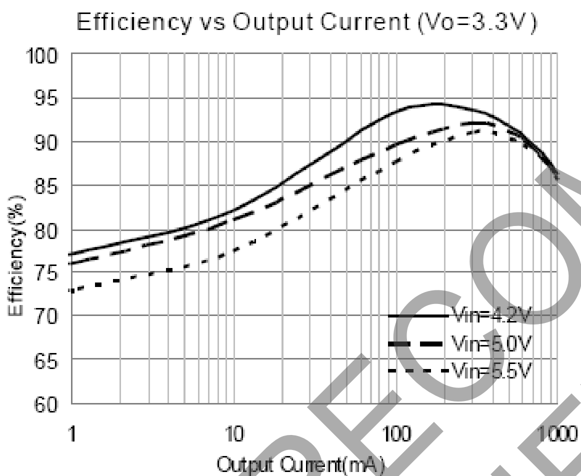


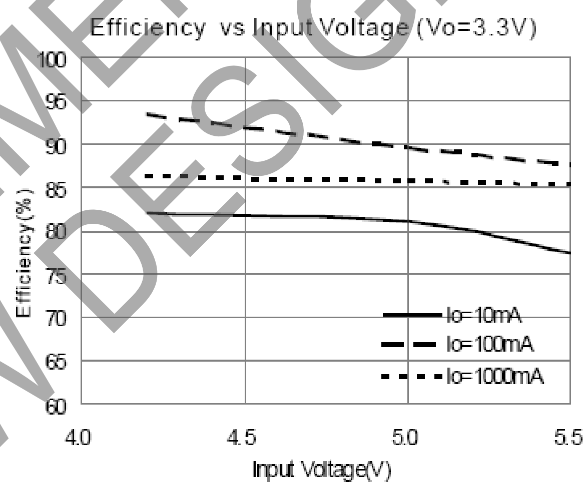


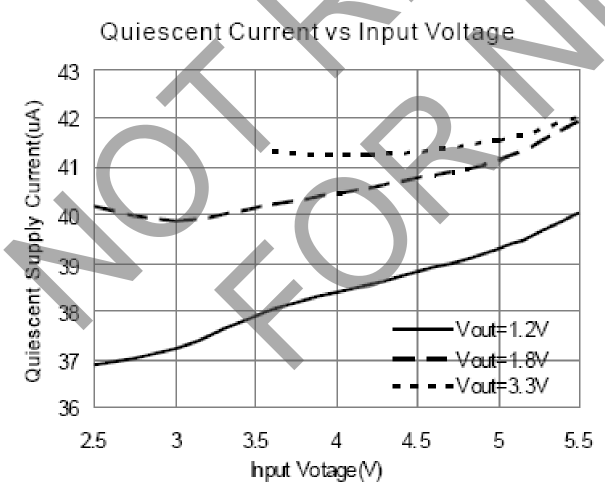
Typical Performance Characteristics (continued) (@T_A = +25°C, C_{IN} = 10μF, C_O = 10μF, L = 4.7μH, unless otherwise specified.)

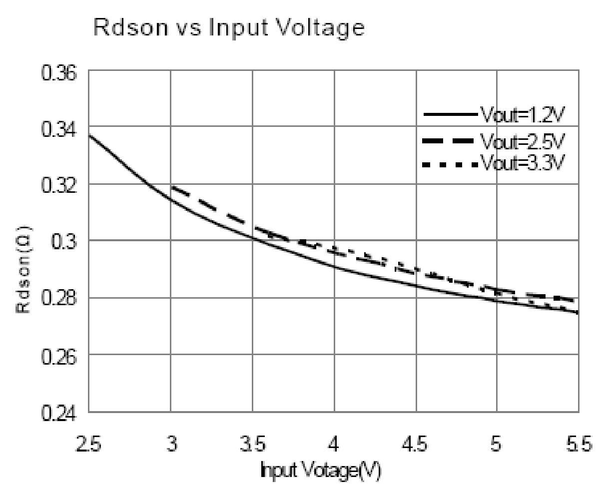




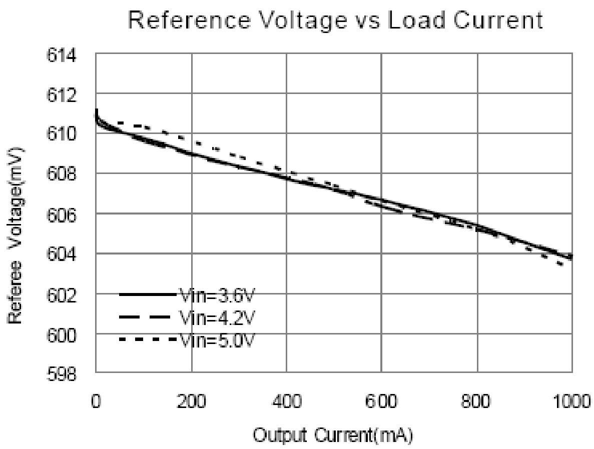


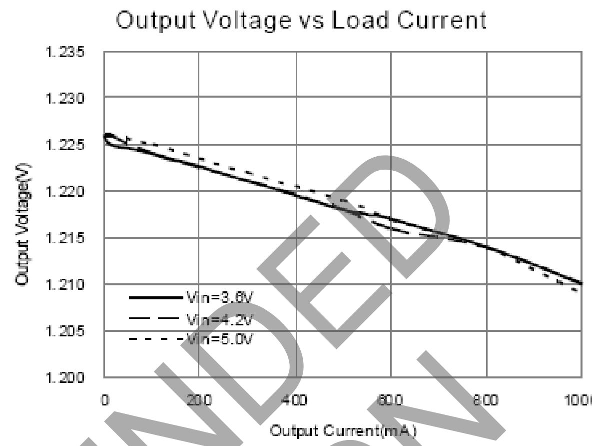


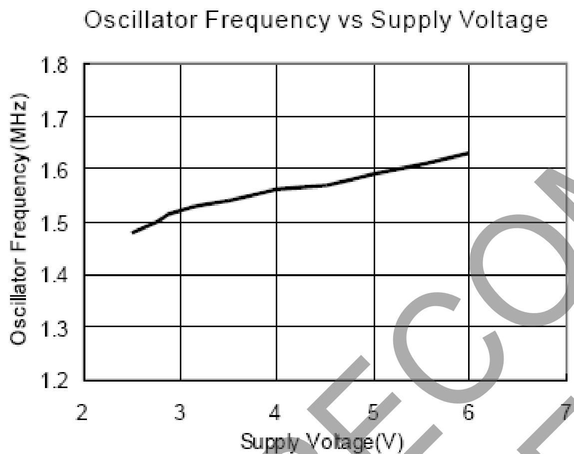


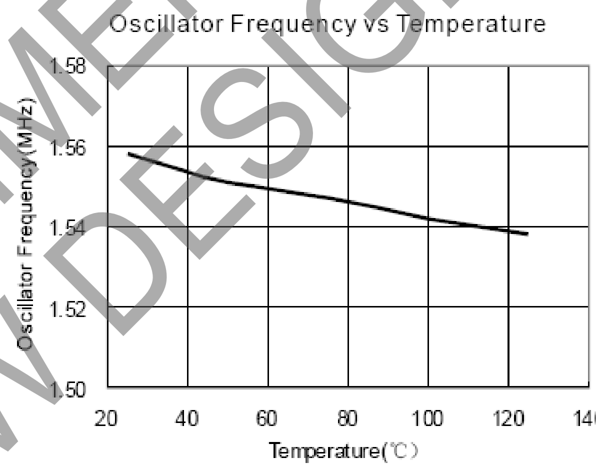


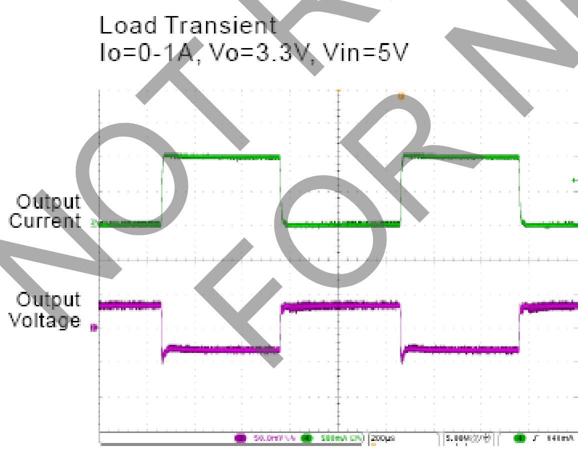
Typical Performance Characteristics (continued) (@T_A = +25°C, C_{IN} = 10µF, C_O = 10µF, L = 4.7µH, unless otherwise specified.)

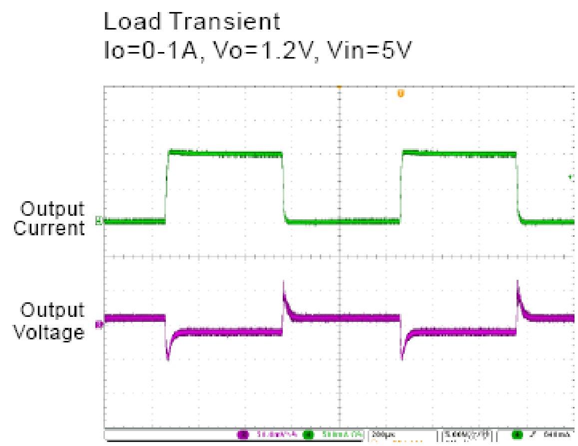












Application Information

The basic PAM2305D application circuit is shown in Page 2. External component selection is determined by the load requirement, selecting L first and then C_{IN} and C_{OUT}.

Inductor Selection

For most applications, the value of the inductor will fall in the range of 1μH to 4.7μH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in Equation 1. A reasonable starting point for setting ripple current is ΔI_L = 400mA (40% of 1A).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad \text{Equation (1)}$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 1.4A rated inductor should be enough for most applications (1A + 400mA). For better efficiency, choose a low DC-resistance inductor.

V_O	1.2V	1.5V	1.8V	2.5V	3.3V
L	2.2μH	2.2μH	2.2μH	4.7μH	4.7μH

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{OMAX} \frac{\left[V_{OUT}(V_{IN} - V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR).

Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the I_{RIPPLE} (P-P) requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta i_L \left(ESR + \frac{1}{8f\,C_{OUT}}\right)$$

Where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Using ceramic capacitors can achieve very low output ripple and small circuit size.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Thermal Consideration

Thermal protection limits power dissipation in the PAM2305D. When the junction temperature exceeds 150°C, the OTP (Over Temperature Protection) starts the thermal shutdown and turns the pass transistor off. The pass transistor resumes operation after the junction temperature drops below +120°C.

For continuous operation, the junction temperature should be maintained below +125°C.
The power dissipation is defined as:

$$P_D = I_O^2 \frac{V_O R_{DS(ON)H} + (V_{IN} - V_O) R_{DS(ON)L}}{V_{IN}} + (t_{SW} F_S I_O + I_Q) V_{IN}$$

I_Q is the step-down converter quiescent current. The term tsw is used to estimate the full load step-down converter switching losses.

Application Information (continued)

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_D = I_O^2 R_{DS(ON)H} + I_Q V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surrounding airflow and temperature difference between junction and ambient. The maximum power dissipation can be calculated by the following formula:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where $T_{J(MAX)}$ is the maximum allowable junction temperature +125°C. T_A is the ambient temperature and θ_{JA} is the thermal resistance from the junction to the ambient. Based on the standard JEDEC for a two layers thermal test board, the thermal resistance θ_{JA} of TSOT25 package is 250°C/W, DFN2X2 102°C/W and QFN3X3 68°C/W, respectively. The maximum power dissipation at T_A = +25°C can be calculated by following formula:

SOT-25 package:

P = (125°C - 25°C)/250°C/W = 0.4W

DFN2*2 package:

P = (125°C - 25°C)/102°C/W = 0.984W

QFN3*3 package:

P = (125°C - 25°C)/68°C/W = 1.47W

Setting the Output Voltage

The internal reference is 0.6V (Typical). The output voltage is calculated as below:

$$V_O = 0.6 \times \left(1 + \frac{R1}{R2}\right)$$

The output voltage is given by Table 1.

Table 1: Resistor selection for output voltage setting.

V_O	R1	R2
1.2V	100k	100k
1.5V	150k	100k
1.8V	200k	100k
2.5V	380k	120k
3.3V	540k	120k

100% Duty Cycle Operation

As the input voltage approaches the output voltage, the converter turns the P-Channel transistor continuously on. In this mode the output voltage is equal to the input voltage minus the voltage drop across the P-Channel transistor:

$$V_{OUT} = V_{IN} - I_{LOAD} (R_{DS(ON)} + R_L)$$

where $R_{DS(ON)}$ = P-Channel switch ON resistance, I_{LOAD} = Output current, R_L = Inductor DC resistance.

UVLO and Soft-Start

The reference and the circuit remain reset until the V_{IN} crosses its UVLO threshold.

The PAM2305D has an internal soft-start circuit that limits the in-rush current during start-up. This prevents possible voltage drops of the input voltage and eliminates the output voltage overshoot. The soft-start acts as a digital circuit to increase the switch current in several steps to the P-Channel current limit (1500mA).

Short Circuit Protection

The switch peak current is limited cycle-by-cycle to a typical value of 1500mA. In the event of an output voltage short circuit, the device operates with a frequency of 400kHz and minimum duty cycle, therefore the average input current is typically 200mA.

Application Information (continued)

Thermal Shutdown

When the die temperature exceeds +150°C, a reset occurs and the reset remains until the temperature decrease to +120°C, at which time the circuit can be restarted.

PCB Layout Check List

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the PAM2305D. These items are also illustrated graphically in Figure 1. Check the following in your layout:

1. The power traces, consisting of the GND trace, the SW trace and the V_{IN} trace should be kept short, direct and wide.
2. Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider R1/R2 must be connected between the (+) plate of C_{OUT} and ground.
3. Does the (+) plate of C_{IN} connect to V_{IN} as closely as possible? This capacitor provides the AC current to the internal power MOSFETs.
4. Keep the switching node, SW, away from the sensitive V_{FB} node.
5. Keep the (–) plates of C_{IN} and C_{OUT} as close as possible.

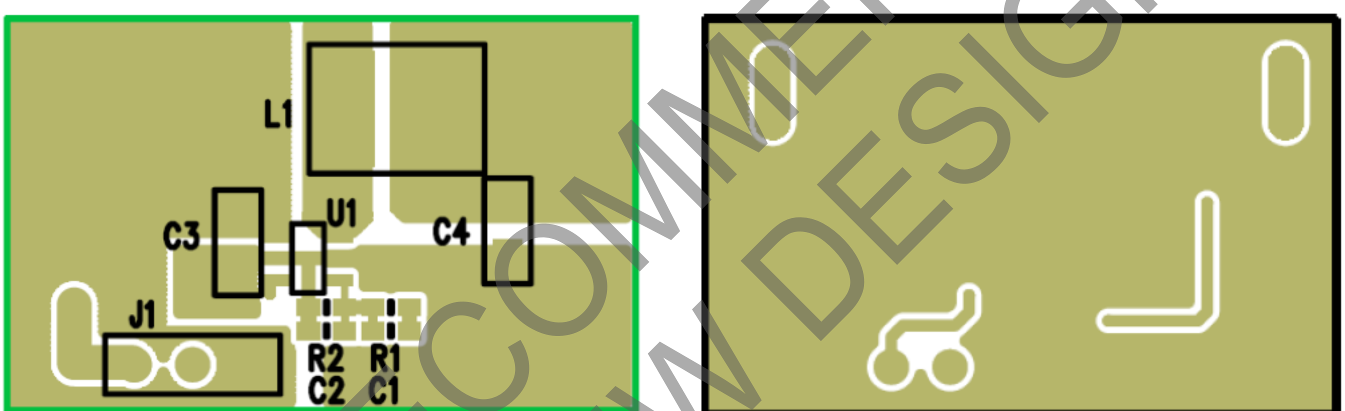


Figure 1. PAM2305D Suggested Layout

Ordering Information

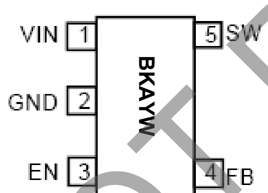
PAM2305D X X xxx

Package Type	Number of Pins	Output Voltage
A: TSOT25	B: 5	ADJ: Adjustable
J: QFN3x3	E: 16	
G: DFN2x2	F: 6	

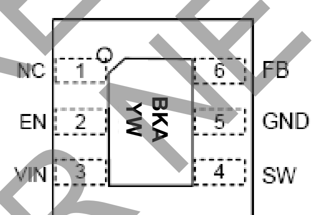
Part Number	Output Voltage	Part Marking	Package Type	Standard Package
PAM2305DABADJ	ADJ	BKAYW	TSOT25	3000 Units/Tape&Reel
PAM2305DJEADJ	ADJ	P2305D	QFN3x3	3000 Units/Tape&Reel
PAM2305DGFADJ	ADJ	BKAYW	DFN2x2-6	3000 Units/Tape&Reel

Marking Information

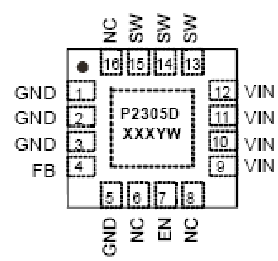
Top View
TSOT25



Top View
DFN 2x2 6L



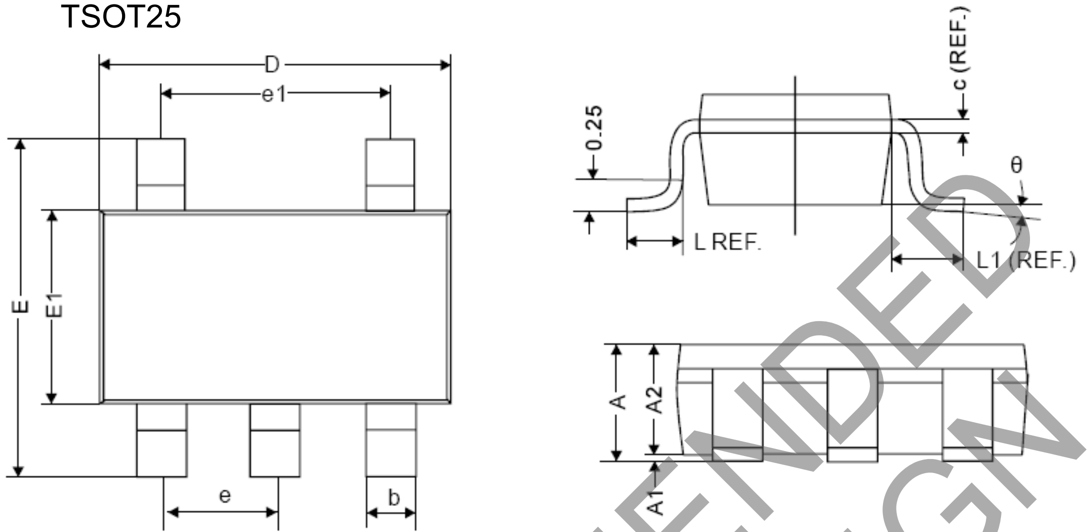
Top View
QFN 3x3 16L



BK: Product Code of PAM2305D
Y: Year
W: Week
X: Internal Code

Package Outline Dimensions (All dimensions in mm.)

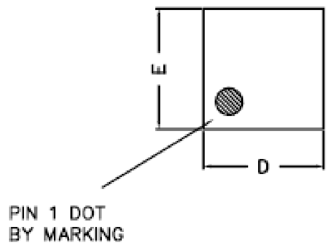
TSOT25



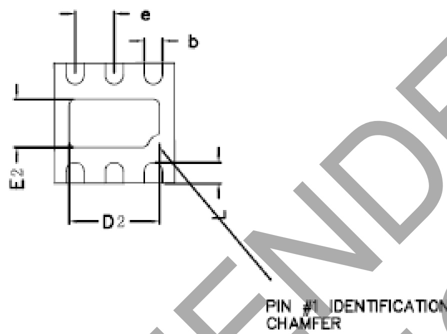
REF.	Millimeter	
	Min	Max
A	1.10 MAX	
A1	0	0.10
A2	0.70	1
c	0.12 REF.	
D	2.70	3.10
E	2.60	3.00
E1	1.40	1.80
L	0.45 REF.	
L1	0.60 REF.	
θ	0°	10°
b	0.30	0.50
e	0.95 REF.	
e1	1.90 REF.	

Package Outline Dimensions (continued) (All dimensions in mm.)

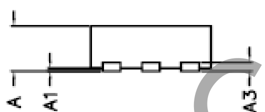
DFN 2x2



TOP VIEW



BOTTOM VIEW

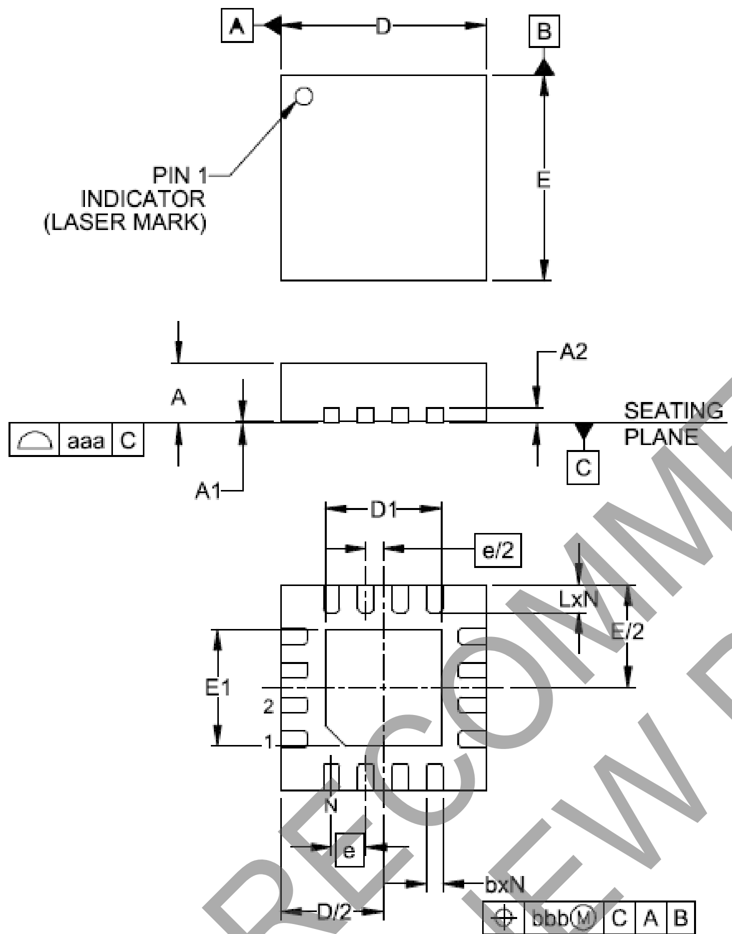


SIDE VIEW

COMMON DIMENSIONS(MM)			
PKG.	W: VERY VERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.2 REF.		
D	1.95	2.00	2.05
E	1.95	2.00	2.05
b	0.25	0.30	0.35
L	0.25	0.35	0.45
D2	1.35	1.50	1.60
E2	0.65	0.80	0.90
e	0.65 BSC		

Package Outline Dimensions (continued) (All dimensions in mm.)

3x3 mm QFN 16



DIMENSIONS (Millieters)			
	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.20	
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D1	1.55	1.70	1.80
E	2.90	3.00	3.10
E1	1.55	1.70	1.80
e		0.50BSC	
L	0.30	0.40	0.50
N		16	
aaa		0.08	
bbb		0.10	

Notes:
2. Controlling dimensions are in millimeters (angles in degress).
3. Coplanarity applies to the exposed pad as well as the terminals.
4. DAP is 1.90 x 1.90mm.