12W STEREO CLASS-D AUDIO AMPLIFIER WITH SYNCHRONOUS BOOST, SSM AND EXTERNAL AUDIO FEEDBACK

Description

The PAM8965 is an extremely high-efficiency Class-D stereo audio power amplifier with an integrated synchronous boost converter. The PAM8965 can drive two channels with 12W each into 4Ω speakers.

The integrated amplifier can achieve system efficiency of 92% (at V_{BAT} = 7.4V). The device consumes exceptionally low quiescent current (10mA at V_{BAT} = 7.4V) and very low shutdown current (0.7μA).

The integrated current-mode boost converter provides regulated power to a feature-laden Class-D stereo amplifier. These include:

Spread spectrum modulation (SSM) for EMI suppression (audio and boost), which enables the use of inexpensive ferrite bead filters.

Non-clipping power limit, which uses 41-step automatic gain control.

Thermal foldback, which reduces output power as the chip heats up.

External audio feedback pins, which allow for customization of sound by using feedback network design. Alternatively, these pins can be used for Kelvin connection to speaker terminals.

GAIN pin to program audio gain at 0.5dB steps such that external resistors are not required to adjust gain, which can result in gain error.

Out-of-audio switching for the boost converter, which minimizes audible noise coming from components on the board.

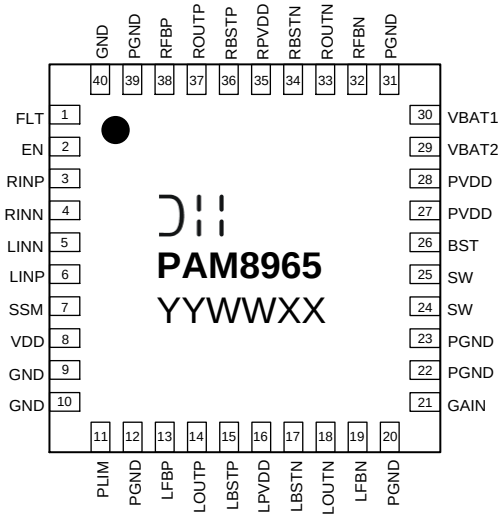
Protection features include under-voltage and over-voltage protection on VBAT, over-voltage protection on PVDD, short circuit protection on all audio outputs, cycle-by-cycle current limit on boost converter, thermal shutdown of the entire system, DC protection for speakers, and an FLT pin that provides a fault flag.

Features

- Operates from 2.8V to 8.5V Supply
- 2 × 12W (10% THD+N) into 4Ω Load with V_{BAT} = 7.4V (2SxP)
- 2 × 8W (10% THD+N) into 6Ω Load with V_{BAT} = 3.7V (1SxP)
- Auto Gain Control Responds to:
- Thermal Foldback
- Non-Clip Power Limit
- GAIN Pin
- Externally Adjustable Gain from 26dB to 6dB with 0.5dB Steps
- Exceptionally High Overall System Efficiency (92% @ V_{BAT} = 7.4V)
- Very Low I_Q = 10mA (V_{BAT} = 7.4V) for Boost + Stereo
- Very Low Shutdown Current = 0.7μA
- DC Protection for Speaker
- Auto-Recovery on Short-Circuit Protection & Thermal Shutdown
- External Audio Feedback Pins
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Pin Assignments

(Top View)



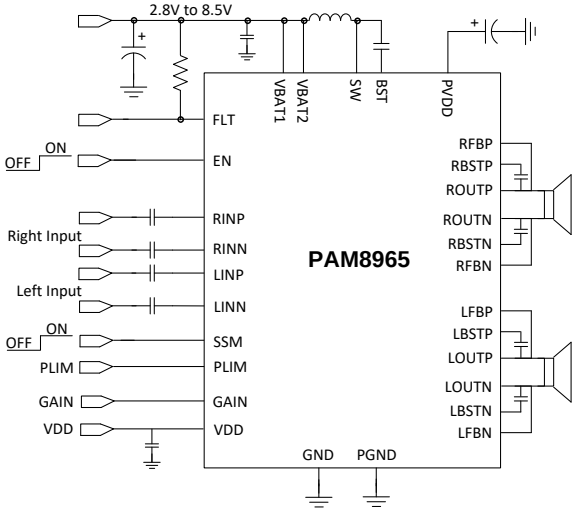
W-QFN5050-40 (Type US)

Applications

- Portable electronics
- Bluetooth speakers
- Wireless speakers
- Music instruments
- High-capacitance piezo actuator drives
- Virtual reality 3D active feedbacks
- PDAs, GPS, game machines

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



Pin Descriptions

Pin Number	Pin Name	I/O/P	Description
1	FLT	O	Fault flag. Open-drain output to signal system faults (VBAT UVLO or OVLO, OTP, DC input, audio SCP)
2	EN	I	Chip enable. High = ON, Low = OFF. Do not float this pin.
3	RINP	I	Right channel audio input – Positive
4	RINN	I	Right channel audio input – Negative
5	LINN	I	Left channel audio input – Negative
6	LINP	I	Left channel audio input – Positive
7	SSM	I	Spread spectrum modulation. High = ON, Low = OFF. Do not float this pin.
8	VDD	O	Internal 5V LDO
9, 10	GND	—	Analog signal ground
11	PLIM	I	Non-clip power limit setting. PLIM = VDD disables power limit. Do not float this pin.
12, 20	PGND	—	Power ground for left channel
13	LFBP	I	Left channel feedback – Positive. Short to LOUTP. Kelvin connect to speaker for higher performance.
14	LOUTP	O	Left channel audio output – Positive
15	LBSTP	P	Left channel boot-strap supply for high-side – Positive
16	LPVDD	P	Left channel power supply for Class-D H-bridge
17	LBSTN	P	Left channel boot-strap supply for high-side – Negative
18	LOUTN	O	Left channel audio output – Negative
19	LFBN	I	Left channel feedback – Negative. Short to LOUTN. Kelvin connect to speaker for higher performance.
21	GAIN	I	Audio channel gain setting. Do not float this pin. 4.5V or above = 26dB (maximum gain setting). Then every 100mV is 0.5dB step, e.g., 4.4V = 25.5dB, 4.3V = 25dB, etc. 0.5V or below = 6dB (minimum gain setting)
22, 23	PGND	—	Power ground for boost converter
24, 25	SW	O	Boost converter's switching node
26	BST	P	Boost converter's boot-strap supply
27, 28	PVDD	O	Boost converter's output. Connect this to pin 16 and pin 35.
29	VBAT2	P	Battery supply input for boost converter. See *Application Information* for decoupling requirement.
30	VBAT1	P	Battery supply input for system. See *Application Information* for decoupling requirement.
31, 39	PGND	—	Power ground for right channel
32	RFBN	I	Right channel feedback – Negative. Short to ROUTN. Kelvin connect to speaker for higher performance.
33	ROUTN	O	Right channel audio output – Negative
34	RBSTN	P	Right channel boot-strap supply for high-side – Negative
35	RPVDD	P	Right channel power supply for Class-D H-bridge
36	RBSTP	P	Right channel boot-strap supply for high-side – Positive
37	ROUTP	O	Right channel audio output – Positive
38	RFBP	I	Right channel feedback – Positive. Short to ROUTP. Kelvin connect to speaker for higher performance.
40	GND	—	Connect to system ground

Functional Block Diagram

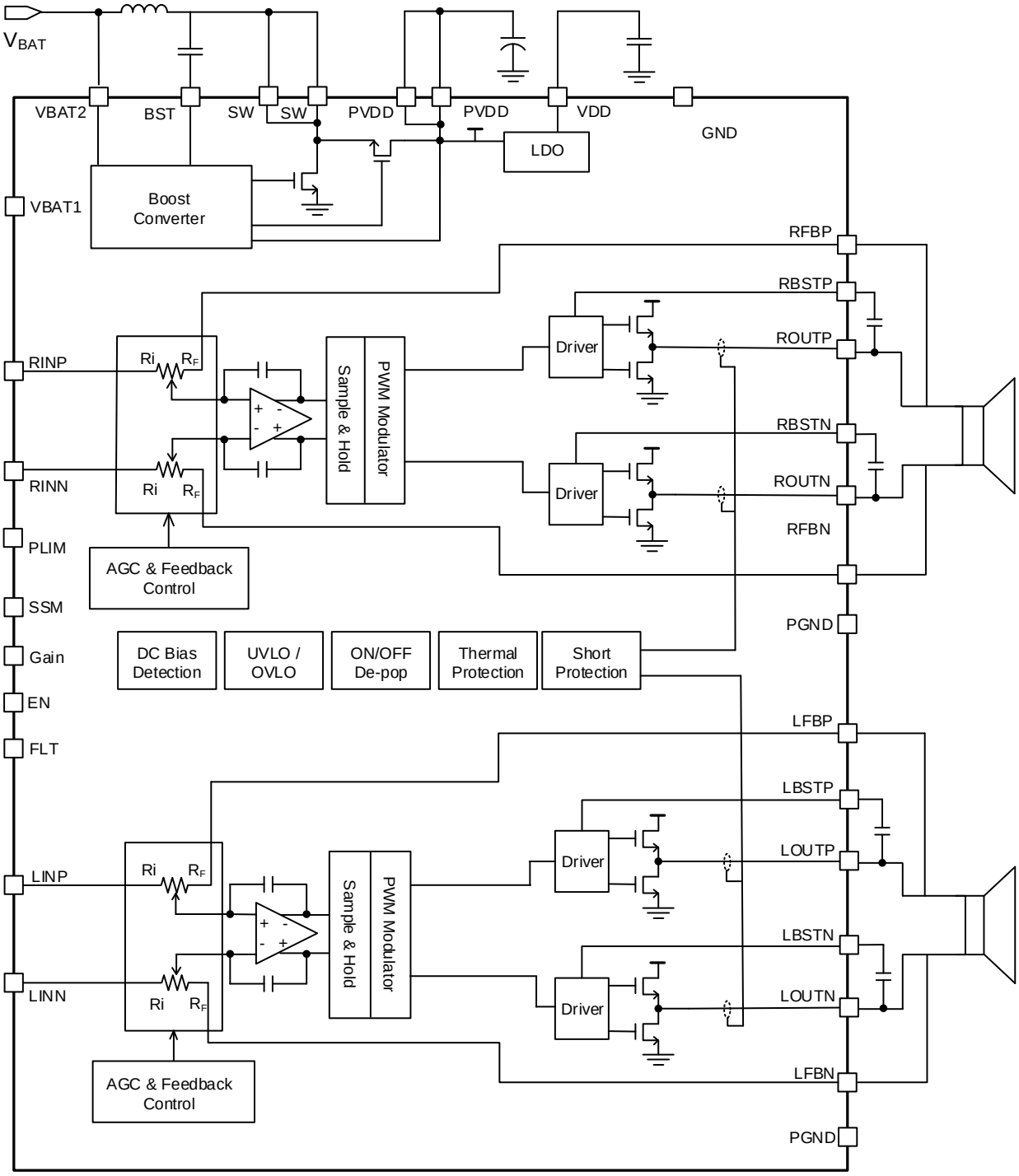


Figure 1. PAM8965 Block Diagram

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
V_{BAT}	Supply Voltage (Pins VBAT1, VBAT2)	-0.3 to +9.0	V
V_{RINP}, V_{RINN}, V_{LINP}, V_{LINN}	Audio Input Voltage	-0.3 to +5.5	V
V_{PLIM}, V_{GAIN}, V_{SSM}	Control Input Voltage	-0.3 to +6.0	V
V_{EN}	Control Input Voltage	-0.3 to V_{BAT}	V
T_{J_MAX}	Maximum Operating Junction Temperature (Note 5)	-40 to +150	°C
T_{STG}	Storage Temperature Range	-40 to +150	°C
HBM	Human Body Model	±2000	V
CDM	Charged Device Model	±1000	V

Note 4. Stresses greater than the *Absolute Maximum Ratings* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{BAT}	Supply Voltage (Pins VBAT1, VBAT2)	2.8	8.5	V
V_{RINP}, V_{RINN}, V_{LINP}, V_{LINN}	Audio Input Voltage	0.0	5.0	V
V_{PLIM}, V_{GAIN}, V_{SSM}	Control Input Voltage	0.0	5.5	V
V_{EN}	Control Input Voltage	0.0	V_{BAT}	V
R_{LMIN}	Minimum Load Resistance (V_{BAT} ≤ 5.0V)	6	—	Ω
	Minimum Load Resistance (V_{BAT} > 5.0V)	4	—	
T_A	Operating Free-Air Temperature Range	-40	+85	°C
T_J	Operating Junction Temperature Range (Note 5)	-40	+125	°C

Note 5. The PAM8965 incorporates an exposed thermal pad on the underside of the chip, which acts as a heatsink. The exposed pad must be connected to a thermally dissipating Cu plane on the PCB for adequate power dissipation. Failure to do so may result in the device going into thermal shutdown.

Thermal Information

Parameter	Symbol	Package	Rating	Unit
Thermal Resistance (Junction to Ambient)	θ_{JA}	W-QFN5050-40 (Type US)	33	°C/W
Thermal Resistance (Junction to Case)	θ_{JC}	W-QFN5050-40 (Type US)	10	°C/W

Electrical Characteristics (V_{BAT} = 7.4V, T_A = +25°C, R_L = 4Ω + 2 × 33μH, V_{PLIM} = V_{GAIN} = V_{DD}, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{BAT}	Input Supply Voltage	—	2.8	—	8.5	V
V_{IH}	High-Level Input Voltage	EN, SSM	1.5	—	—	V
V_{IL}	Low-Level Input Voltage	EN, SSM	—	—	0.5	V
η	System Efficiency (Boost + Stereo)	V_{BAT} = 7.4V, R_L = 4Ω, P_O = 5W, f = 1kHz	—	92	—	%
		V_{BAT} = 3.7V, R_L = 6Ω, P_O = 3W, f = 1kHz	—	86	—	
I_Q	Quiescent Current	V_{BAT} = 7.4V, No Load	—	10	—	mA
		V_{BAT} = 3.7V, No Load	—	20	—	
I_{SD}	Shutdown Current	V_{EN} = 0, V_{BAT} = 2.8V to 8.5V	—	0.7	5.0	μA
UVLO	VBAT UVLO Threshold	V_{BAT} Rising	—	2.7	2.8	V
		V_{BAT} Falling	2.30	2.45	2.55	
		Hysteresis	—	0.250	—	
OVLO	VBAT OVLO Threshold	V_{BAT} Rising	8.6	8.95	9.2	V
		V_{BAT} Falling	8.5	8.6	—	
		Hysteresis	—	0.350	—	
T_{SD}	Thermal Shutdown Threshold	—	—	+150	—	°C
T_{SD_HYS}	Thermal Shutdown Hysteresis	—	—	+40	—	
T_{FOLD}	Thermal Foldback Trip Point	—	—	+125	—	

Boost Converter (V_{BAT} = 7.4V, T_A = +25°C, R_L = 4Ω + 2 × 33μH, V_{PLIM} = V_{GAIN} = V_{DD}, unless otherwise specified.)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{PVDD}	Boost Output Voltage	—		—	9.2	—	V
f_{SW}	Boost Switching Frequency	—		—	768	—	kHz
	Boost Switching Frequency in PFM	No Load		50	75	—	kHz
R_{ON}	On-State Resistance (Boost)	Rectifier Switch	I_L = 20mA	—	50	—	mΩ
		Low-Side Switch		—	50	—	mΩ
I_{LIM}	Boost Converter Current Limit	—		—	8	—	A

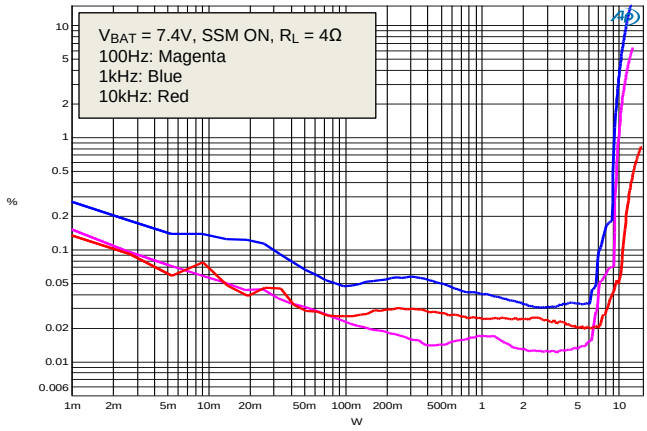
Class-D Amplifier (V_{BAT} = 7.4V, T_A = +25°C, R_L = 4Ω + 2 × 33μH, V_{PLIM} = V_{GAIN} = V_{DD}, unless otherwise specified.)

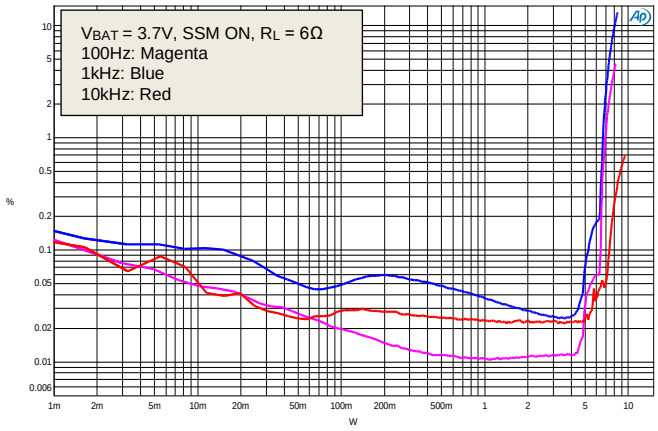
Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
P_O	Continuous Output Power, 2SxP (per Channel) (Note 6)	V_{BAT} = 7.4V, R_L = 4Ω, f = 1kHz, THD+N = 10%		—	12.0	—	W
		V_{BAT} = 7.4V, R_L = 4Ω, f = 1kHz, THD+N = 1%		—	9.6	—	W
	Continuous Output Power, 1SxP (per Channel) (Note 7)	V_{BAT} = 3.7V, R_L = 6Ω, f = 1kHz, THD+N = 10%		—	8.0	—	W
		V_{BAT} = 3.7V, R_L = 6Ω, f = 1kHz, THD+N = 1%		—	6.4	—	W
THD+N	Total Harmonic Distortion + Noise	V_{BAT} = 7.4V, R_L = 4Ω, P_O = 5W, C_{PVDD} = 220μF		—	0.035	—	%
		V_{BAT} = 3.7V, R_L = 6Ω, P_O = 3W, C_{PVDD} = 220μF		—	0.023	—	
V_N	Integrated Output Noise	Gain = 20dB VIN @ AC Ground, 20Hz to 22kHz SSM Off	A-Weighting	—	50	—	μVrms
			No A-Weighting	—	70	—	
		Gain = 26dB VIN @ AC Ground, 20Hz to 22kHz SSM Off	A-Weighting	—	70	—	
			No A-Weighting	—	100	—	
PSRR	Power Supply Rejection Ratio	VIN = AC Ground ±100mV Supply Ripple Gain = 26dB	f = 217Hz	—	-79	—	dB
			f = 1kHz	—	-67	—	
SNR	Signal-to-Noise Ratio	THD+N = 1%, Gain = 26dB, A-Weighted, SSM Off	f = 1kHz	—	100	—	dB
G_V	Gain	GAIN = VDD	—	—	26	—	dB
		GAIN = GND	—	—	6	—	
V_{OS}	Output Offset Voltage	VIN @ AC Ground, Gain = 26dB	—	—	1	10	mV
f_{OSC}	Audio Oscillator Frequency	—	—	—	384	—	kHz
R_{IN}	Input Resistance	GAIN = VDD (26dB)	—	—	15	—	kΩ
		GAIN = GND (6dB)	—	—	105	—	
t_{ON}	Startup Time from EN Asserted	—	—	—	15	—	ms
R_{ON}	On-State Resistance (Class-D)	High-Side H-Bridge Switch	I_L = 100mA	—	100	—	mΩ
		Low-Side H-Bridge Switch		—	100	—	
R_{FLT}	FLT Open-Drain Resistance	Under Any Fault Condition		—	2.1	—	kΩ

Notes: 6. For 2SxP battery configuration, minimum speaker resistance supported is 4Ω per channel.
7. For 1SxP battery configuration, minimum speaker resistance supported is 6Ω per channel.

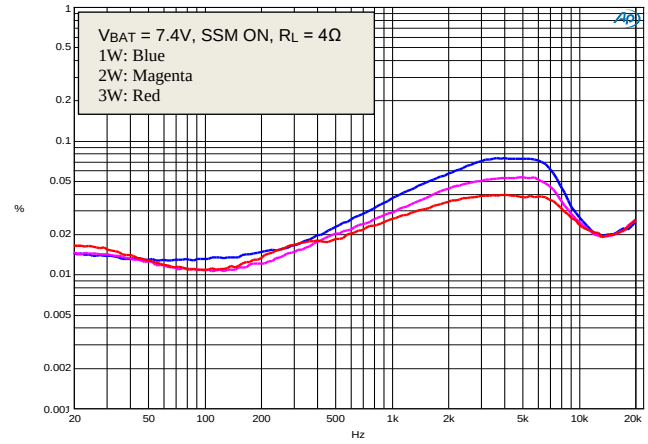
Performance Characteristics (V_{BAT} = 7.4V, T_A = +25°C, R_L = 4Ω + 33μH, V_{GAIN} = V_{DD}, SSM On, unless otherwise specified.)

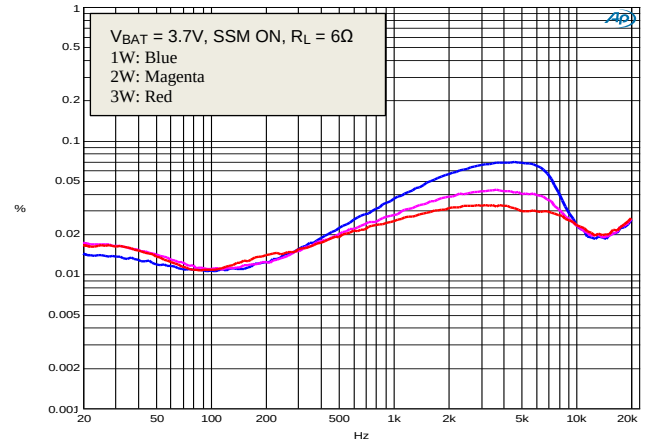
1. THD+N vs Power



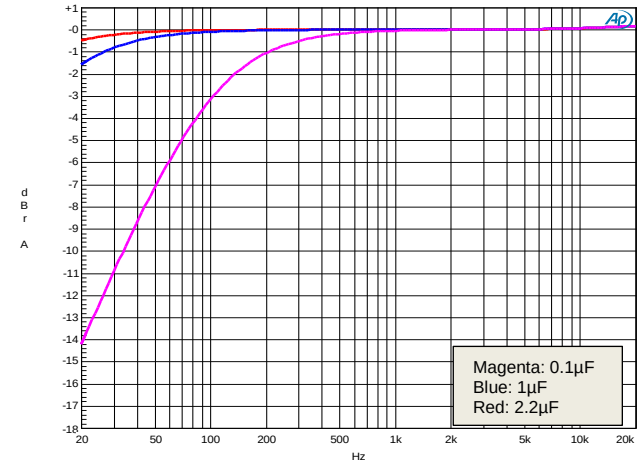


2. THD+N vs Frequency

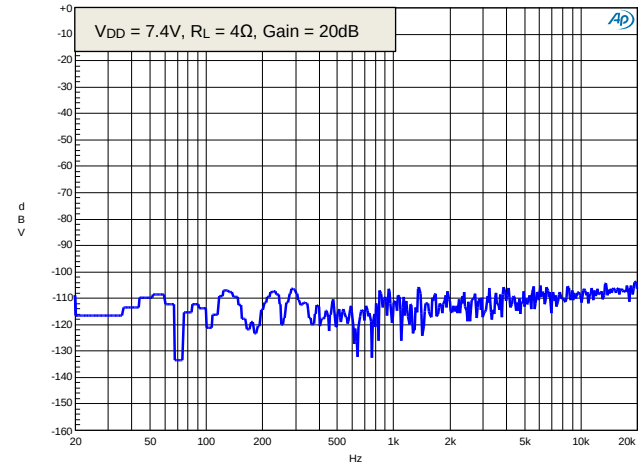




3. Frequency Response

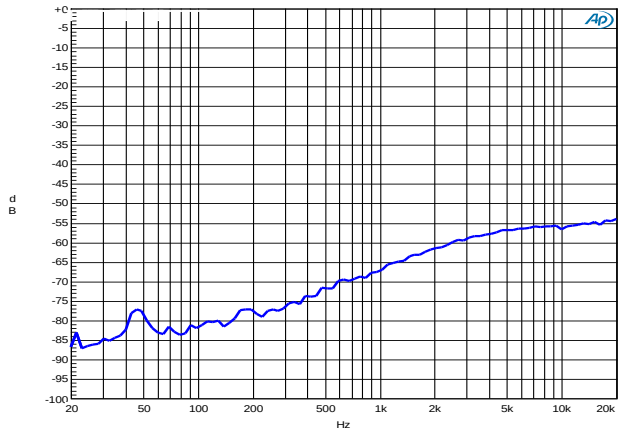


4. Noise Floor

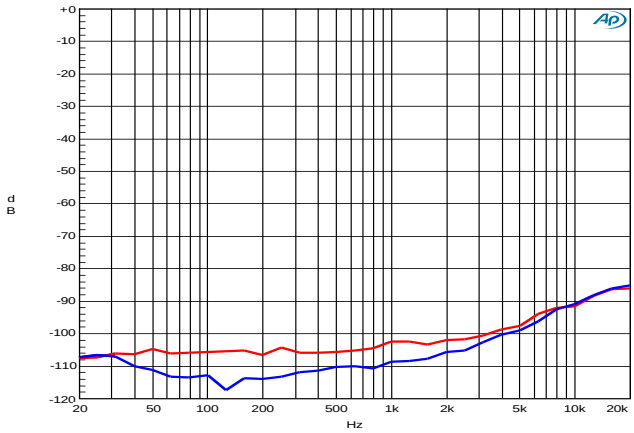


Performance Characteristics (V_{BAT} = 7.4V, T_A = +25°C, R_L = 4Ω + 33μH, V_{GAIN} = V_{DD}, unless otherwise specified.) (continued)

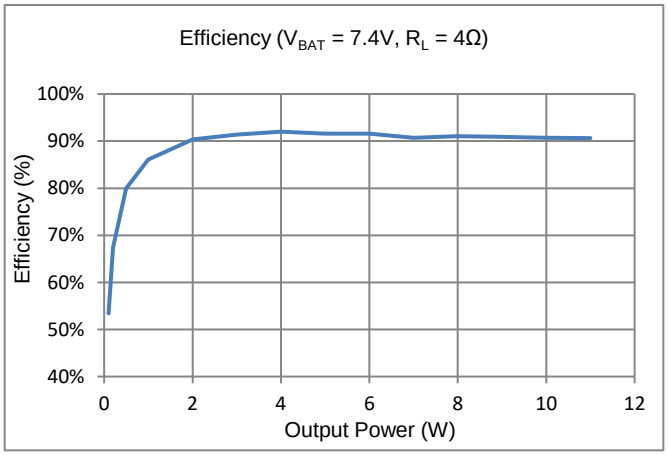
5. **PSRR**



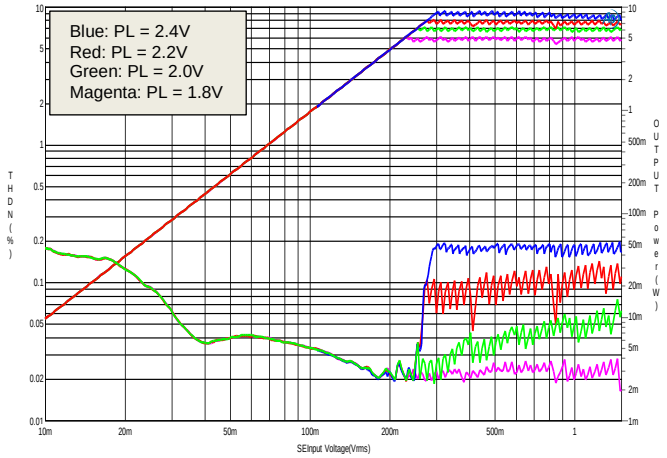
6. **Crosstalk**



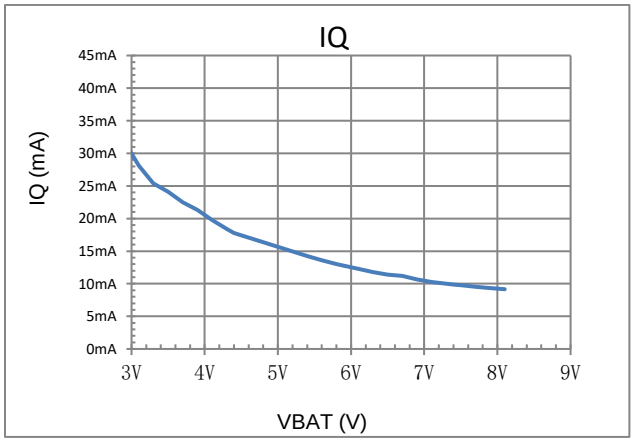
7. **Efficiency vs. Output Power**

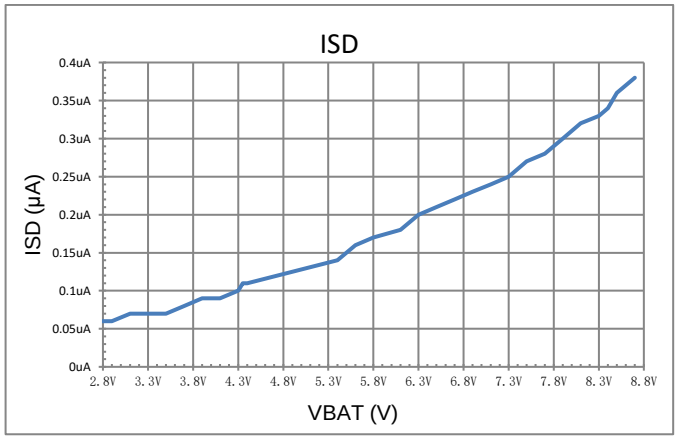


8. **Power Limit**



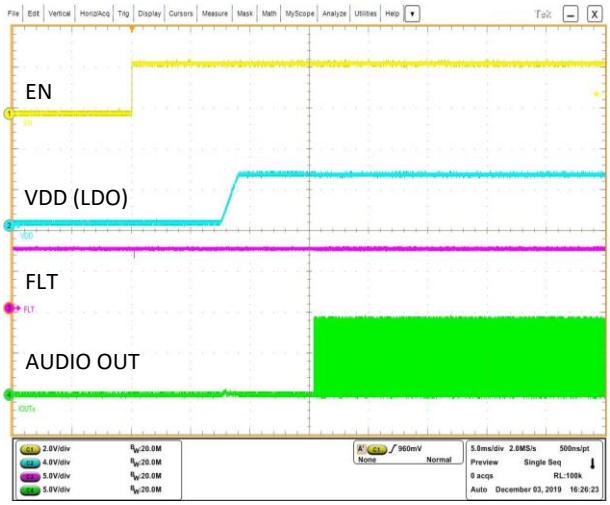
9. **Quiescent Current**



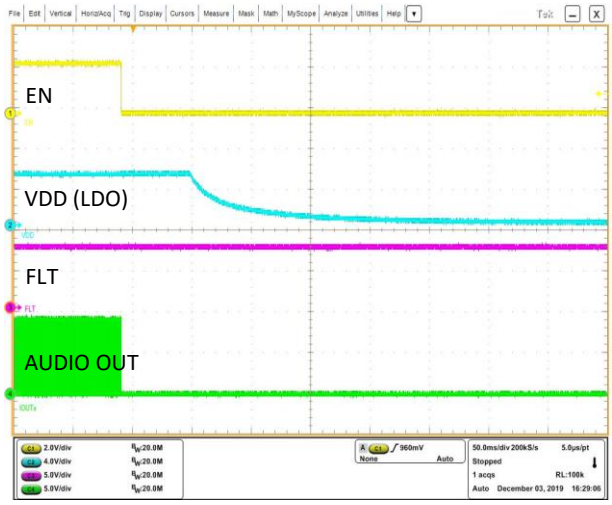


Performance Characteristics (V_{BAT} = 7.4V, T_A = +25°C, R_L = 4Ω + 33μH, GAIN = VDD, unless otherwise specified.)

10. Start-up Waveform with EN Control



11. Shutdown Waveform with EN Control



Detailed Description

The PAM8965 is a stereo Class-D audio amplifier with integrated synchronous boost converter. The device boasts system efficiency of 92% (V_{BAT} = 7.4V), which implies that the boost converter and stereo Class-D amplifier can reach average efficiency of 96% each, negating any advantage of using separate ICs. The high efficiency also allows PAM8965 to deliver 2 × 12W (10% THD+N with V_{BAT} = 7.4V) in to 2 × 4Ω speakers without the need of a heat sink.

The two Class-D audio channels, the integrated synchronous boost converter, and the high efficiency makes PAM8965 an extremely cost-effective general-purpose audio amplifier. The integration also results in the reduction of external components.

With V_{BAT} (input power supply) range of 2.8V to 8.5V, the PAM8965 is perfectly suited for battery applications. The wide input supply range makes it ideal for 1SxP or 2SxP Li-ion battery configurations. In addition, the PAM8965 consumes just 10mA quiescent current (V_{BAT} = 7.4V), and the shutdown current is only 0.7μA (typ), which helps to extend the battery life.

The synchronous boost converter provides a regulated output of 9.2V and operates in pulse width modulation (PWM) mode for medium to high load. For light load condition, the converter transitions to pulse frequency modulation (PFM) mode to improve the efficiency of the converter. In PFM mode, to avoid the switching frequency from dropping in to the audio band, the boost converter features an out-of-audio mode, which keeps the switching frequency above 75kHz (typ). This minimizes the possibility of audible vibrations coming from the components mounted on the PCB.

In terms of performance, the integrated output noise of the audio channel at maximum gain setting of 26dB is only 70μVrms (A-weighted). Similarly, THD+N is only 0.035% at P_O = 5W. The chopper-enabled integrator in the audio channel ensures that the output offset is typically < 1mV at maximum gain.

The headlining feature of PAM8965 is the provision of external audio feedback pins. While internal feedback connection takes care of nonlinearities only in the internal feedback loop, with external feedback pins, the feedback can be Kelvin-connected to the speaker terminals. This eliminates parasitic resistance and inductance from bond wires, PCB trace, ferrite beads and long speaker leads from adversely affecting the fidelity of the audio signal. Furthermore, the external feedback pins allow the use of filter networks in the feedback path to customize sound without relying on DSP.

In terms of features, the PAM8965 incorporates a 41-step (0.5dB per step) automatic gain control (AGC) system, which delivers smooth variations in audio channel gain when responding to the following conditions:

- Junction temperature exceeds +125°C (thermal foldback)
- Output power exceeds a set threshold based on PLIM pin voltage (non-clip power limit)
- Volume control based on the GAIN pin voltage

The PAM8965 output can be driven in single-ended or in bridge-tied-load (BTL) configuration.

Spread spectrum modulation (SSM) allows the use of inexpensive ferrite bead filters and yet meet EMI specification. Although boost switching frequency (768kHz) is twice that of Class-D PWM frequency (384kHz), nevertheless, the spread added on both systems due to SSM is synchronized. This ensures audible beats are not generated due to difference in switching frequencies.

The start-up time, defined as the time between EN asserted and audible output from the speakers, is only 15ms. This includes the boost converter start-up and audio channel wake-up along with the pre-charge of the DC-blocking capacitors at audio Inputs. The advantage of this fast start is that the device does not require mute control. The device can be enabled when audio output is required, and disabled when audio output is off, consuming only 0.7μA in the off state.

The PAM8965 has a multitude of protection features, which include under-voltage and over-voltage lock out on VBAT, over-voltage lock out on PVDD, short circuit protection on all audio outputs, cycle-by-cycle current limit on the boost converter, thermal shutdown of the entire system, speaker protection against DC audio, and an FLT pin that provides a fault flag.

Application Information

Audio Input

The PAM8965 supports differential and single-ended input configurations.

Differential Input

Differential input operation minimizes noise that appears common on both the input lines of the channel. To apply a differential input, connect the positive terminal of the audio source to xINP pin and connect the negative terminal to xINN pin, where x can be L or R for Left and Right channels, respectively.

It is best to AC-couple the audio source to xINP and xINN pins.

Single-Ended Input

To apply a single-ended input, connect the audio source to xINN pin. AC-ground xINP pin by connecting a capacitor equal in value to the DC-blocking capacitor on xINN pin. xINP input should be AC-grounded at the audio source, rather than at the device input, for achieving the best noise performance.

AC- or DC-Coupled Audio Signal

The preferred method to provide audio input is to AC-couple the audio source to xINP and xINN pins with capacitors.

It is also possible to DC-couple the audio source, provided the common-mode voltage of the audio source is close to 2.5V. If output impedance of audio source is high, or the common-mode voltage is far away from 2.5V, then risk of pop noise at turn-on is higher for a DC-coupled audio signal.

In addition, the further the common-mode voltage of the audio source is away from 2.5V, the more the audio source will have to source/sink DC current.

Input Capacitor Selection

For best THD performance, film capacitors are recommended at the Audio Inputs because they offer excellent stability over a wide temperature and voltage range. Use ceramic capacitors for cost-sensitive applications.

Input resistance of the PAM8965 can vary from 15kΩ at 26dB to 105kΩ at 6dB Gain setting. As a result, for AC-coupled applications, the cut-off frequency of high-pass filter that is formed at the input, varies with the Gain setting. The -3dB cut-off frequency is given by (1). Using the minimum value of R_{IN}, which is 15kΩ, provides a minimum recommended value of C_{IN} = 1μF to pass 20Hz to the amplifier.

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}} \quad (1)$$

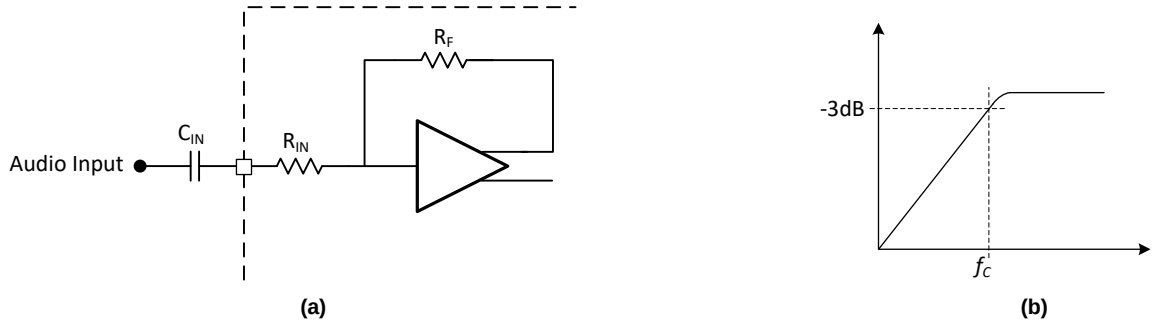


Figure 2. (a) Audio Input Interface, (b) -3dB Cut-Off Frequency of Audio Input High-Pass Filter

Application Information (continued)

Audio Channel Gain

The PAM8965 audio channel gain is defined using the GAIN pin. The channel gain can be set between 26dB and 6dB at 0.5dB steps. Channel gain is accurate when it is based on internal resistors only. If using external resistor on the inputs to set the gain, then the device-to-device gain variation will be large. More importantly, even right and left channel gain will not match because the use of external resistors makes the channel gain dependent on the absolute values of these resistors.

Connect a resistor divider between VDD and GND pins to define a voltage on the GAIN pin (Figure 3). This is important because GAIN is referenced to these supplies. Table 1 provides the resistor ratio required on the GAIN pin to obtain the required channel gain. Figure 4 show the relationship between the GAIN pin voltage and audio channel gain assuming V_{DD} = 5.0V. Aim for $R_1 + R_2 \geq 100k\Omega$ to reduce current wasted in the divider. Place R_1 and R_2 close to the GAIN pin. A small 1nF capacitor can be placed near the pin to filter noise.

$$\text{GAIN Resistor Ratio} = \frac{R_2}{R_1 + R_2} \quad (2)$$

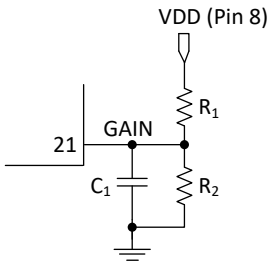


Figure 3. GAIN Resistor Divider Setup

Ratio	Gain (dB)	Ratio	Gain (dB)	Ratio	Gain (dB)	Ratio	Gain (dB)	Ratio	Gain (dB)	Ratio	Gain (dB)
GND to 0.10	6.0	0.24	9.5	0.38	13.0	0.52	16.5	0.66	20.0	0.80	23.5
0.12	6.5	0.26	10.0	0.40	13.5	0.54	17.0	0.68	20.5	0.82	24.0
0.14	7.0	0.28	10.5	0.42	14.0	0.56	17.5	0.70	21.0	0.84	24.5
0.16	7.5	0.30	11.0	0.44	14.5	0.58	18.0	0.72	21.5	0.86	25.0
0.18	8.0	0.32	11.5	0.46	15.0	0.60	18.5	0.74	22.0	0.88	25.5
0.20	8.5	0.34	12.0	0.48	15.5	0.62	19.0	0.76	22.5	0.90	26.0
0.22	9.0	0.36	12.5	0.50	16.0	0.64	19.5	0.78	23.0	0.90 to 1.0	26.0

Table 1. GAIN Resistor Ratio vs. Audio Channel Gain (dB)

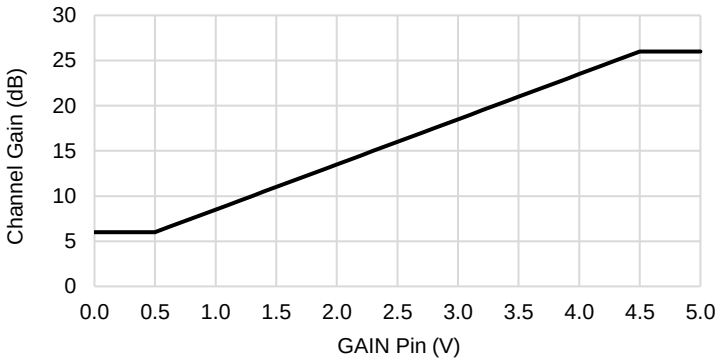


Figure 4. Channel Gain vs. GAIN Pin Voltage (with V_{DD} = 5.0V)

Application Information (continued)

Enable-Disable Control

EN pin on the PAM8965 is active-high. Voltage above V_{IH} (1.5V) enables the device. EN pin is not limited to 5V operation and can be connected directly to VBAT, which has a maximum specification of 8.5V.

When EN pin is pulled below V_{IL} (0.5V), this disables the device and the audio outputs are muted and the boost converter is turned off. In the disabled or shutdown state, the device consumes only 0.7μA (typ). To achieve the best pop-noise performance, it is recommended to first disable the device before removing the power supply. Figure 5 shows one possible power-up and power-down sequence that would minimise output pop-noise.

After device turn-off, minimum wait of 400ms is required before asserting EN again.

EN pin has to be driven and cannot be left floating.

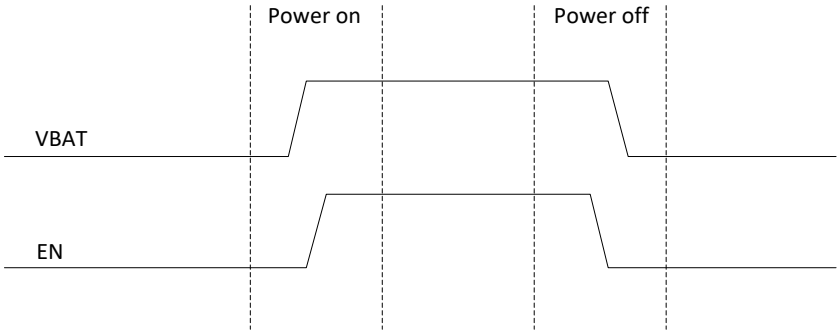


Figure 5. Optional Power-up & Power-down Sequence

Non-Clip Power Limit (PLIM)

The PAM8965 features a non-clipping power limit that protects the speakers from burn out. PLIM pin should be set such that the maximum power rating of the speaker is matched with the maximum output power of the PAM8965.

$$\text{PLIM Resistor Ratio} = \frac{R_2}{R_1 + R_2} \quad (3)$$

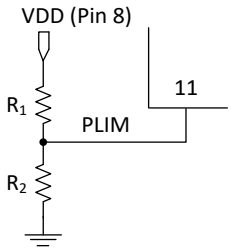


Figure 6. PLIM Resistor Divider Setup

Connect a resistor divider between VDD and GND pins to define a voltage on PLIM pin as shown in Figure 6. This is important because the PLIM function is referenced to these supplies. Aim for $R_1 + R_2 \leq 20k\Omega$. Place R_1 and R_2 close to the PLIM pin. Table 2 shows resistor ratio required on the PLIM pin to set the required output power.

Maximum PLIM voltage is 2.4V when using Power Limit function. PLIM = 2.4V will result in POUT = 9W for VBAT = 7.4V and RL = 4Ω. To disable the power limit function, connect PLIM to VDD (Pin 8).

Application Information (continued)

—				R_L = 4Ω, V_{BAT} = 7.4V	R_L = 6Ω, V_{BAT} = 3.7V
R1 (Ω)	R2 (Ω)	Ratio	V_{PLIM} (V)	P_{OUT} (W)	P_{OUT} (W)
10K	3.0K	0.23	1.15	1.00	1.20
10K	3.9K	0.28	1.40	2.00	1.87
10K	4.7K	0.32	1.60	3.00	2.40
10K	5.4K	0.35	1.75	4.00	3.00
10K	6.2K	0.38	1.91	5.00	3.67
10K	6.8K	0.40	2.02	6.00	4.13
10K	7.5K	0.43	2.14	7.00	4.73
10K	8.2K	0.45	2.25	8.00	5.30
10K	9.1K	0.48	2.40	9.00	6.00
—	—	—	V_{DD}	11.50	8.00

Table 2. PLIM Pin Voltage (for V_{DD} = 5.0V) or Resistor Ratio for Output Power (per Channel)

If instantaneous output power exceeds the defined PLIM value, then the amplifier triggers an attack cycle. Effectively, this begins a process of the PAM8965's amplifier gain stepping down with 0.5dB steps for every attack cycle. The gain is reduced with successive attack cycles until the output power drops to the value defined by the PLIM pin voltage as shown in Figure 7.

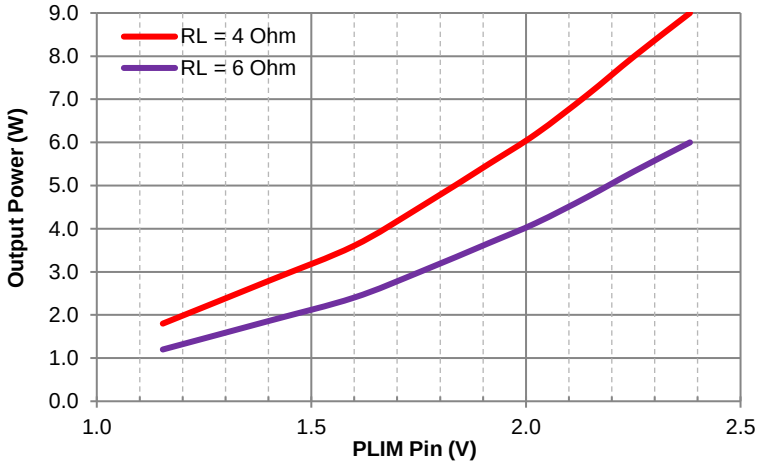


Figure 7. Output Power (per Channel) vs. PLIM Pin Voltage (for V_{DD} = 5.0V)

Adjusting the amplifier's closed-loop gain to control the output power results in an extremely smooth control, which prevents harsh sounds due to saturation. This type of control avoids the output signal from being clipped, thus providing a much nicer listening experience. Figure 8 illustrates the non-clip power limit attack cycle.

Attack time for power limit is 50μs, and release time is 340ms.

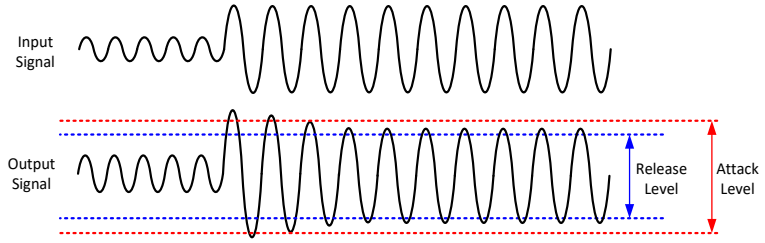


Figure 8. Non-Clip Power Limit Attack Cycle

Application Information (continued)

Thermal Foldback

Device protection due to OTP results in abrupt turn-off and turn-on of sound. The primary purpose of thermal foldback (ThmFB) is to avoid interruption of sound due to OTP. The PAM8965's ThmFB feature works by stepping down the closed-loop gain of the amplifier once the die temperature reaches the ThmFB threshold. As the gain is stepped down, output power is reduced, which results in lower power dissipation thereby reducing the possibility of the device shutting down due to OTP.

Thermal Foldback threshold is set at +125°C. As with PLIM, this feature controls the closed-loop gain of the amplifier resulting in smooth transitions in the audio output. The full AGC range of 26dB to 6dB is available for ThmFB feature. Figure 9 shows an illustration of ThmFB attack and release cycles. The attack time is set at 170ms and the release time is 340ms.

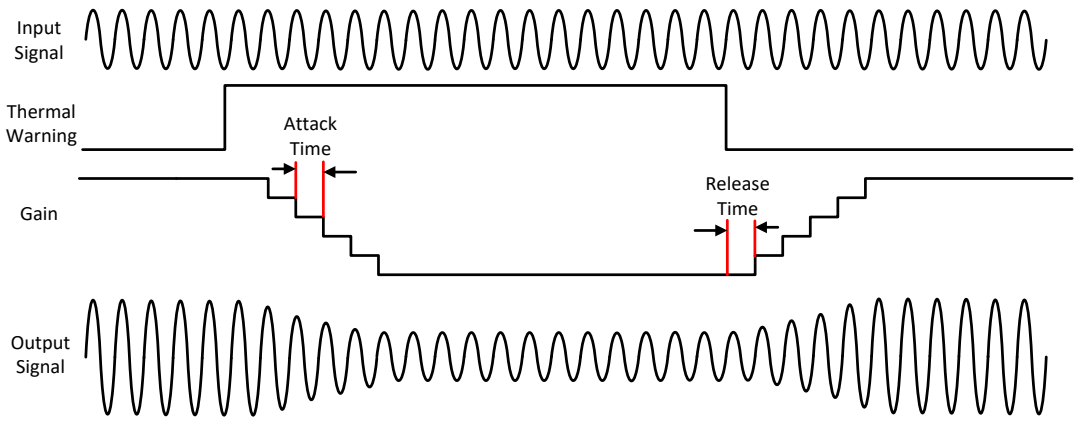


Figure 9. Thermal Foldback Attack/Release Cycle

Fault Flag (FLT)

The PAM8965 features a fault flag, which is an open-drain output on the FLT pin. This pin supports full voltage range up to V_{BAT}.

The following abnormal conditions are flagged on the FLT pin:

- UVLO on VBAT
- OVLO on VBAT
- Over-temperature shutdown (OTP)
- DC detected on any of the audio inputs (no auto-recovery on this fault)
- Short circuit protect (SCP) on any audio output

The open-drain FET turns on when fault occurs, and turns off once the fault is cleared. It is recommended to connect a 100kΩ pull-up resistor from FLT pin to any voltage up to V_{BAT}. If the aim is to minimize PCB component count, then FLT pin can be left floating.

Under Voltage Lock Out (UVLO) on VBAT

When V_{BAT} drops below the UVLO threshold of 2.45V (typ), the device enters a quasi-disabled state where the boost converter and the audio channels are turned off but a few blocks remain powered up. As a result, the current drawn from the battery in this state is higher than I_{SD}. The device will auto-recover and repeat the start-up sequence once V_{BAT} goes above 2.8V.

Over Voltage Lock Out (OVLO) on VBAT

When V_{BAT} goes above the OVLO threshold of 8.9V (typ), the device enters a quasi-disabled state similar to UVLO condition. The device will auto-recover and repeat the start-up sequence once V_{BAT} drops 350mV below the OVLO threshold.

Application Information (continued)

Over-Temperature Protection

To prevent device from over-temperature stress, the PAM8965 incorporates thermal shutdown, which turns the device off when junction temperature exceeds +150°C (typ). OTP has a hysteresis of +40°C. The system will resume operation after junction temperature goes below +110°C (typ). In OTP state, both the audio channels and the boost converter are turned off. This is not a latched fault.

For 1SxP applications, the high boost ratio results in very high boost switch currents. This reduces the efficiency of the system thereby increasing the junction temperature of the device. Depending on the physical enclosure the device is placed in, it may be necessary to use a heatsink if outputting maximum power with maximum boost ratio.

DC Audio Detection

The PAM8965 analyses the PWM output waveform to detect if a DC signal is being applied to the speakers. This can occur due to damaged capacitors at the audio inputs or due to shorts on the PCB. A DC signal can quickly over-heat and damage the speakers. By detecting DC in the output waveform rather than at the input, DC protection will kick-in at the same output level irrespective of the GAIN setting.

Once DC is detected on any of the outputs (P or N of right or left channel), both audio channels are turned off with all four audio outputs changing state to Hi-Z. The audio channels will remain off because this fault condition is latched. This ensures the speaker is protected against repeated exposure to DC voltage/current, which can cause damage.

Cycling EN or VBAT will clear the fault.

Short-Circuit Protection with Auto-Recovery for Audio Outputs

If the PAM8965 detects a short on any of the audio outputs, then it will change the state of all the audio outputs to Hi-Z. This protection not only saves the PAM8965 from damage but also prevents excessive currents from flowing from the supply, or to ground, which can cause damage to other components in the system. The PAM8965 protects against the following short conditions:

- Any audio output shorted to boosted supply (PVDD) or VBAT
- Any audio output shorted to Ground
- LOUTP shorted to LOUTN
- ROUTP shorted to ROUTN

Once any of the above-mentioned short is detected, then all the audio outputs are immediately disabled. The auto-recovery time is 340ms (typ). After this time has elapsed, the device will restart the outputs. If the short persists, the device will continue to trigger short protection after each auto-recovery.

Spread Spectrum Modulation

The PAM8965 features spread spectrum modulation, which randomizes the oscillator frequency to improve EMI performance.

SSM on the PAM8965 is center-spread with ±11% modulation.

With SSM enabled, EMI specification can be met with inexpensive ferrite bead filters rather than bulky low-pass LC filters at the audio output. Given that the boost switching frequency (768kHz) is twice that of Class-D PWM frequency (384kHz), to avoid audible beats between the two systems, the SSM spread added to both systems is synchronized.

Connect SSM pin to a voltage above V_{IH} (1.5V) to enable SSM, or below V_{IL} (0.5V) to disable it. This pin is compliant to VDD.

Application Information (continued)

EMI Requirement

The PAM8965 features spread-spectrum modulation, which can be turned on to reduce emissions. With SSM enabled, the PAM8965 can provide high-efficiency Class-D amplification while minimizing interference to the surrounding circuits.

Two possibilities exist to meet FCC Class B regulations:

1. Ferrite Bead Filter
   The PAM8965 EVM passes FCC Class B standard with a ferrite bead filter using 60cm long twisted-pair wires for 4Ω speakers and operating at 2x8W.

   Only a low-cost ferrite bead filter is required for most applications. Select the ferrite bead type and size based on the application. A 600Ω@, 100MHz ferrite bead with a 330pF bypass capacitor and 100Ω+560pF snubber is recommended. A larger capacitor can be used to improve EMI filter, but system efficiency will be impacted. The filter should be placed close to the pins. Figure 10 shows an example of such a filter.

2. Low-Pass LC Filter
   For long wires, it is recommended to use an LC filter to supress EMI. If the amplifier is close to sensitive circuits, then LC filter will provide better EMI filtering than ferrite filter. In addition, LC filter will have a smaller detrimental impact on system efficiency than a ferrite filter. Again, this filter should be placed close to the pins. See Figure 11 for details.

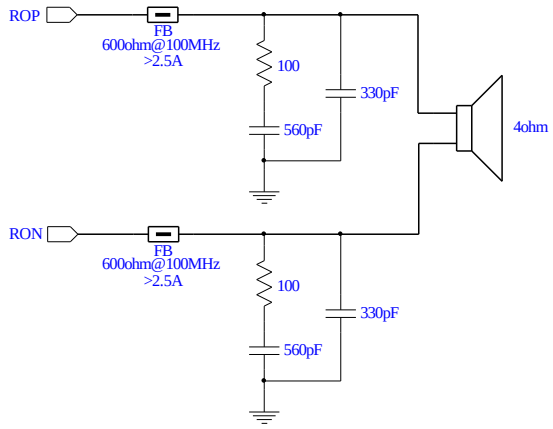


Figure 10. Typical Ferrite Bead Filter

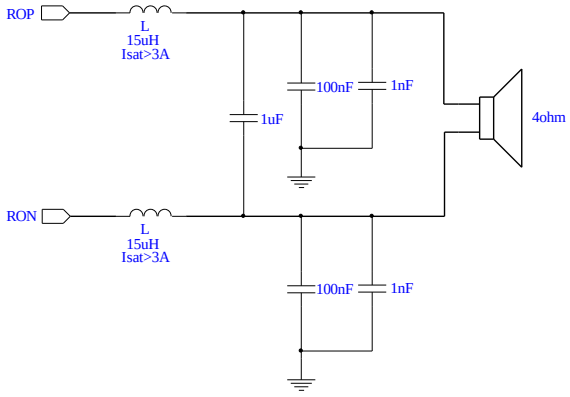


Figure 11. Typical LC Filter for BTL, Cutoff Frequency = 28kHz, Speaker Impedance = 4Ω

3. Snubber Circuit
   A snubber circuit can be added to the booster switching inductor, See option “A” in Figure 14 for details.

Application Information (continued)

EMI Performance

PAM8965 passes CISPR 32 Class B EMI test driving 2x8W into 4Ω left/right speakers with 60cm long twisted-pair wires using Diodes Incorporated's released PAM8965EVM (v1.1, 2 layer board) which has options EMI options "A", "B" and "C" installed (Please refer to Figure 14) on board. PCB layout is critical for good EMI performance, please refer to "PAM8965 EV Board User Guide" for details.

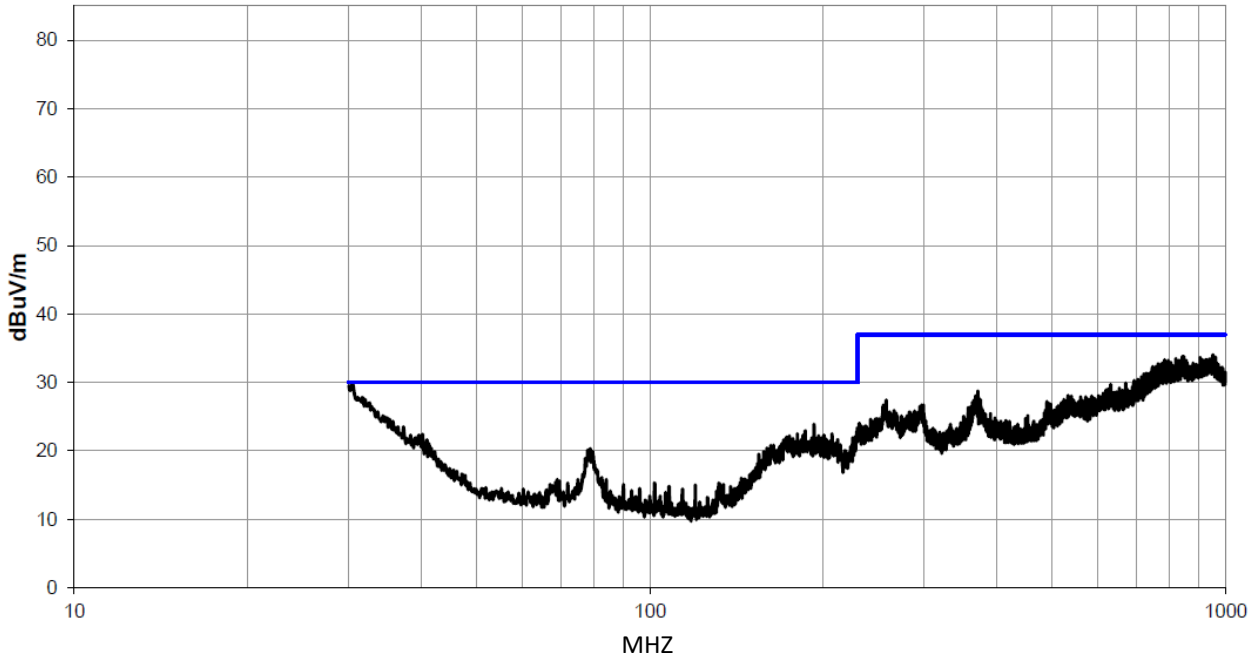


Figure 12. PAM8965 EMI Performance

Synchronous Boost Converter

The PAM8965 creates its own boosted power supply for the audio channels using a fully integrated synchronous boost converter. The converter delivers a fixed output voltage (V_{PVDD}) of 9.2V from V_{BAT} input supply that can range from 2.8V to 8.5V. It incorporates a 50mΩ power switch and a 50mΩ synchronous switch making it capable of delivering 2 × 12W in 4Ω load with 2SxP battery, or 2 × 8W in 6Ω load with 1SxP battery pack.

The current-mode boost converter operates in constant-frequency PWM mode for heavy loads and PFM (pulse frequency modulation) mode when operating in light load condition. This allows the converter to operate at optimum efficiency throughout the load range. The boost control loop is internally compensated.

The converter features an out-of-audio mode, which ensures that the switching frequency on the SW node never falls in the audio band when the device is operating in PFM mode, typically restricting it to > 75kHz.

Cycle-by-cycle current limit monitors the current flowing in low-side FET, and turns it off immediately if the peak switch current reaches the threshold of 8A (typ). The converter also features an over-voltage protection on PVDD, which is set at 10.5V (typ).

1SxP Battery – Special Considerations for $V_{BAT} \leq 5.0V$

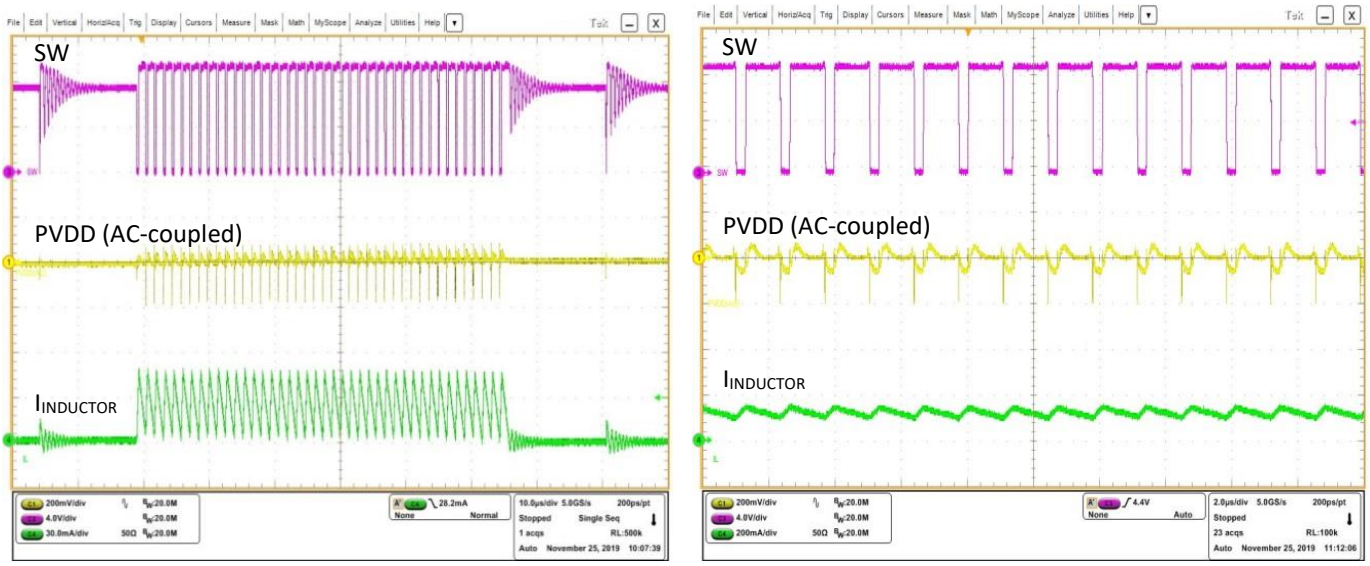
The efficiency of the system is lower when operating with 1SxP battery configuration as compared to 2SxP. The higher switch current due to higher boost ratio results in the device running hotter. The following three options may be implemented for 1SxP operation. Since this issue is related to heat dissipation, it is highly dependent on the PCB layout and metal thickness. Some applications may require all the options below, while some may only need one.

1. Use 4.7μH inductor

2. High-current Schottky diode (e.g., SBR10U45SP5) placed between SW and PVDD (Pin 27 and 28):
   A Schottky diode, in parallel with boost high-side, should be placed very close to the pins. Bottom plane can be used for this connection. Omit this device if it cannot be placed within 10mm of the device pins.

Application Information (continued)

3. Schottky diode (e.g., DFLS220L) and 10Ω resistor from VDD (Pin 8) to BST (Pin 26).
   This improves boost high-side drive at low V_{BAT}, which results in improved system efficiency.



(a) (b)

Figure 13. Boost Converter Waveforms, (a) PFM Mode, I_{LOAD} = 0A, (b) PWM Mode, I_{LOAD} = 1A

Boost Inductor Selection

It is critical to select a correct value of inductor for the boost converter because efficiency, transient behavior and loop stability rely on this selection. Three most important specification of the inductor are its inductor value, DC resistance, and saturation current. In a boost regulator, the average DC current in the inductor is given by equation (4).

$$I_{L\_DC} = \frac{PVDD * I_{OUT}}{V_{BAT} * \eta} \quad (4)$$

where,

$PVDD$	is the output voltage of the boost regulator
I_{OUT}	is the output current of the boost regulator
V_{BAT}	is the supply voltage
η	is the efficiency of the boost regulator

For $PVDD$ = 9.2V, I_{OUT} = 4.3A (assuming 600mV drop across the audio FETs, and 2 × 4Ω load), V_{BAT} = 7.4V, and η = 90%, gives I_{L_DC} = 5.94A.

The Inductor peak-to-peak ripple current is given by the following equation:

$$\Delta I_{L\_PP} = \frac{V_{BAT}(PVDD - V_{BAT})}{L \cdot f_{SW} \cdot PVDD} \quad (5)$$

where,

L	is the inductor
f_{SW}	is the switching frequency of the Boost regulator

For f_{SW} = 768kHz and L = 4.7μH results in ΔI_{L_PP} = 401mA (using the above mentioned values for V_{BAT} and PVDD).

The peak inductor current, I_{L_PK}, can be calculated using (6).

$$I_{L\_PK} = I_{L\_DC} + \frac{\Delta I_{L\_PP}}{2} \quad (6)$$

Application Information (continued)

Plugging the above calculations in to (6), results in peak inductor current, I_{L_PK} = 6.14A.

Note that boost converter's current limit is set at 8A. Even though peak inductor current calculated in this example is 6.14A, nevertheless, it is recommended to use an inductor with saturation current rating that is at least 25% higher than the current limit of 8A. There will be transients where the peak inductor current will reach the converter's current limit, especially at lower V_{BAT} voltages. It is imperative that when this occurs, the inductor is not close to its saturation limit.

4.7μH inductor with saturation current rating of at least 10A is recommended.

Capacitor Selection Guide

Refer to *Input Capacitor Selection* for audio input capacitor calculation and recommendation.

Power Supply Decoupling - VBAT Terminal
Capacitor Value: 1000μF
Voltage Rating: $2 \times V_{BAT}$
Capacitor Type: Aluminium Polymer Electrolytic

Capacitor Value: 22μF
Voltage Rating: $5 \times V_{BAT}$
Capacitor Type: X7R (ceramic)

V_{BAT} is the power supply of the entire chip. It is important to place a bulk capacitor in parallel with a ceramic capacitor at this node, where the battery connects to the PCB. VBAT1 and VBAT2 are supply pins on the IC, and these should be Kelvin connected to the VBAT terminal on the PCB.

Where the bulk capacitor acts as a large storage, the ceramic capacitor provides a low impedance path for high frequency noise due to its low equivalent series resistance (ESR).

Capacitors on the VBAT terminal and on the VBAT1 and VBAT2 pins can be scaled based on the VBAT supply used in the system. As a rule-of-thumb, use $2 \times V_{BAT}$ voltage rating for electrolytics, and $5 \times V_{BAT}$ voltage rating for ceramics.

VBAT1 (Pin 30)
Capacitor Value: 1μF 0.033μF and 330pF in parallel
Voltage Rating: $5 \times V_{BAT}$
Capacitor Type: X7R (ceramic)

VBAT1 is the primary power supply for the PAM8965. A number of internal start-up and regulation circuitry is powered off VBAT1. Place these capacitors close to the pin.

VBAT2 (Pin 29)
Capacitor Value: 10μF
Voltage Rating: $5 \times V_{BAT}$
Capacitor Type: X7R (ceramic)

VBAT2 supplies the boost internal circuitry, including regulators that help drive the power transistors. Thus, a larger capacitor of 10μF is recommended on VBAT2. Place this capacitor close to the pin.

VDD (Pin 8)
Capacitor Value: 22μF in parallel with 0.1μF
Voltage Rating: 25V
Capacitor Type: X7R (ceramic)

The PAM8965's VDD Pin is the output of an internal 5V LDO regulator. Place these capacitors close to the VDD pin. This regulator's output should not be used to drive any external circuitry.

Application Information (continued)

Bootstrap Capacitors (Pin 15, 17, 26, 34, 36)
Capacitor Value: 0.1µF
Voltage Rating: 25V
Capacitor Type: X7R (ceramic)

All the bootstrap pins, including both audio channels (RBSTP, RBSTN, LBSTP, LBSTN) and the boost converter (BST), require a 0.1µF X7R capacitor on each pin. The capacitors must be connected from the bootstrap pins to their corresponding switching output. Place these capacitors close to the pins.

PVDD Boost Output (Pin 27 shorted with Pin 28)
Capacitor Value: 1000µF
Voltage Rating: 25V
Capacitor Type: Aluminium Polymer Electrolytic

Capacitor Value: 10µF 033µF, 2x330pF in parallelel
Voltage Rating: 50V
Capacitor Type: X7R (ceramic)

The PAM8965 is a high-performance audio amplifier that requires adequate audio power supply decoupling to ensure the total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents ringing oscillations caused by long leads between the amplifier and the speaker.

PVDD (Pin 27, 28), which is the boost converter's output, is the primary power supply for both the audio channel's H-bridges (Pin 16 and Pin 35). Boost converter output requires a bulk capacitor, and four ceramic capacitors to provide a clean supply to the audio channels. Place the ceramic capacitors close to the pins.

This regulator output should not be used to drive any external circuitry.

LPVDD & RPVDD (Pin 16 & Pin 35)
Capacitor Value: 1µF and 0.1µF in parallel
Voltage Rating: 50V
Capacitor Type: X7R (ceramic)

LPVDD & RPVDD are supply pins for the audio H-bridge. For adequate noise filtering, each channel's supply shares a bulk aluminium polymer electrolytic capacitor of 1000µF with boost output, along with ceramic capacitors. Place the ceramic capacitor close to the pins.

Additional Application Feasibilities

Other than typical applications with dynamic speaker load, the PAM8965 is also capable of wide varieties of applications to drive other types of loads, including high-capacitive ceramic speaker and Linear Resonant Actuator (LRA). For exploring these applications, please refer to related sales representative or Diodes Incorporated' Field Application team for further application support.

Application Information (continued)

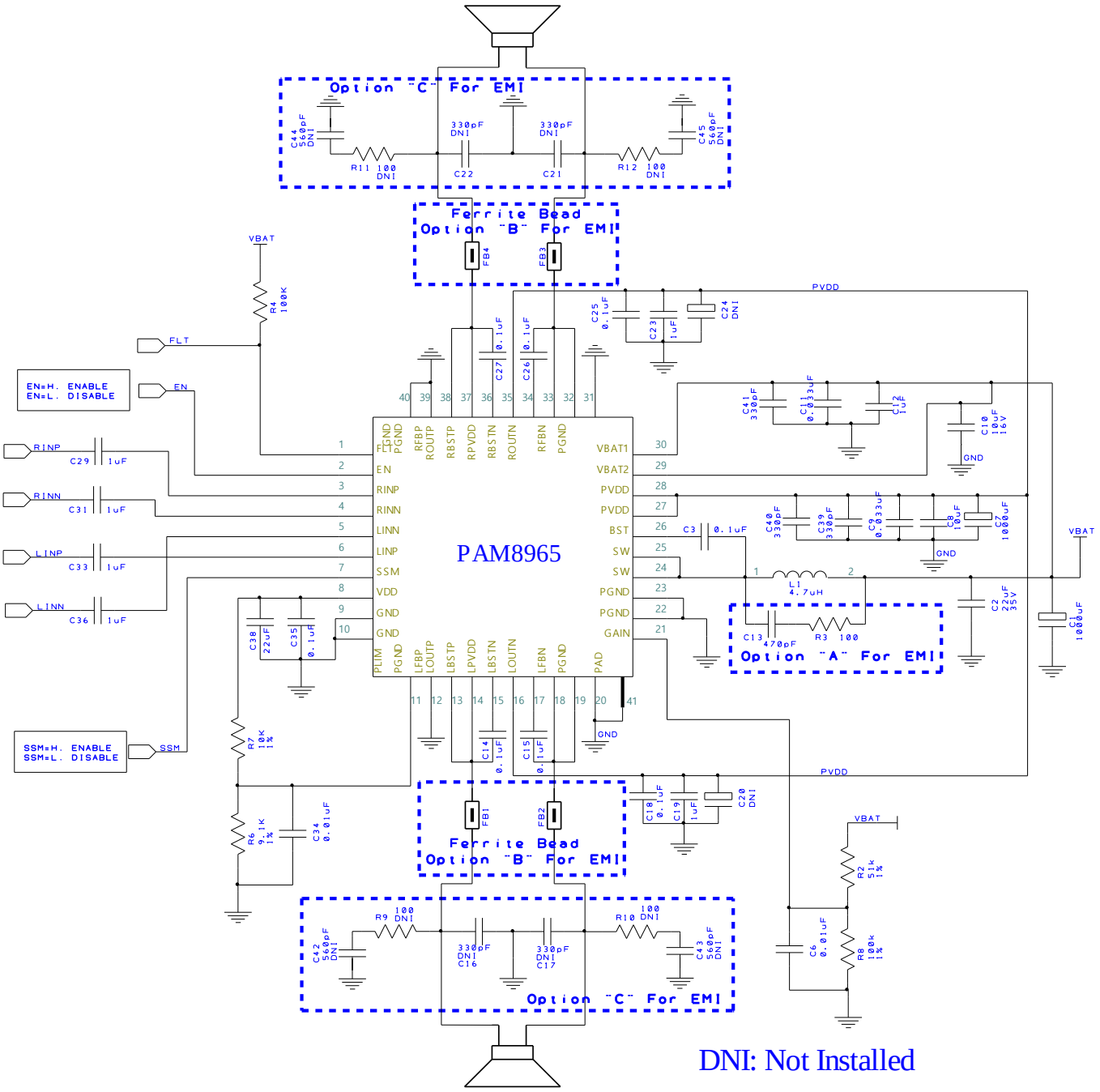
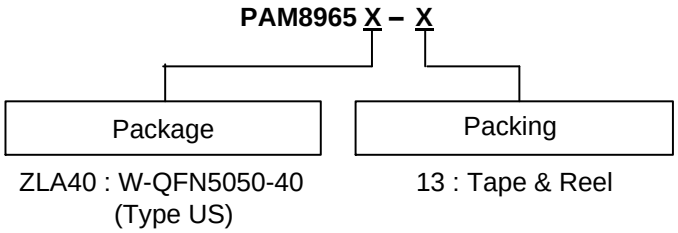


Figure 14. Typical Application Circuit for PAM8965 in BTL Mode

Ordering Information

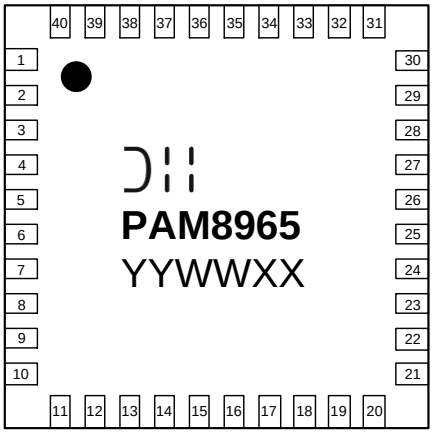


Part Number	Package Code	Package	Packing	
			Qty.	Carrier
PAM8965ZLA40-13	ZLA40	W-QFN5050-40 (Type US)	3000	13” Tape & Reel

Marking Information

(1) W-QFN5050-40 (Type US)

(Top View)



: Logo

PAM8965 : Marking ID

YY : Year : 21, 22, 23~

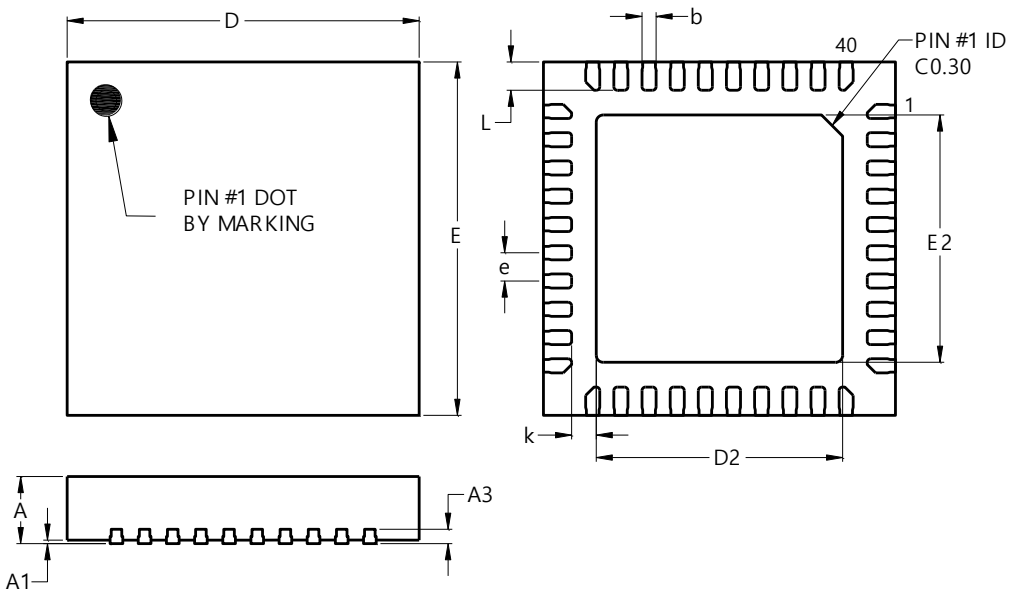
WW : Week : 01 to 52; 52 Represents 52 and 53 Week

XX : Internal Code

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN5050-40 (Type US)

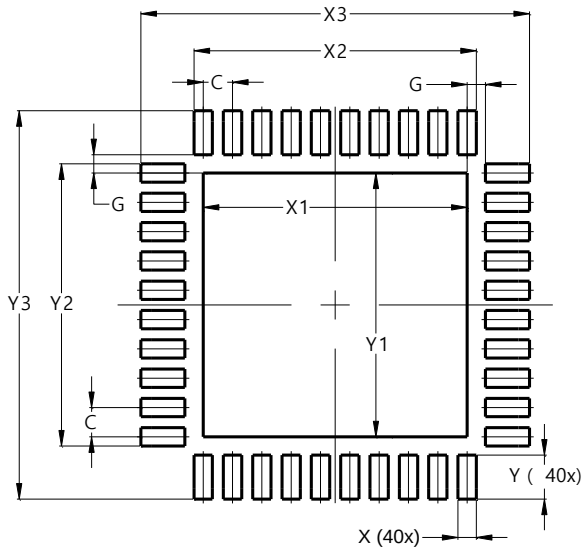


W-QFN5050-40 (Type US)			
Dim	**Min**	**Max**	**Typ**
A	0.700	0.800	0.750
A1	--	0.050	--
A3	0.203 REF		
b	0.150	0.250	0.200
D	4.950	5.050	5.000
D2	3.450	3.550	3.500
E	4.950	5.050	5.000
E2	3.450	3.550	3.500
e	0.400 BSC		
k	0.350 REF		
L	0.350	0.450	0.400
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN5050-40 (Type US)



Dimensions	Value (in mm)
C	0.400
G	0.250
X	0.250
X1	3.600
X2	3.850
X3	5.300
Y	0.600
Y1	3.600
Y2	3.850
Y3	5.300

Mechanical Data

- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per J-STD-002, Test B1 (e3)
- Weight: 0.066 grams (Approximate)

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