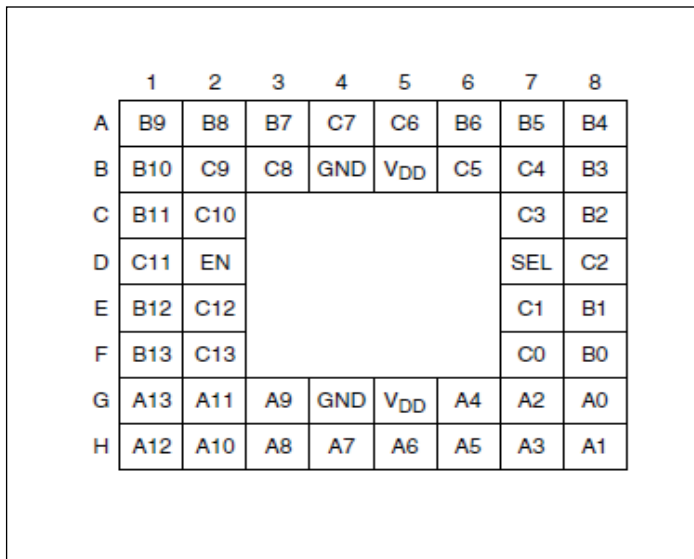


Features

- 14 bit 2:1 switch that supports DDR3 800 2133Mbps, DDR4 1600~4266 Mbps
- VDD 1.35V/ 1.5V/ 1.8V
- Flow through pinout option for easy layout
- SEL and Global Enable
- 110 μ A typ. operating current at 1.35V VDD.
- High impedance and low Coff channel output when disabled or deselected
- Low R_{ON} : 8 Ω typical
- 3dB Bandwidth: 3.3GHz
- Low insertion loss: -0.7dB ($0 \leq f \leq 1$ GHz)
- Low return loss: -23dB ($0 \leq f \leq 1$ GHz)
- Low cross-talk for high speed channels: -25dB typ. ($0 < f < 2$ GHz)
- Low off-isolation: -28dB ($0 \leq f \leq 1$ GHz)
- Low bit-to-bit skew 20ps Max
- ESD: 2KV HBM
- POD_12, SSTL_12, SSTL_135, SSTL_15 or SSTL_18 signaling
- Packaging (Pb-free and Green)
 - 52 pin TQFN (3.5x9mm)
 - 48 pin TFBGA (4.5x4.5mm)pin compatible with CBTW28DD14

Pin Configuration (48 pin TFBGA)



Description

This 14-bit DDR3/DDR4 switch is designed for 1.35V/ 1.5V/ 1.8V supply voltage, POD_12, SSTL_135, SSTL_15 or SSTL_18 signaling and CMOS select input signals. It is designed for DDR3 or DDR4 memory bus with speed up to 5Gbps. It supports DDR3 800 2133Mbps and DDR4 1600~4266 Mbps.

PI2DDR3212 has a 1:2 demux or 2:1 mux topology. All 14-bit channels can be switched to one of the two ports simultaneously with the SEL input. This device also allows all ports to be disconnected.

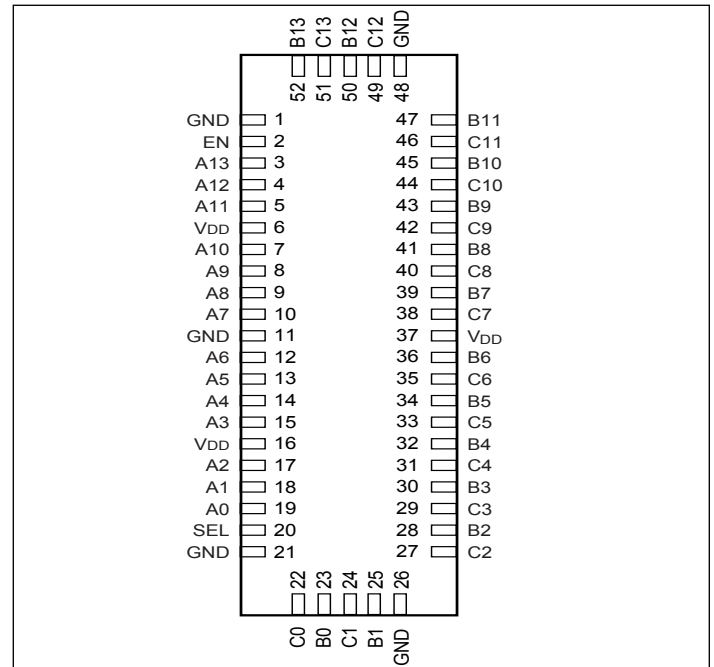
PI2DDR3212 uses Pericom's proprietary high speed switch technology providing consistent high bandwidth across all channels, with very little insertion loss, cross-talk, and bit to bit skew.

It is available in a 52-pin TQFN 3.5x9mm package and 48-pin TFBGA 4.5x4.5mm package. The 48-pin version is pin compatible with CBTW28DD14.

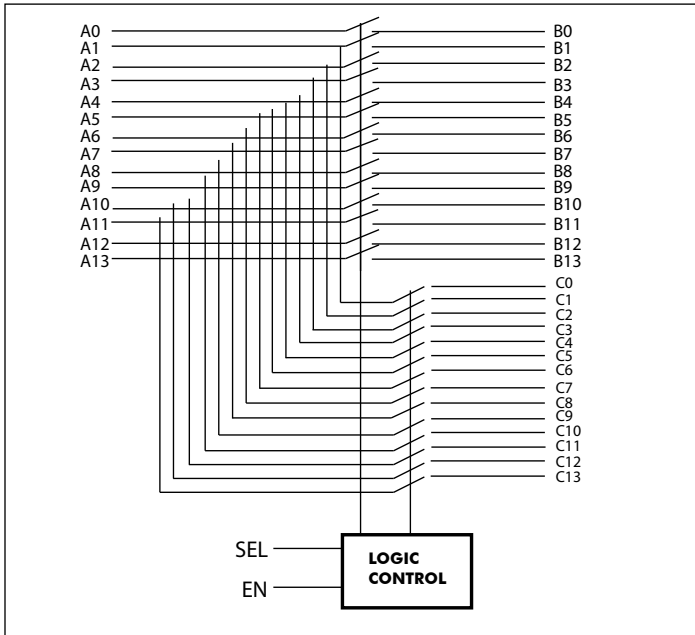
Application

- DDR3/DDR4 Memory Bus System
- NVDIMM Module
- Flash Memory Array sub system
- High Speed multiplexing

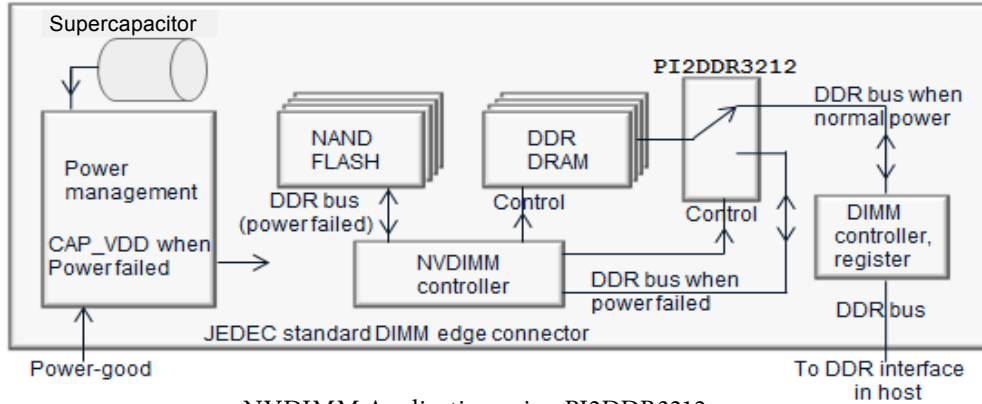
Pin Configuration (52-pin TQFN)



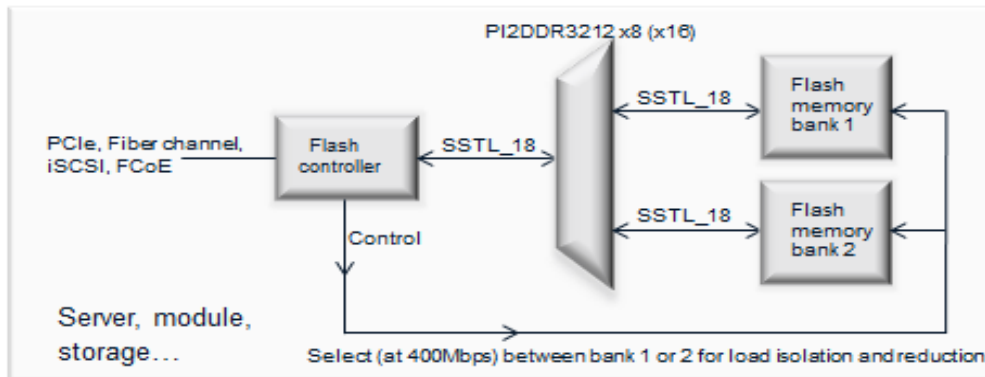
Block Diagram



Application



NVDIMM Application using PI2DDR3212



SSD, Flash storage application using PI2DDR3212

Pin Description

Pin Name	IO Type	Descriptions
V _{DD}	Power	1.35V, 1.5V or 1.8V power supply.
GND	Ground	1.35V, Ground connection
A[0:13]	I/O	14-bit wide input/output, port A
B[0:13]	I/O	14-bit wide input/output, port B
C[0:13]	I/O	14-bit wide input/output, port C
SEL	I	CMOS input for channel selection
EN	I	CMOS input When HIGH, connection is set using the SEL input signal When LOW, all ports are mutually isolated

Truth Table (SEL)

SEL	Function
0	Output B is selected
1	Output C is selected

Truth Table (EN)

EN	Function
1	Global Enable
0	Global Disable

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential	-0.3V to 2.5V
All Inputs.....	-0.3V to $V_{DD}+0.3V$
Ambient Operating Temperature	-10 to +85°C
Storage Temperature.....	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature.....	260°C

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-10		+85	°C
Power Supply Voltage (measured in respect to GND)	+1.28	1.8	+2.0	V

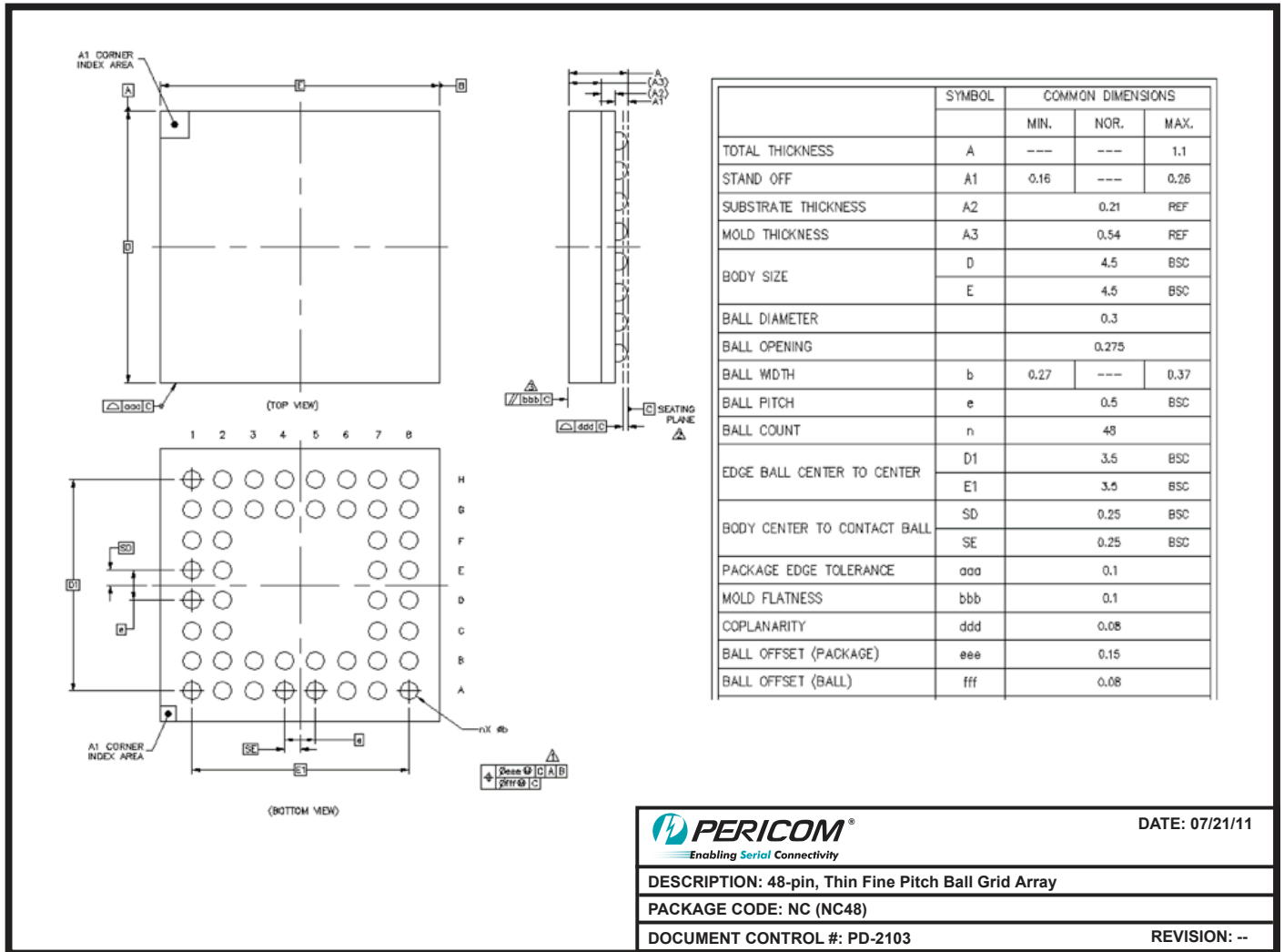
Static Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.28	1.35/ 1.5 / 1.8	2	V
I_{DD}	V_{DD} Supply Current	EN= HIGH; $V_{DD}=1.8V$		220	350	μA
		EN= LOW; $V_{DD}=1.8V$		0.1	10	μA
I_{DD}	V_{DD} Supply Current	EN= HIGH; $V_{DD}=1.35V$		110	200	μA
		EN= LOW; $V_{DD}=1.35V$		0.05	2	μA
Control pin (SEL, EN)						
I_{IH}	High level digital input current	$V_{IH}=V_{DD}$, $V_{DD}=2.0V$			5	μA
I_{IL}	Low level digital input current	$V_{IL} = GND$, $V_{DD}=2.0V$			5	μA
V_{IH}	High level digital input voltage		0.8 * V_{DD}			V
V_{IL}	Low level digital input voltage				0.2* V_{DD}	V
I/O pin (A, B ,C)						
C_{OFF}	Switch OFF capacitance	$f = 1MHz$; $V_{I/O} = 0V$		1.1		pF
C_{ON}	Switch ON capacitance	$f = 1MHz$; $V_{I/O} = 0V$		2.1		pF

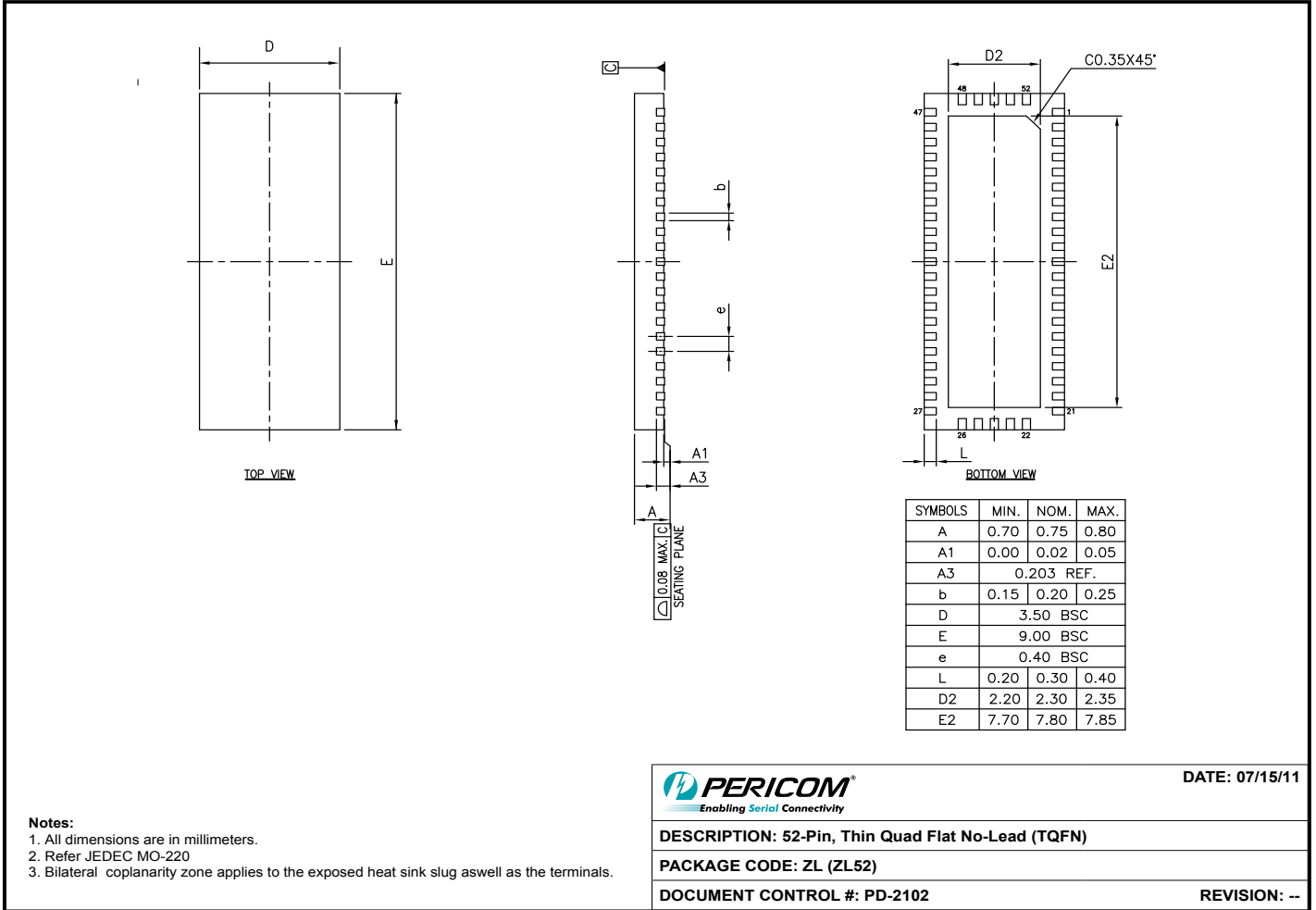
Dynamic Characteristics (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
tstartup	Startup time	Supply voltage valid or EN going HIGH to channels specified characteristics		5	10	μs
trcfg	Reconfiguration time	SEL state change to channel specified operating characteristics		0.02	0.04	
tpd	Propagation delay	From A port to B port or C port or vice versa		60		ps
tsk	Skew time	From any output to any output		18	20	ps
V _I	Input Voltage		-0.3		Vdd+0.3	V
B	Bandwidth	-3dB intercept		3.3		GHz
C	Crosstalk attenuation	Adjacent channels are on; 0 ≤ f ≤ 1GHz		-26		dB
I _L	Insertion Loss	0 ≤ f ≤ 1GHz		-0.7		dB
		f = 2.5GHz		-2.5		dB
R _L	Input Return Loss	0 ≤ f ≤ 1GHz		-23		dB
OI	Off Isolation	0 ≤ f ≤ 1 GHz		-28		dB

Packaging Mechanical: 48-Pin TFBGA



Packaging Mechanical: 52-Pin TQFN (ZL)



Ordering Information

Ordering Code	Packaging Code	Package Description
PI2DDR3212ZLE	ZL	52-Pin, Thin Quad Flat No-Lead (TQFN)
PI2DDR3212NCE	NC	48-Pin, Thin Fine Pitch Ball Grid Array (TFBGA)

NOTES:

1. Thermal characteristics can be found on the company web site at www.pericom.com/package
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel

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