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Diodes Incorporated

**PERICOM**®

**PI3EQX6801A**

## 6.5Gbps, 1-port, 1.5V/3.3V SATA/SAS ReDriver™ with Analog/Digital Configuration

## Features

➜ Two 6.5Gbps differential channels
➜ Output swing up to 1.2V pk-to-pk
➜ SAS, SATA fully supported
➜ Adjustable Receiver Equalization - 0 to 16 dB
➜ 100Ω Differential CML I/O's
➜ Continuous step output swing adjustment
➜ Continuous step output pre-emphasis control
➜ Input signal level detect and squelch for each channel
➜ OOB fully supported
➜ Auto HDD Rate Detection for out swing/emphasis setting
➜ Supply Voltage: 1.5V or 3.3V
➜ Low Power, 162mW @ 1.5V (600 mV Swing)
➜ Stand-by Mode – Power Down State: Current < 56 µA
➜ Auto Slumber Mode power: 22.5mW typical
➜ Industrial Temperature Range -40 to 85°C
➜ Packaging: 20-contact TQFN (4x4mm)

## Applications

➜ Server
➜ Desktop
➜ Data Storage/Workstation

## Block Diagram



- Repeated 2 times -
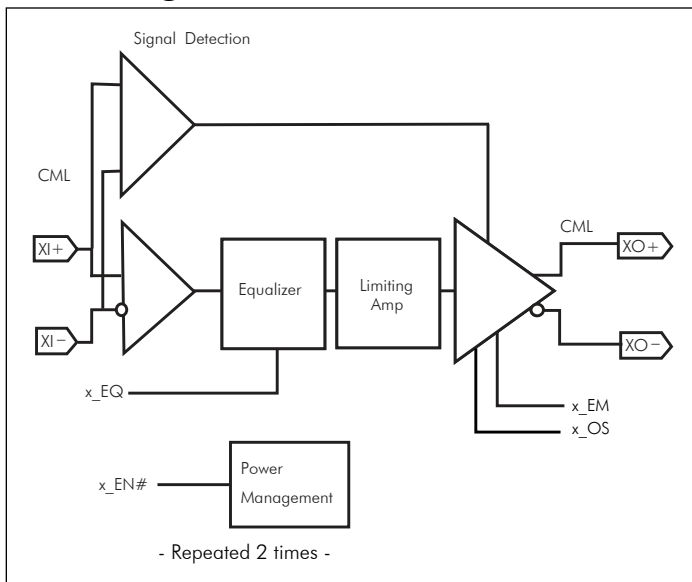
## Description

The PI3EQX6801A is a low power, 1.5V/3.3V, 6.5Gbps, SATA/SAS signal ReDriver™. The device provides programmable equalization, to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference.

PI3EQX6801A supports two 100Ω Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver.

A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independently. When the channels are enabled (x_EN#=0) and operating, that channels input signal level (on xI+/-) determines whether the output is active. If the input signal level of the channel falls below the active threshold level (Vth-) then the outputs are driven to the common mode voltage.

Each lane can be powered-down if x_EN# =1, and when A_EN# and B_EN# are both high, the device enters a low power standby mode.

## Pin Diagram (Top Side View)
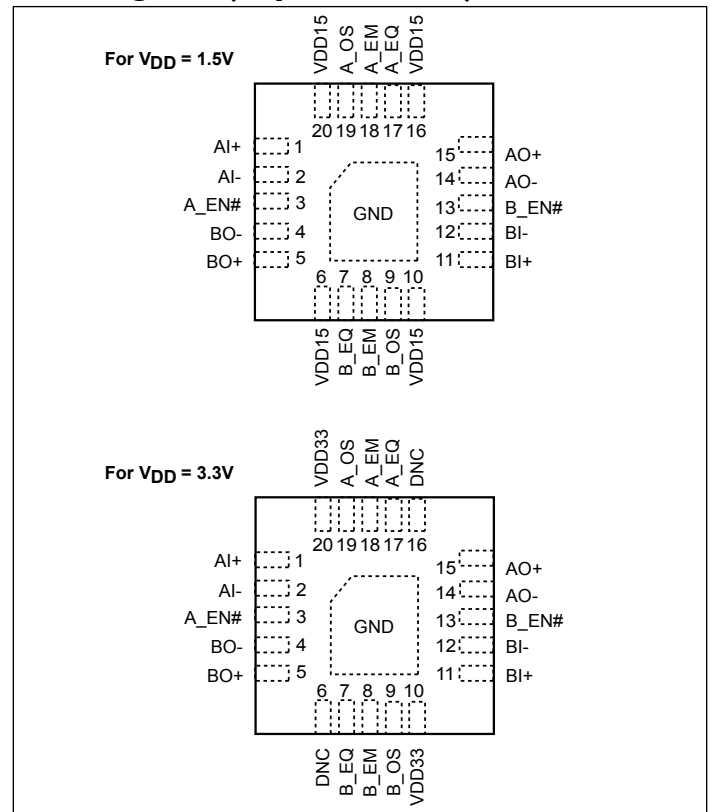
## Pin Description

| 3.3V Supply | 1.5V Supply | Pin Name | Type | Description |
|---|---|---|---|---|
| 18 | 18 | A_EM | Input | Output emphasis adjustment for Channel A. Allows analog resistive adjustment of emphasis. (See configuration tables.) |
| 3 | 3 | A_EN# | Input | Channel A Enable. Low is normal operation. High is power down mode. With internal 200K$\Omega$ pull-down resistor. |
| 17 | 17 | A_EQ | Input | Equalization adjustment. (See Configuration table.) (Tri-level) |
| 19 | 19 | A_OS | Input | Channel A output swing adjustment. Allows analog resistive adjustment of output swing level. (See configuration tables.) |
| 1 2 | 1 2 | AI+ AI- | Input | CML input forward channel A with internal 50W pull-up resistors connected to $V_{BIAS}$ (100$\Omega$ differential). |
| 15 14 | 15 14 | AO+ AO- | Output | CML output channel A with internal 50$\Omega$ pull-up resistors connected to $V_{BIAS}$ (100$\Omega$ differential). |
| 8 | 8 | B_EM | Input | Output emphasis adjustment for channel B. Allows analog resistive adjustment of output emphasis. (See configuration tables.) |
| 13 | 13 | B_EN# | Input | Channel B Enable. Low is normal operation. High is power down mode. With internal 200K$\Omega$ pull-down resistor. |
| 7 | 7 | B_EQ | Input | Channel B equalization adjustment. (Tri-level) |
| 11 12 | 11 12 | BI+ BI- | Input | CML input return channel B with internal 50$\Omega$ pull-up resistor connected to $V_{BIAS}$ (100$\Omega$ differential). |
| 5 4 | 5 4 | BO+ BO- | Output | Positive CML output channel B with internal 50$\Omega$ pull-up resistor connected to $V_{BIAS}$ (100$\Omega$ differential). |
| 9 | 9 | B_OS | Input | Channel B output swing adjustment. Allows analog resistive adjustment of output swing level. See configuration tables. |
| 6, 16 | - | DNC / $V_{DD15}$ | - | Do not connect for 3.3V application, or $V_{DD15}$ for 1.5V application |
| Center Pad | Center Pad | GND | GND | Supply ground. |
| - | 6, 10, 16, 20 | $V_{DD15}$ | Power | Alternate supply voltage, 1.5V |
| 10, 20 | | $V_{DD33}$ / $V_{DD15}$ | Power | $V_{DD33}$ for 3.3V application, or $V_{DD15}$ for 1.5V application |

## Receive Equalizer Configuration Table

| x_EN# | x_EQ | Input Equalization @ 3.0GHz | Function |
|-------|------|------------------------------|----------|
| 1 | X | N/A | Channel x disabled. Hi-impedance terminations |
| 0 | 0 | 8dB | Channel enabled, medium input equalization |
| 0 | 1 | 16dB | Channel enabled, high input equalization |
| 0 | $V_{DD}/2$ | 4dB (Default) | Channel enabled, low input equalization |

## Output Swing Adjustment [1]

| R[A:B]_OS ($\Omega$) | Output Swing, mV ($V_{TX-DIFF-p}$)[2] | |
|---|---|---|
| | 3Gbps | 6Gbps |
| 5.5K | 450 | 600 |
| 5K | 490 | 660 |
| 4.5K | 540 | 730 |
| 4K | 600 | 820 |
| 3.5K | 670 | 910 |
| 3K | 760 | 1,000 |
| 2.5K | 870 | 1,080 |
| 2K | 990 | 1,200 |

**Note:**
1. Suggested initial test values. Exact resistor values will vary depending on PCB design.
2. Auto HDD Rate Detection is ON.

## Output Emphasis Adjustment [1,2]

| R[A:B]_EM ($\Omega$) | Pre-emphasis |
|---|---|
| Do Not Connect | 0dB |
| 14K | +2.0dB |
| 10K | +3.0dB |
| 6K | +4.0dB |
| 2K | +6.0dB |

**Note:**
1. Suggested initial test values. Exact resistor values will vary depending on PCB design.
2. Referenced to output saving of 600mV, will vary as a function of swing, increasing as swing decreases.

**Note:**
$V_{MAX}$ of output can not exceed 1,200mVppd (i.e. $V_{DIFF-PRE}$ can not exceed 1,200mV)

## Maximum Ratings

(Above which useful life may be impaired.  For user guidelines, not tested.)

Storage Temperature.........................................................–65°C to +150°C
Supply Voltage to Ground Potential ($V_{DD33}$)....................–0.5V to +4.5V
Supply Voltage to Ground Potential ($V_{DD15}$)....................–0.5V to +2.5V
DC SIG Voltage.................................................................–0.5V to $V_{DD}$ +0.5V
Current Output ................................................................–25mA to +25mA
Power Dissipation Continuous ............................................... 1W
Junction Temperature (Tj) ...............................................125°C
ESD, Human Body Model.......................................................-7kV to +7kV

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## AC/DC Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{DD\text{-}STANDBY1}$ | Standby Supply Current , 1.5V or 3.3V | [A:B]_EN#=1 | | | 0.056 | mA |
| $I_{DD\text{-}ACTIVE1}$ | Active Supply Current, 1.5 or 3.3V | x_EN# = 0, Output 600mV$_{PP}$, 0dB pre-emph | | 108 | | |
| **1.5V Power Characteristics** [1] | | | | | | |
| $V_{DD15}$ | Power Supply Voltage | | 1.425 | | 1.575 | V |
| $P_{STANDBY15}$ | Standby Supply Power, 1.5V | [A:B]_EN#=1 | | | 0.089 | mW |
| $P_{ACTIVE15}$ | Active Supply Power, 1.5V | x_EN# = 0, Output 600mV$_{PP}$, 0dB pre-emph | | 162 | | |
| $P_{SLUMBER}$ | Supply Power Slumber | | | 22.5 | | |
| **3.3V Power Characteristics** [1] | | | | | | |
| $V_{DD33}$ | Power Supply Voltage | | 3 | | 3.6 | V |
| $P_{STANDBY33}$ | Standby Supply Power, 3.3V | [A:B]_EN#=1 | | | 1.82 | mW |
| $P_{ACTIVE33}$ | Active Supply Power, 3.3V | x_EN# = 0, Output 600mV$_{PP}$, 0dB pre-emph | | 356 | | |
| $P_{SLUMBER}$ | Supply Power Slumber, 3.3V | | | 50 | | |

**Note:**
1. This device can operate from either 1.2V or 3.3V power supply. Note these different device pins are used for the different supply voltages.
   Performance characteristics are the same at either operating voltage.

## AC/DC Electrical Characteristics

### CML Transmitter Output

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $Z_{TX-DIFF-DC}$ | DC Differential TX Impedance | | 85 | 100 | 115 | $\Omega$ |
| $V_{TX-DIFFP-P}$ | Differential Peak-to-peak Output Voltage | $V_{TX-DIFFP-P} = 2 * \mid V_{TX-D+} - V_{TX-D-} \mid$ | 400 | | 1200 | mV |
| $V_{TX-C}$ | Common-Mode Voltage | $\mid V_{TX-D+} + V_{TX-D-} \mid /2$ | 0 | | 2 | V |
| $t_F$, $t_R$ | Transition Time 20% to 80% | | 50 | | 150 | ps |
| $V_{amp\_bal}$ | TX amplitude imbalance | @3Gbps | | | 10 | % |
| $T_{skew}$ | TX differential skew | | | | 20 | ps |
| $V_{cm\_ac}$ | TX AC common mode voltage | @3Gbps | | | 30 | mVpp |
| $V_{TX-Pre-Ratio-max}$ | Max TX Pre-emphasis Level | | | | 6 | dB |
| $S_{dd11\_TX}$ | TX differential mode return loss | 75MHz - 300MHz<br>300MHz - 600MHz<br>600MHz - 1.2GHz<br>1.2GHz - 2.4GHz<br>2.4GHz - 3.0GHz<br>3.0 GHz - 6.5GHz | 14<br>8<br>6<br>6<br>3<br>1 | | | dB |
| $S_{cc11\_TX}$ | TX common mode return loss | 150MHz - 300MHz<br>300MHz - 600MHz<br>600MHz - 1.2GHz<br>1.2GHz - 2.4GHz<br>2.4GHz - 3.0GHz<br>3.0GHz - 5.0GHz | 8<br>5<br>2<br>1<br>1<br>1 | | | dB |
| $S_{dc11\_TX}$ | TX impedance balance | 150MHz - 300MHz<br>300MHz - 600MHz<br>600MHz - 1.2GHz<br>1.2GHz - 2.4GHz<br>2.4GHz - 3.0GHz<br>3.0GHz - 5.0GHz | 30<br>30<br>20<br>10<br>10<br>4 | | | dB |
| **LVCMOS Control Pins** | | | | | | |
| $V_{IH}$ | Input High Voltage (Bi-level) | | $0.65 \times V_{DD}$ | | | V |
| $V_{IL}$ | Input Low Voltage (Bi-level) | | | | $0.35 \times V_{DD}$ | |
| $V_{IH}$ | Input High Voltage (Tri-level) | | $0.8 \times V_{DD}$ | | | |
| $V_{IL}$ | Input Low Voltage (Tri-level) | | | | $0.2 \times V_{DD}$ | |
| $I_{IH}$ | Input High Current | | | | 50 | μA |
| $I_{IL}$ | Input Low Current | | −50 | | | |

## AC/DC Electrical Characteristics Cont.

### CML Receiver Input

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $Z_{RX-DC}$ | DC Input Impedance | | 40 | | | Ω |
| $Z_{RX-DIFF-DC}$ | DC Differential Input Impedance | | 85 | 100 | 115 | |
| $V_{RX-DIFFP-P}$ | Differential Input Peak-to-peak Voltage | | 240 | | 1000 | mV |
| $V_{RX-CM-ACP}$ | AC Peak Common Mode Input Voltage | | | | 100 | mV |
| $V_{TH-SD}$ | OOB Signal detect input Threshold | | 75 | | 200 [1] | mVppd |
| $S_{cc11\_RX}$ | RX common mode return loss | 150MHz - 300MHz<br>300MHz - 600MHz<br>600MHz - 1.2GHz<br>1.2GHz - 2.4GHz<br>2.4GHz - 3.0GHz<br>3.0GHz - 5.0GHz | 5<br>5<br>2<br>1<br>1<br>1 | | | dB |
| $S_{dd11\_RX}$ | RX differential mode return loss | 75MHz-300MHz<br>300MHz - 600MHz<br>600MHz - 1.2GHz<br>1.2GHz - 2.4GHz<br>2.4GHz - 3.0GHz<br>3.0 GHz - 6.5GHz | 18<br>14<br>10<br>8<br>3<br>1 | | | dB |
| $S_{dc11\_RX}$ | RX impedance balance | 150MHz - 300MHz<br>300MHz - 600MHz<br>600MHz - 1.2GHz<br>1.2GHz - 2.4GHz<br>2.4GHz - 3.0GHz<br>3.0GHz - 5.0GHz<br>5.0GHz - 6.5GHz | 30<br>30<br>20<br>10<br>10<br>4<br>4 | | | dB |
| Equalization | | | | | | |
| $T_J$ | Total Jitter p-p | Measured at 6Gbps | | | 0.37 | Ul |
| $D_J$ | Deterministic Jitter | Measured at 6Gbps | | | 0.19 | UI |

**Note:**
1. Using Compliance test at 1.5Gbps and 3Gbps. Also using OOB (OOB is formed by ALIGNp primitive or D24.3) test patterns at 1.5Gbps.
   The ALIGN primitive (K28.5+D10.2+D27.3 = 0011111010+0101010101+0010011100). The D24.3 = 00110011001100110011

## Auto Slumber Mode Entry/Exit Time

| Symbol | Parameter | Conditions | Min. | Typ.[1] | Max. | Units |
|---|---|---|---|---|---|---|
| $T_{SlumberON}$ | Entry time to Slumber Mode | Electrical Idle at Input (See Figure) | | 10 | 20 | μs |
| $T_{SlumberOFF}$ | Exit time from Slumber Mode | After first signal activity (See Figure) | | 6 | 20 | ns |

## Latency

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------|-----------|------------|------|------|------|-------|
| $t_{PD}$ | Latency | | | 750 | | ps |
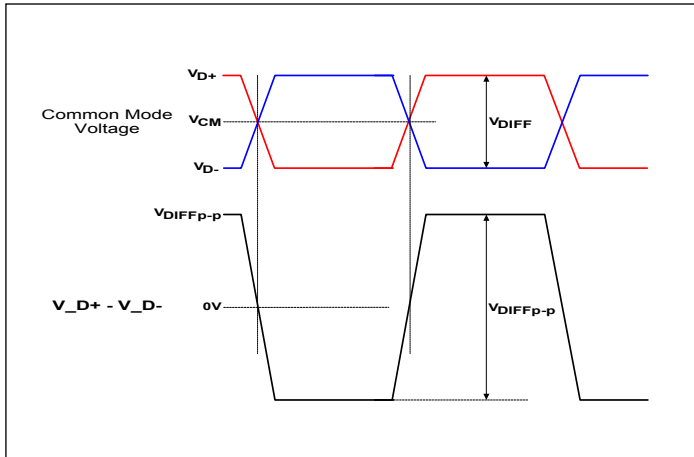


**Definition of Differential Voltage
and Differential Voltage Peak-to-Peak**
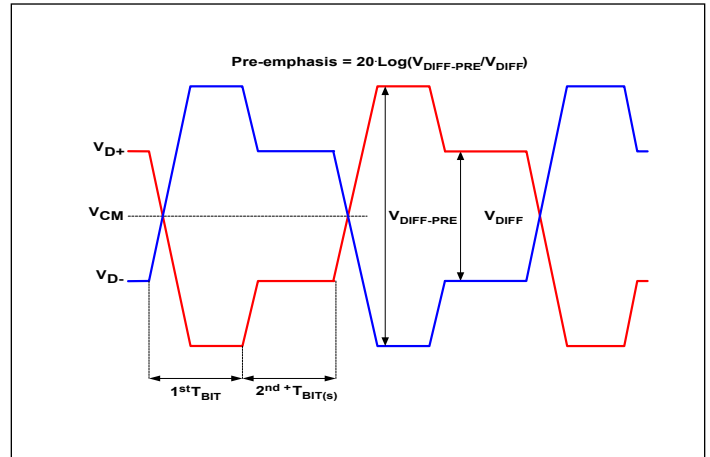


**Definition of Pre-emphasis**
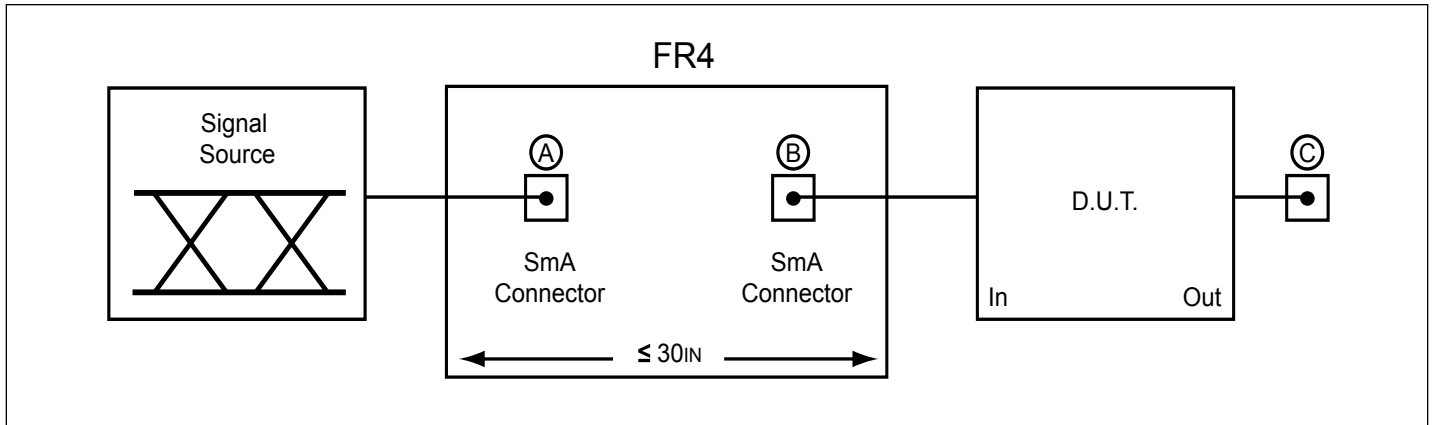


**Test Condition Referenced in the Electrical Characteristic Table**
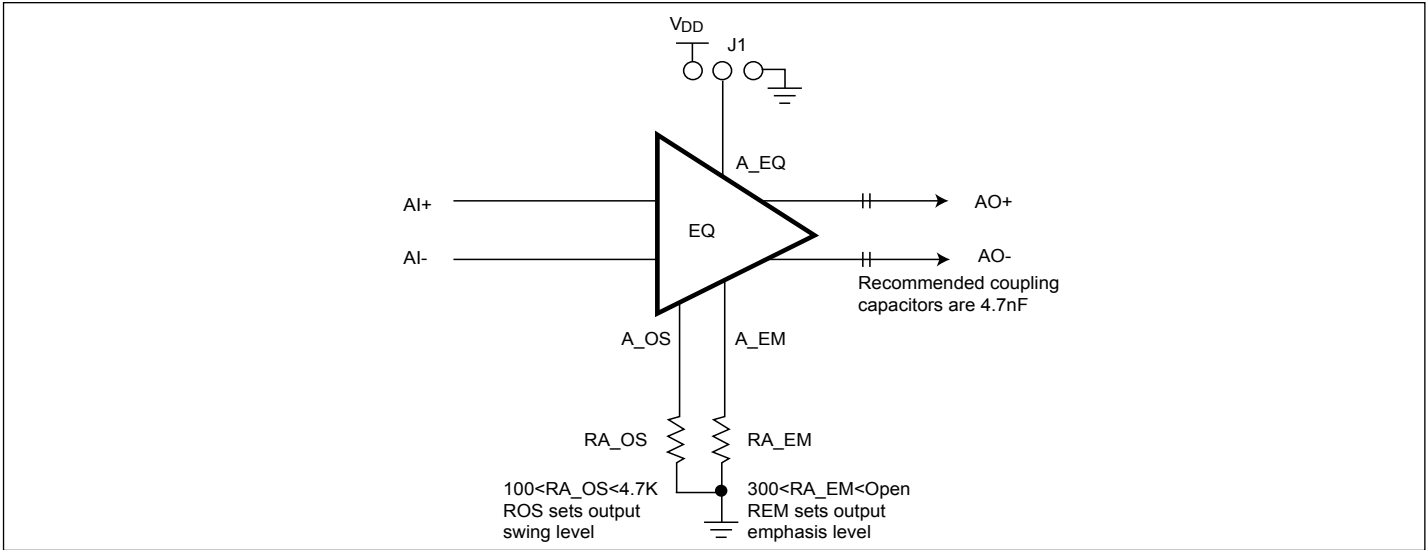
**Implementation Diagram**

VDD  J1

A_EQ

AI+ → EQ → AO+

AI- → AO-

Recommended coupling capacitors are 4.7nF

A_OS    A_EM

RA_OS    RA_EM

100<RA_OS<4.7K
ROS sets output
swing level

300<RA_EM<Open
REM sets output
emphasis level
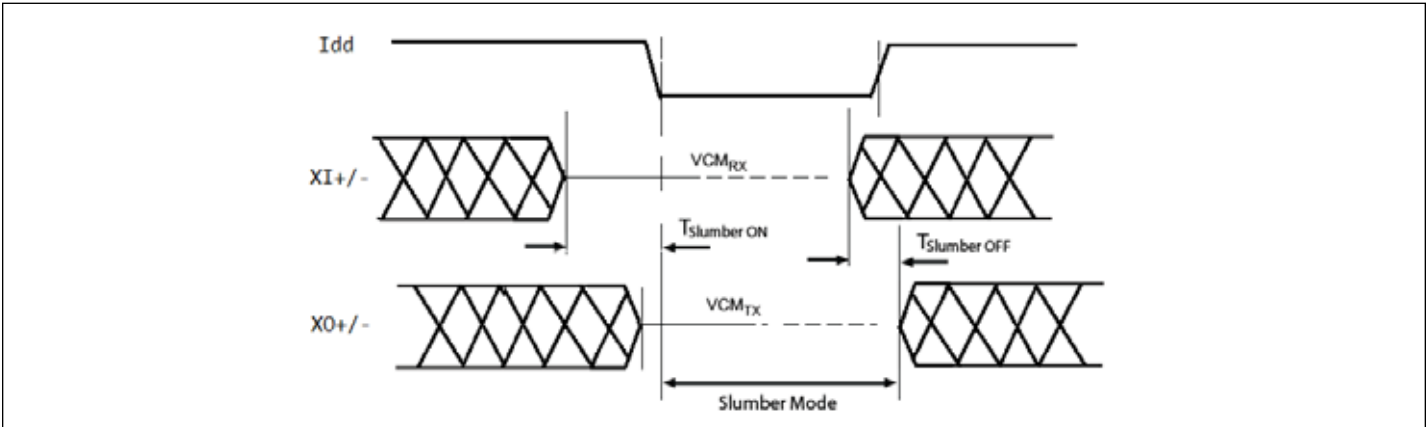


**Auto Slumber Mode Entry and Exit Timing**

Idd

XI+/-    VCM_RX

T_Slumber ON    T_Slumber OFF

XO+/-    VCM_TX

Slumber Mode

## Part Marking
ZD Package

EQX68
01AZDE
YYWWXX
○
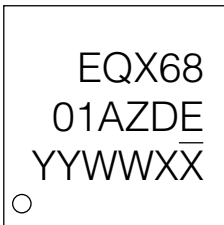
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

## Packaging Mechanical: 20-TQFN (ZD)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
   COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.08 mm.
4. REFER JEDEC MO−220.

| ⚡PERICOM® Semiconductor Corporation | DATE: 09/11/08 |
|---|---|
| DESCRIPTION: 20-Lead, Thin Fine Pitch Quad Flat No-Lead (TQFN) | |
| PACKAGE CODE:  ZD20 | |
| DOCUMENT CONTROL #: PD-2084 | REVISION: -- |
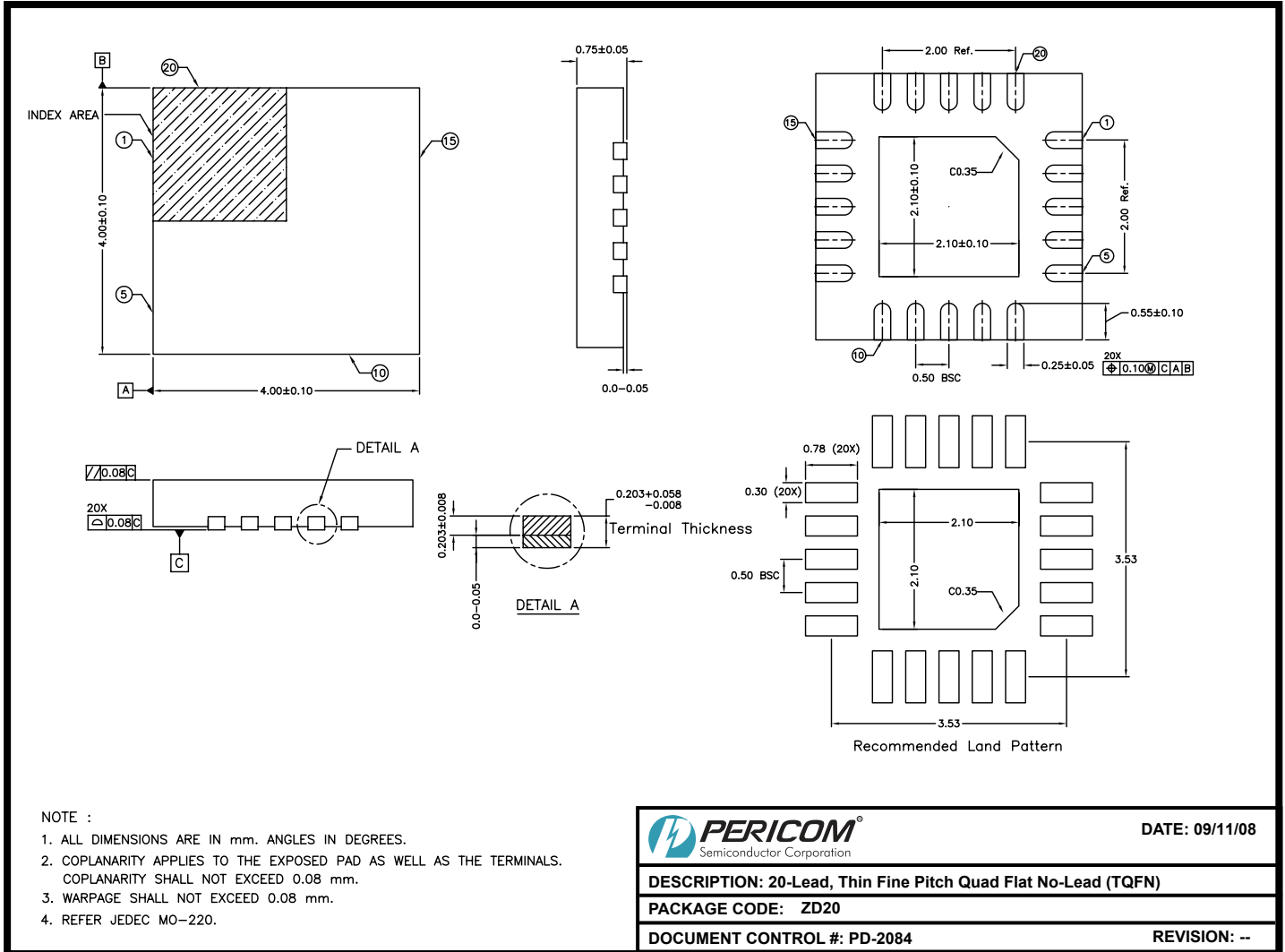
08-0456

**For latest package info.**

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

## Ordering Information

| Ordering Number | Package Code | Package Description |
|---|---|---|
| PI3EQX6801AZDEX | ZD | 20-Lead, Thin Fine Pitch Quad Flat No-Lead (TQFN) |

**Notes:**

1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
3. E = Pb-free and Green
4. X suffix = Tape/Reel

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