PI3HDX1204B1

HDMI 2.0 6Gbps Limiting ReDriver with High EQ, Low Jitter and DP++ Level Shift

Description

PI3HDX1204B1 is suitable for HDMI 2.0 6.0 Gbps ReDriver with programmable high equalization, output swing and de-emphasis control mode. Max EQ is +22dB @ 6Gbps and can deliver 2x better additive jitter performance than other traditional ReDriver.

In addition, it can supports the Dual-mode DisplayPort Level Shifter application for HDMI 2.0 compliant output signals.

The device EQ/SW/De-emphasis configuration can be supported by either the pin-strapping or the I^2C programming to optimize differential signal performance over the variety of physical mediums.

Features

- **HDMI 2.0 compliant Limiting-type Redriver to compensate high insertion loss of the long TMDS signal transmission**
- **Support Dual-mode DP HBR3 to HDMI 2.0 Level Shifting**
- **Double the jitter performance than conventional CMOS-process redriver**
- **Input EQ support 16 steps up to +22.2dB @ 3GHz (6 Gbps), 4 steps De-emphasis and 4 steps output voltage swing setting**
- **Independent each channel configuration for Equalization, Output Swing and De-emphasis**
- **Built-in channel activity detector with selectable input termination between 50Ω to V_{DD} and 200kΩ to V_{DD}**
- **Pin Strap and I^2C selectable device programming mode support**
- **Supply Voltage: 3.3V**
- **Industrial Temperature Range: -40°C to 85°C**
- **Packaging (Pb-free & Green): 42-contact TQFN (3.4x9mm)**

Applications

- Notebooks, Desktops and AIO PCs
- HDMI Active cables
- Internal board connection inside Video system

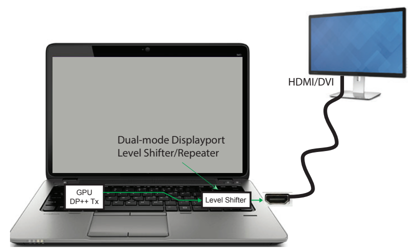


Figure 1-1 DP++ to HDMI 2.0 Level Shifter

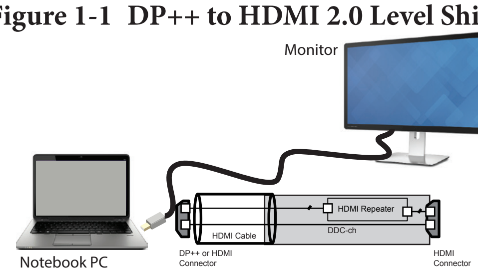


Figure 1-2 HDMI 2.0 Active cable application

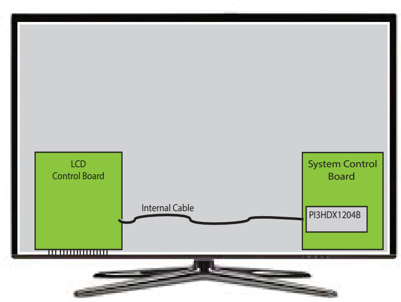


Figure 1-3 TMDS Connection inside TV

Ordering Information

Ordering Number	Package Code	Package Description
PI3HDX1204B1 ZHE	ZH	Pb-free & Green 42-pin TQFN (3.5x9mm)
PI3HDX1204B1 ZHEX	ZH	Pb-free & Green 42-pin TQFN (3.5x9mm), Tape & Reel.
PI3HDX1204B1 ZHIEX	ZH	Industrial-temp, Pb-free & Green 42-pin TQFN (3.5x9mm), Tape & Reel.

Suffix: I = Industrial Temp, E = Pb-free and Green, X = Tape/Reel

Revision History

Revision	Description
June 2016	Electrical chapter: PI3HDX1204-B revision to improve TMDS clock rising and falling time from typ 50ps to 70ps. De-emp [1:0] range adjusted between 0 and -2.1dB. Package and pin-out are same as PI3H-DX1204-B.
July 2016	Application chapter: Updated reference schematics in application chapter. Add load switch AP2151 re-quirement to protect sink to source-side devices back drive.
Sep 2016	Finial datasheet release with package pin-out typo fixed - pin name 30, 37 and 38

Contents

2. Pin Configuration

2.1 Package Pin-out

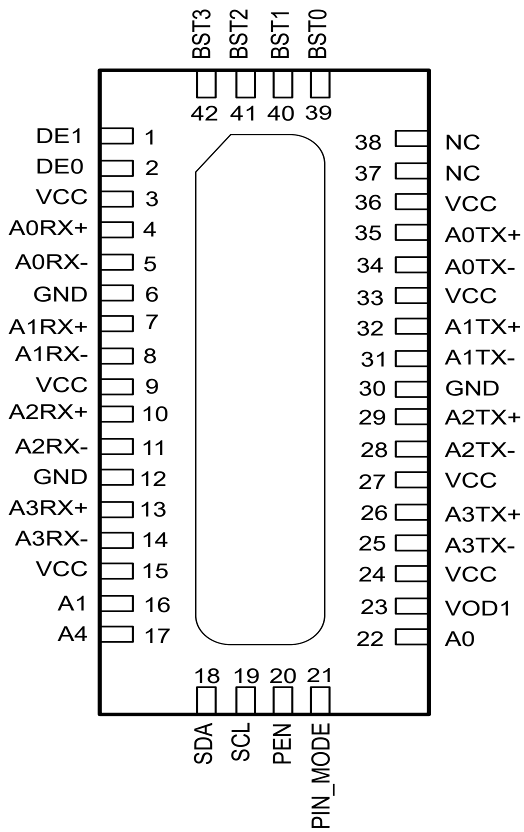


Figure 2-1 Package Pin-out (Top-Side View)

2.1 Pin Description

Pin #	Pin Name	Type	Description
Data Signals			
4 5	A0RX+ A0RX-	I	TMDS inputs for Channel A0, with internal 50-Ohm Pull-Up and ~200k-Ohm Pull-Up otherwise.
35 34	A0TX+, A0TX-	O	TMDS outputs for Channel A0, with internal 50-Ohm Pull-Up and ~2k-Ohm Pull-Up otherwise.
7 8	A1RX+, A1RX-	I	TMDS inputs for Channel A1, with internal 50-Ohm Pull-Up and ~200k-Ohm Pull-Up otherwise.
32 31	A1TX+, A1TX-	O	TMDS outputs for Channel A1, with internal 50-Ohm Pull-Up and ~2k-Ohm Pull-Up otherwise.
10 11	A2RX+, A2RX-	I	TMDS inputs for Channel A2, with internal 50-Ohm Pull-Up and ~200k-Ohm Pull-Up otherwise.
29 28	A2TX+, A2TX-	O	TMDS outputs for Channel A2, with internal 50-Ohm Pull-Up and ~2k-Ohm Pull-Up otherwise.
13 14	A3RX+, A3RX-	I	TMDS inputs for Channel A3, with internal 50-Ohm Pull-Up and ~200k-Ohm Pull-Up otherwise.
26 25	A3TX+, A3TX-	O	TMDS outputs for Channel A3, with internal 50-Ohm Pull-Up and ~2k-Ohm Pull-Up otherwise.
Control Signals			
19	SCL	I	I^2C Clock input.
18	SDA	I/O	I^2C Data input/output.
17, 16, 22	A4, A1, A0	I	I^2C programmable address bits, with internal 100k-Ohm Pull-Up.
20	PEN	I	Power Enable with internal 100K-Ohm Pull-Up
21	Pin_Mode	I	Input with internal 100k-Ohm Pull-Up. When HIGH, each channel is programmed by the external pin voltage. When LOW, each channel is programmed by the data stored in the I^2C bus.
42 41 40 39	BST[3:0]	I	Inputs with internal 100k-Ohm Pull-Up. This pins set the amount of Equalizer Boost in all channel when Pin mode is HIGH.
23	VOD1	I	Inputs with internal 100k-Ohm Pull-Up. This pin sets the output Voltage Level in all channel when Pin mode is HIGH.
1 2	DE[1:0]	I	Inputs with internal 100k-Ohm Pull-Up. This pins set the output De-Emphasis Level in all channel when Pin_Mode is HIGH.
38 37	NC	NC	No Connect

Power Pins			
6, 12, 30, Center Pad	GND	GND	Ground Pins
3, 9, 15, 24, 27, 33, 36	V_{DD}	PWR	Power Supply Pins

3. Functional Description

3.1 Functional Block Diagram

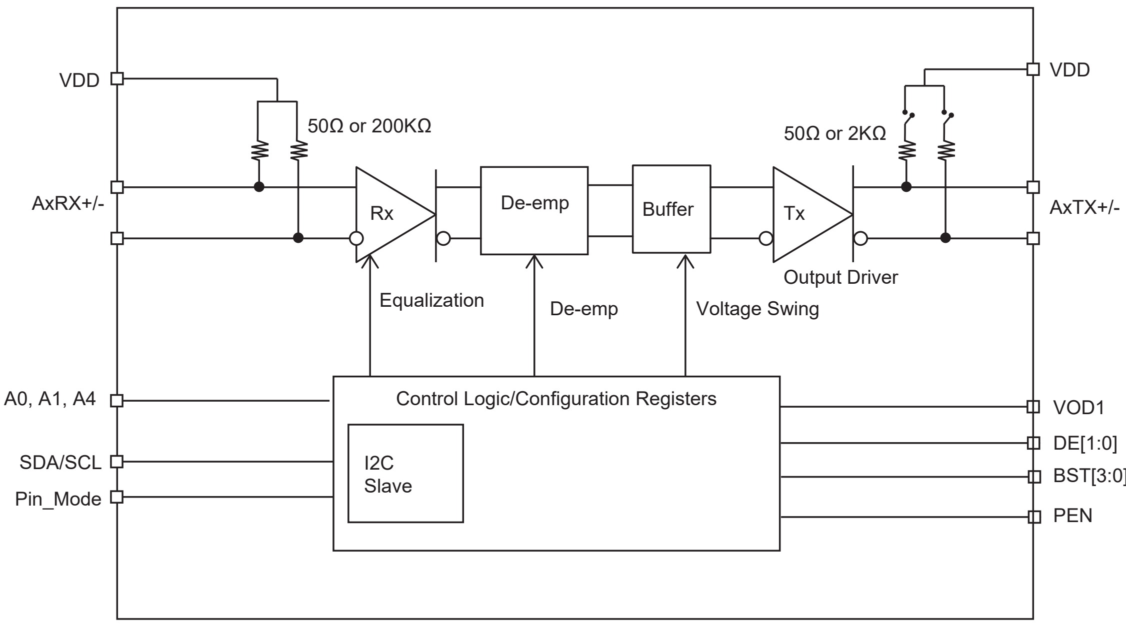


Figure 3-1 Functional block diagram

3.2 Function settings

3.2.1 Output Termination Detector

On power up or when PEN becomes true, the output resistance is set to 2K ohms, and the input resistance is set to 200K ohms. The device continually looks to detect an external 50 ohm termination resistor on a per channel basis. If no 50 ohms is detected in the first 5ms of time, the channel is continually polled with 5ms detection cycle until detection occurs.

3.2.2 Input Activity Detector

When the input voltage on individual channel basis falls below de-assert threshold VTH-, the output is driven to the common mode voltage so as to eliminate output chatter. When the input voltage is higher than assert threshold VTH+, the channel is resumed immediately.

3.2.3 Power Enable function

One pin control or I2C control, when PEN is set to low, the IC goes into power down mode, both input and output termination set to 200K and 2K respectively. Individual Channel Enabling is done through the I2C register programming.

3.2.4 Equalization Setting

BST[3:0] are the selection pins for the equalization selection for each channel.

Table 3-1. Table 1. Equalization Setting

BST3	BST2	BST1	BST0	6Gbps (3GHz)	8Gbps (4GHz)
0	0	0	0	0.25 dB	0.4 dB
0	0	0	1	0.8 dB	1.1 dB
0	0	1	0	1.1 dB	1.6 dB
0	0	1	1	2.2 dB	3.1 dB
0	1	0	0	4.1 dB	5.4 dB
0	1	0	1	7.1 dB	8.9 dB
0	1	1	0	9.0 dB	10.8 dB
0	1	1	1	10.3 dB	12.2 dB
1	0	0	0	11.8 dB	13.8 dB
1	0	0	1	13.9 dB	15.8 dB
1	0	1	0	15.3 dB	17.3 dB
1	0	1	1	16.9 dB	19.0 dB
1	1	0	0	17.9 dB	20.0 dB
1	1	0	1	19.2 dB	21.3 dB
1	1	1	0	20.5 dB	22.6 dB
1	1	1	1	22.2 dB	24.3 dB

3.2.5 Output De-emphasis Setting

De-emphasis Setting: DE[1:0] are the selection bits for the de-emphasis value.

Table 3-2. Output De-emphasis Setting

DE1	DE0	De-emphasis
0	0	0 dB
0	1	-0.5 dB
1	0	-0.7 dB
1	1	-1.0 dB

3.2.6 Swing Setting

Swing Setting: VOD1 is the selection bit for the output swing voltage value.VOD0 fixed as 1.

Table 3-3. Output Voltage Swing Setting

VOD1	VOD0	Output Voltage Swing
0	1	0.85 Vppd
1	1	1.15 Vppd

3.2.7 Activity Detector Threshold

Threshold Setting: VTH[1:0] are the selection bits for the activity detector threshold.

Table 3-4. Activity Detector Threshold Setting

VTH1	VTH0	VTH+ (Assert threshold)	VTH- (De-assert threshold)	Units
0	0	130	30	mVppd
0	1	150	50	
1	0	170	70	
1	1	210	110	

3.3 Output Eye Diagram changes with Different EQ setting

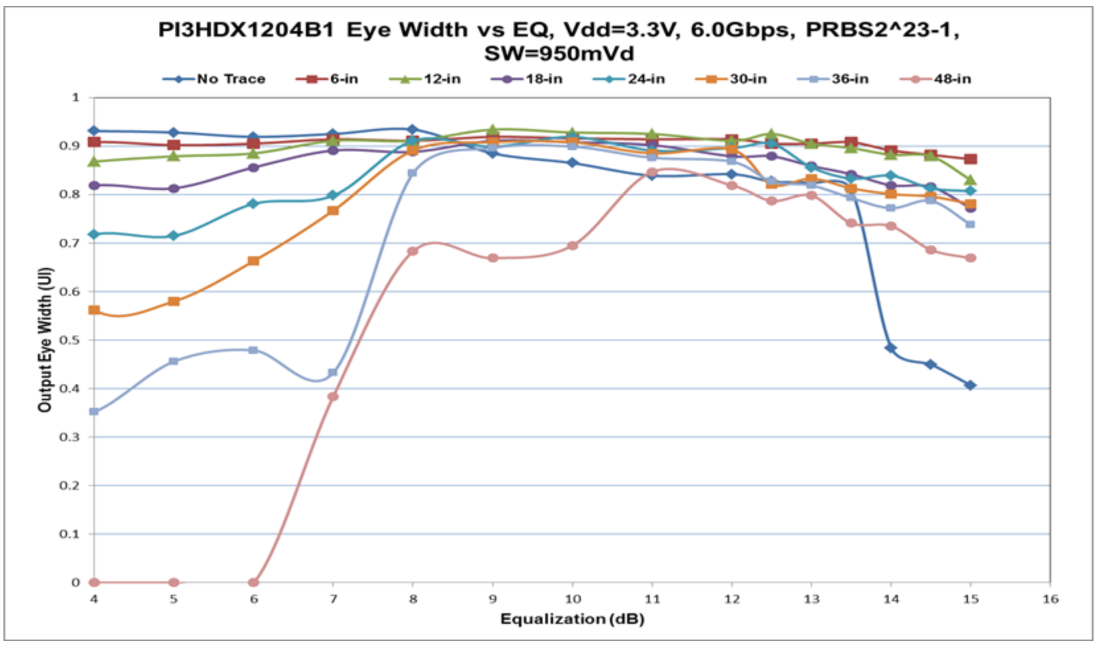


Figure 3-2 Eye Width vs. Input Equalization at Different Input trace Lengths

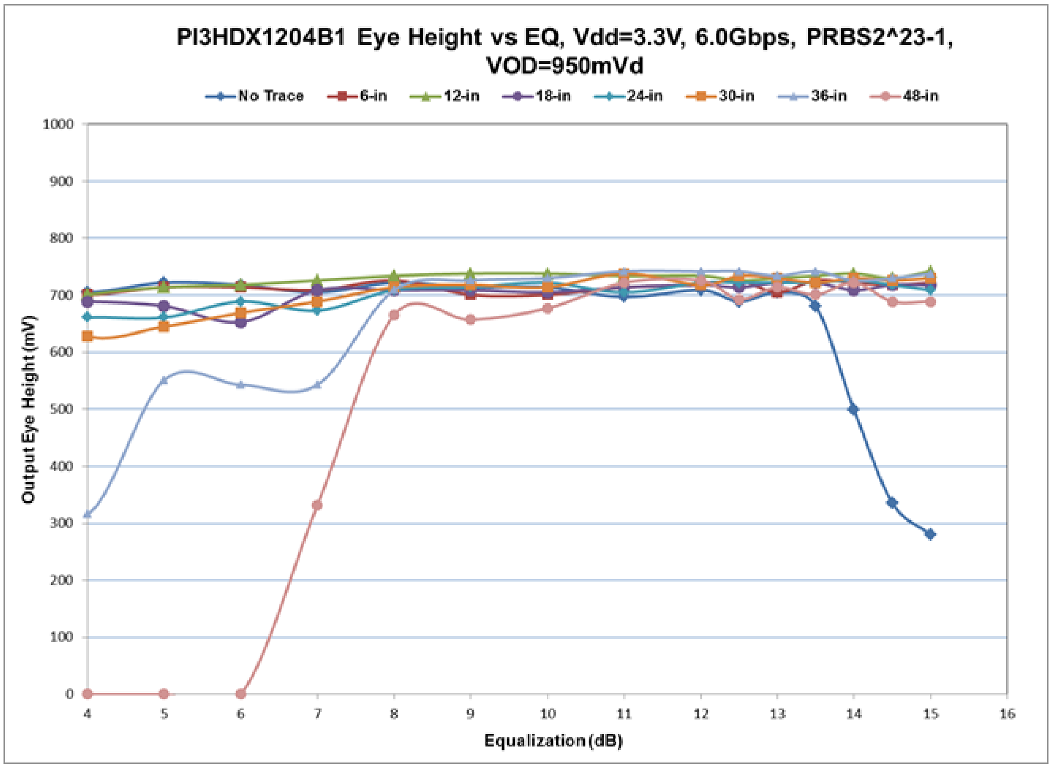
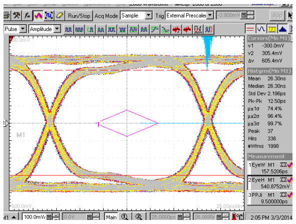
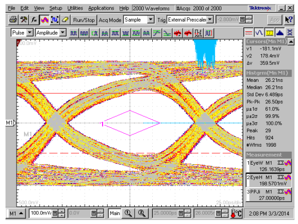


Figure 3-3 Eye Height vs. Input Equalization at Different Input trace Lengths

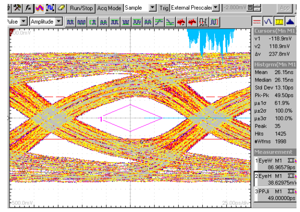
Table 3-5. Input Eye Diagram without trace boards



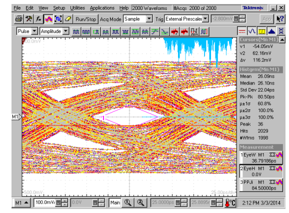
6-in trace



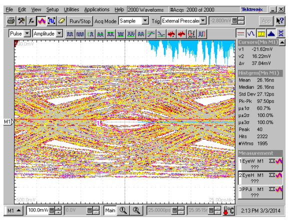
18-in trace



24-in trace

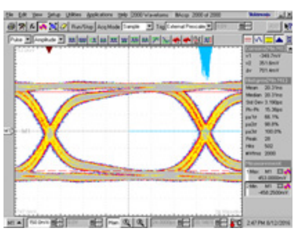


30-in trace

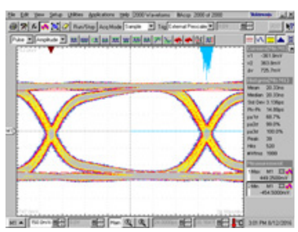


36-in trace

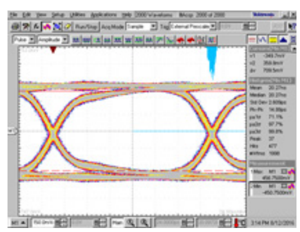
Table 3-6. Output Eye Opening with trace and different EQ Settings, 6.0 Gbps, Vdd=3.3V, 25C



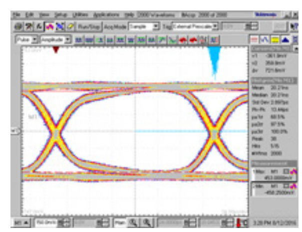
6-in trace
EQ=0001 (0.8dB)



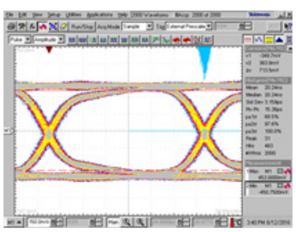
12-in trace
EQ=0100(4.1dB)



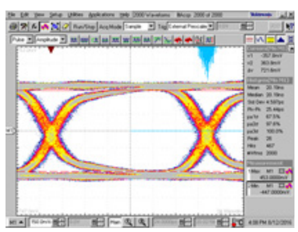
18-in trace
EQ=0110(9.0dB)



24-in trace
EQ=0111(10.3dB)



30-in trace
EQ=0111(10.4dB)



48-in trace
EQ=1000(11.8dB)

Note: Trace Card Loss Informations is shown below.

Frequency	3 GHz	6GHz	Units
6 inch Input Trace	-2.1	-4	dB
12 inch Input Trace	-4	-7.5	dB
18 inch Input Trace	-6.1	-11.3	dB
30 inch Input Trace	-10.14	-18	dB
36 inch Input Trace	-12.13	-22	dB
48 inch Input Trace	-16.42	-29	dB

4. I2C Programming

4.1 Address assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	Controlled by Pin# A4	0	0	Program Controlled by Pin# A1	Program Controlled by Pin# A0	1=R, 0=W

BYTE 0				
Bit	Type	Power up condition	Control affected	Comment
7	R		Ch3 Activity Detector	1 = Activity 0 = No activity
6	R		Ch2 Activity Detector	
5	R		Ch1 Activity Detector	
4	R		Ch0 Activity Detector	
[3:0]	R	0	Not used	

BYTE 1				
Bit	Type	Power up condition	Control affected	Comment
[7:0]	R	0	Not used	

BYTE 2				
Bit	Type	Power up condition	Control affected	**Comment**
7	R/W	Latch from PEN input at startup	Ch3 Enable	1 = Enable
6	R/W		Ch2 Enable	
5	R/W		Ch1 Enable	
4	R/W		Ch0 Enable	
[3:0]	R/W	0	Not used	

BYTE 3				
Bit	**Type**	**Power up condition**	**Control affected**	**Comment**

7	R/W	Latch from BST[3:0] at startup	BST3 Ch1	
6	R/W		BST2 Ch1	
5	R/W		BST1 Ch1	
4	R/W		BST0 Ch1	
3	R/W		BST3 Ch0	
2	R/W		BST2 Ch0	
1	R/W		BST1 Ch0	
0	R/W		BST0 Ch0	

BYTE 4

Bit	Type	Power up condition	Control affected	Comment
7	R/W	Latch from BST[3:0] at startup	BST3 Ch3	
6	R/W		BST2 Ch3	
5	R/W		BST1 Ch3	
4	R/W		BST0 Ch3	
3	R/W		BST3 Ch2	
2	R/W		BST2 Ch2	
1	R/W		BST1 Ch2	
0	R/W		BST0 Ch2	

BYTE 5

Bit	Type	Power up condition	Control affected	Comment
7	R/W	Latch from VOD1 at startup	VOD1 Ch3	
6	R/W	VOD0 = "1"	VOD0 Ch3	
5	R/W	Latch from VOD1 at startup	VOD1 Ch2	
4	R/W	VOD0 = "1"	VOD0 Ch2	
3	R/W	Latch from VOD1 at startup	VOD1 Ch1	
2	R/W	VOD0 = "1"	VOD0 Ch1	
1	R/W	Latch from VOD1 at startup	VOD1 Ch0	
0	R/W	VOD0 = "1"	VOD0 Ch0	

BYTE 6

Bit	Type	Power up condition	Control affected	Comment

7	R/W	Latch from DE[1:0] at startup	DE1 Ch3	
6	R/W		DE0 Ch3	
5	R/W		DE1 Ch2	
4	R/W		DE0 Ch2	
3	R/W		DE1 Ch1	
2	R/W		DE0 Ch1	
1	R/W		DE1 Ch0	
0	R/W		DE0 Ch0	

BYTE 7: Reserved

BYTE 8				
Bit	Type	Power up condition	Control affected	**Comment**
7	R/W	1	Ch3 RX detect PD	1 = power down
6	R/W	1	Ch2 RX detect PD	
5	R/W	1	Ch1 RX detect PD	
4	R/W	1	Ch0 RX detect PD	
3	R/W	0	Ch3 RX reset	1 = reset
2	R/W	0	Ch2 RX reset	
1	R/W	0	Ch1 RX reset	
0	R/W	0	Ch0 RX reset	

BYTE 9				
Bit	Type	Power up condition	Control affected	**Comment**
7	R/W	0	Ch3 Activity Detector Enable	1=inactive
6	R/W	0	Ch2 Activity Detector Enable	
5	R/W	0	Ch1 Activity Detector Enable	
4	R/W	0	Ch0 Activity Detector Enable	
[3:0]	R/W	0	Not use	

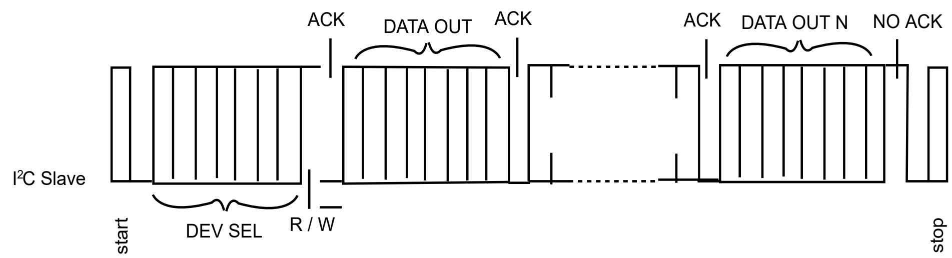
BYTE A				
Bit	Type	Power up condition	Control affected	**Comment**

7	R/W	0	Ch3 Activity Detector Threshold VTH1	
6	R/W	0	Ch3 Activity Detector Threshold VTH0	
5	R/W	0	Ch2 Activity Detector Threshold VTH1	
4	R/W	0	Ch2 Activity Detector Threshold VTH0	
3	R/W	0	Ch1 Activity Detector Threshold VTH1	
2	R/W	0	Ch1 Activity Detector Threshold VTH0	
1	R/W	0	Ch0 Activity Detector Threshold VTH1	
0	R/W	0	Ch0 Activity Detector Threshold VTH0	

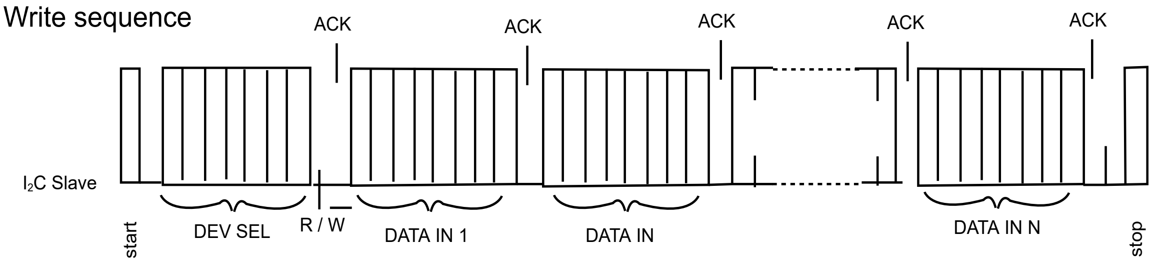
BYTE B-F : RESERVED

4.2 I²C Data Transfer Sequence

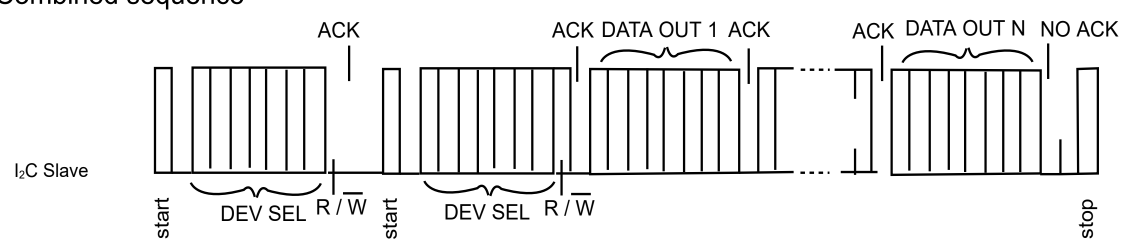
Read sequence



Write sequence



Combined sequence



Notes:
1. only block read and block write from the lowest byte are supported for this application.
2. for some I2C application, an offset address byte will be presented at the second byte in write command, which is called dummy byte here and will be simply ignored in this application for correct interoperation.

5. Electrical

5.1 Absolute Maximum Ratings

Supply Voltage to Ground Potential. . . . .–0.5 V to +4.6 V
DC SIG Voltage . . . .–0.5 V to V_{DD} + 0.5 V
Output Current . . . . –25 mA to +25 mA
Power Dissipation Continuous. . . . . 2.1 W
ESD, HBM . . . . –2 kV to +2 kV
Storage Temperature . . . .–65 °C to +150 °C

Note
(1) Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.2 Recommended Operation Conditions

Parameter	Min.	Typ.	Max	Units
Power supply voltage (VDD to GND)(1)	3.0	3.3	3.6	V
I2C (SDA, SCL)			3.6	V
Supply Noise Tolerance up to 25 MHz (2)			100	mVp-p
Ambient Temperature	-40	25	85	°C

Note
(1) Typical parameters are measured at VDD = 3.3 ± 0.3V, TA = 25°C. They are for the reference purposes, and are not production-tested
(2) Allow supply noise (mVp-p sine wave) under typical condition

5.3 DC/AC Characteristics

5.3.1 LVCMOS DC specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{IH}	DC input logic high		$V_{DD}/2 + 0.7$		$V_{DD} + 0.3$	V
V_{IL}	DC input logic low		-0.3		$V_{DD}/2 - 0.7$	V
V_{OH}	At I_{OH} = -200µA		$V_{DD} + 0.2$			V
V_{OL}	At I_{OL} = -200µA				0.2	V
V_{hys}	Hysteresis of Schmitt trigger input		0.8			V

5.3.2 Power Dissipation

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{max}	Supply Current	PEN = 1, EQ = 0dB, De-emphasis = 0dB, All 4 channels 0.8V Swing		265	325	mA
		PEN = 1, EQ = 0dB, De-emphasis = 0dB, All 4 channels 1.3V Swing		300	350	mA
I_{DDQ}	Quiescent Supply Current	PEN=0, TMDS Output Disable		0.17		mA
P_{idle}	Standby Mode Supply Power	PEN=0, All channels disable		0.8		mA

5.3.3 Package power ratings

Package	Theta Ja(still air) (°C/W)	Theta Jc (°C/W)	Max. Power Dissipation Rating (Ta ≤ 70°)
42-pin TQFN (ZH42)	33.69	15.17	1.63W

5.3.4 TMDS Differential Pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Single-ended High Level Output Voltage	VDD = 3.3 V, Rout = 50 Ohm	V_{DD}-10		V_{DD}+10	mV
V_{OL}	Single-ended Low Level Output Voltage		V_{DD}-600		V_{DD}-400	mV
V_{swing}	Output Voltage Swing		700		1300	mVppd
R_T	Input Termination Resistance	V_{IN} = 2.9V	45	50	55	Ohm
I_{OZ}	Leakage Current with Hi-Z I/O	V_{DD} = 3.6V			10	uA

5.3.5 Switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{pd}	Propagation Delay				2000	ps
T_r	Tx Signal Rise Time (20% - 80%)	VDD = 3.3V, RT = 50 Ohm, Pre-/De-emp = 0 dB		70		ps
T_f	Tx Signal Fall Time (80% - 20%)			70		ps
$T_{sk(p)}$	Pulse Skew			10	50	ps
$T_{sk(D)}$	Intra-pair Differential Skew			23	50	ps
$T_{sk(O)}$	Inter-pair Differential Skew				100	ps
$T_{Jit-Clk}$	Peak-to-peak Output Jitter for Clock channel	Pre-/De-emp = 0 dB Data Input = 6 Gbps HDMI Pattern, Clock input = 150 MHz		15	30	ps
$T_{Jit-Data}$	Peak-to-peak Output Jitter for Data channels			18	50	ps
t_{sx}	Select to switch Output				10	ns
t_{en}	Enable Time				200	ns
t_{dis}	Disable Time				10	ns

5.3.6 Signal Detector

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Vth+	Assert Threshold of Signal Detector	Signal swing @ 3GHz	130		210	mVppd
Vth-	De-assert Threshold of Signal Detector	Signal swing @ 100 MHz	30		110	mVppd

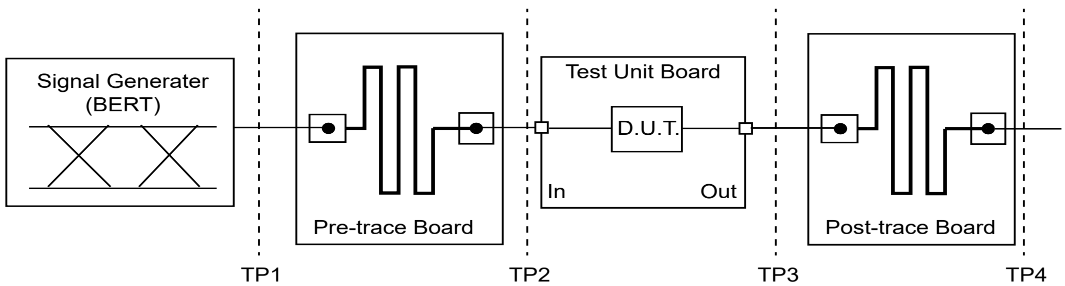


Figure 5-1 Electrical parameter test setup

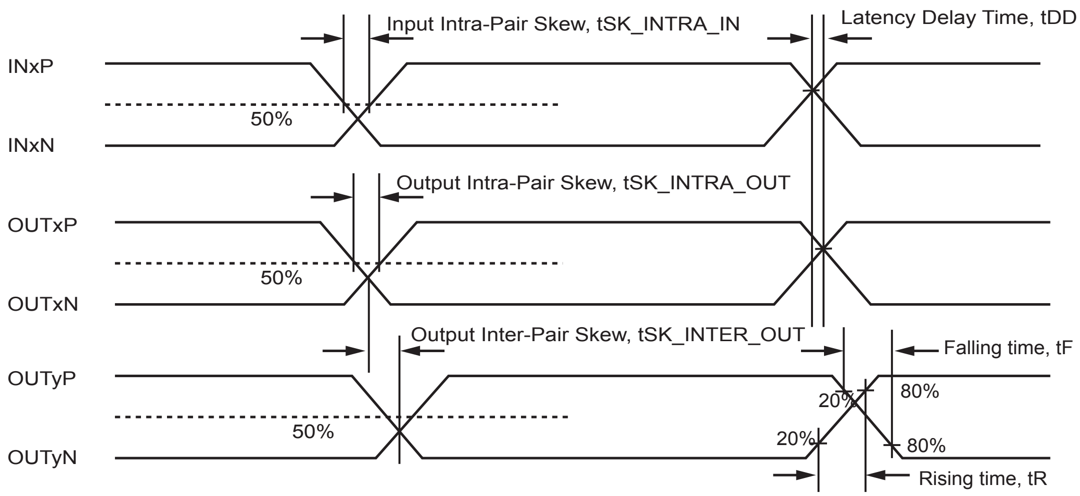


Figure 5-2 Intra and Inter-pair Differential Skew definition

Common Mode Voltage

V_{CM} = (|VD+ + VD-| / 2)

V_{CMP} = (max |VD+ + VD-| / 2)

V_D + -V_D-

Symmetric Differential Swing

$V_{DIFFp-p}$ = (2 * max $|V_{D+} - V_{D-}|$)

Asymmetric Differential Swing

$V_{DIFFp-p}$ = (max $|V_{D+} - V_{D-}|$ $\{V_{D+} > V_{D-}\}$

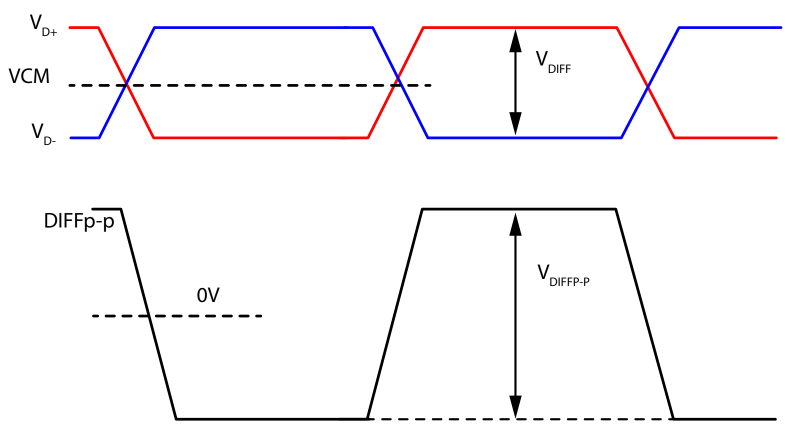


Figure 5-3 Definition of Peak-to-peak Differential voltage

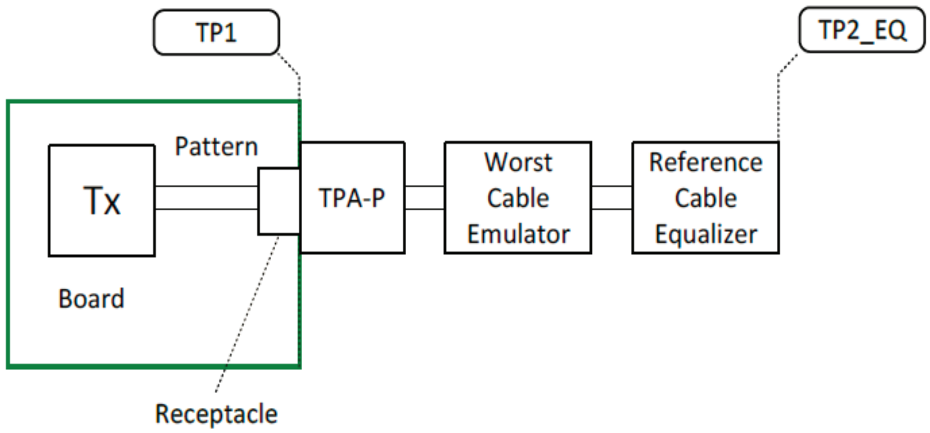


Figure 5-4 HDMI Source Test Point for Eye Diagram

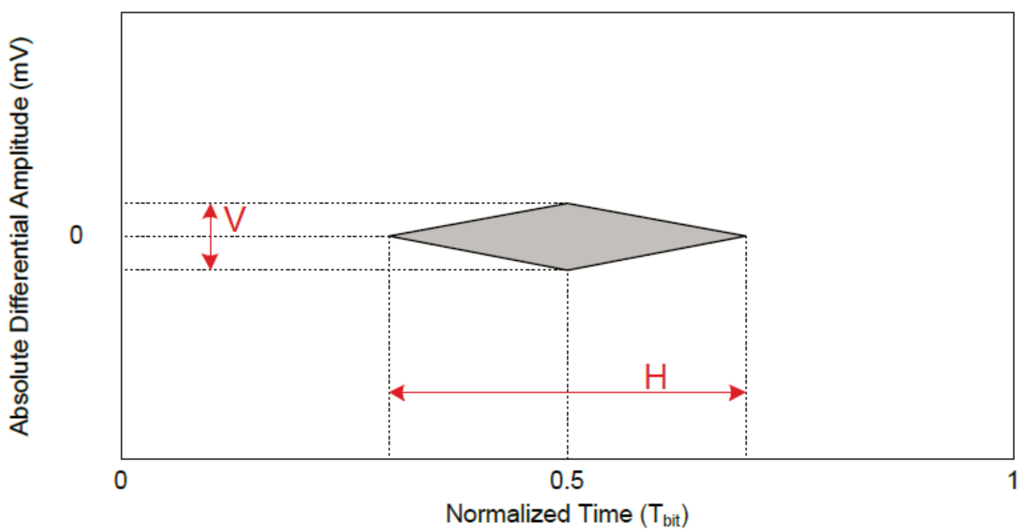


Figure 5-5 HDMI Sink Test Point for Eye Diagram

5.4 I2C Bus

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
VDD	Nominal Bus Voltage		3.0		3.6	V
Freq	Bus Operation Frequency				400	kHz
V_{IH}	DC input logic high		$V_{DD}/2 + 0.7$		$V_{DD} + 0.3$	V
V_{IL}	DC input logic low		-0.3		$V_{DD}/2 - 0.7$	V
V_{OL}	DC output logic low	$I_{OL} = 3mA$			0.4	V
Ipullup	Current Through Pull-Up Resistor or Current Source	High Power specification	3.0		3.6	mA
Ileak-bus	Input leakage per bus segment		-200		200	uA
Ileak-pin	Input leakage per device pin			-15		uA
CI	Capacitance for SDA/SCL				10	pF
tBUF	Bus Free Time Between Stop and Start condition		1.3			us
tHD:STA	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	At pull-up, Max	0.6			us
TSU:STA	Repeated start condition setup time		0.6			us
TSU:STO	Stop condition setup time		0.6			us
THD:DAT	Data hold time		0			ns
TSU:DAT	Data setup time		100			ns
tLOW	Clock low period		1.3			us
tHIGH	Clock high period		0.6		50	us
tF	Clock/Data fall time				300	ns
tR	Clock/Data rise time				300	ns
tPOR	Time in which a device must be operation after power-on reset				500	ms

Note:
(1) Recommended maximum capacitance load per bus segment is 400pF.
(2) Compliant to I2C physical layer specification.
(3) Ensured by Design. Parameter not tested in production.

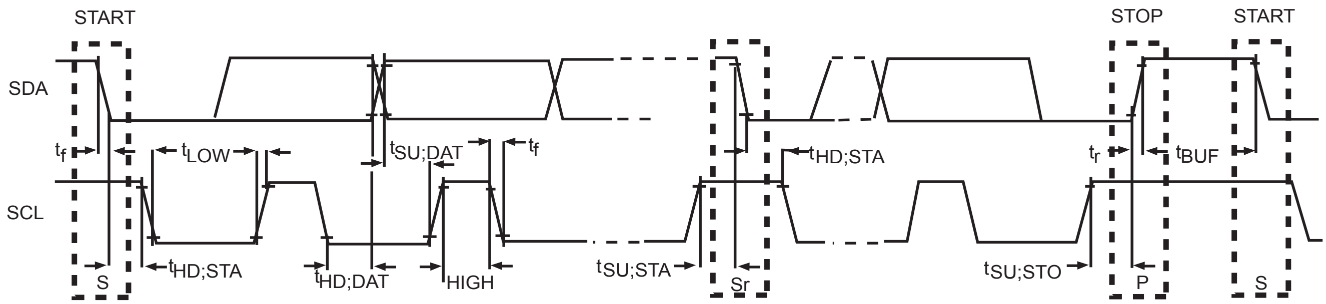


Figure 5-6 I2C Timing Diagram

6. Application/Implementation

6.1 Source Application

PI3HDX1204B1 is designed to accept AC-coupled as well as DC-coupled main link signals. When a dual-mode DP source is connected to the input of PI3HDX1204B1 in a source application, AC coupling capacitors must be placed at the input side.

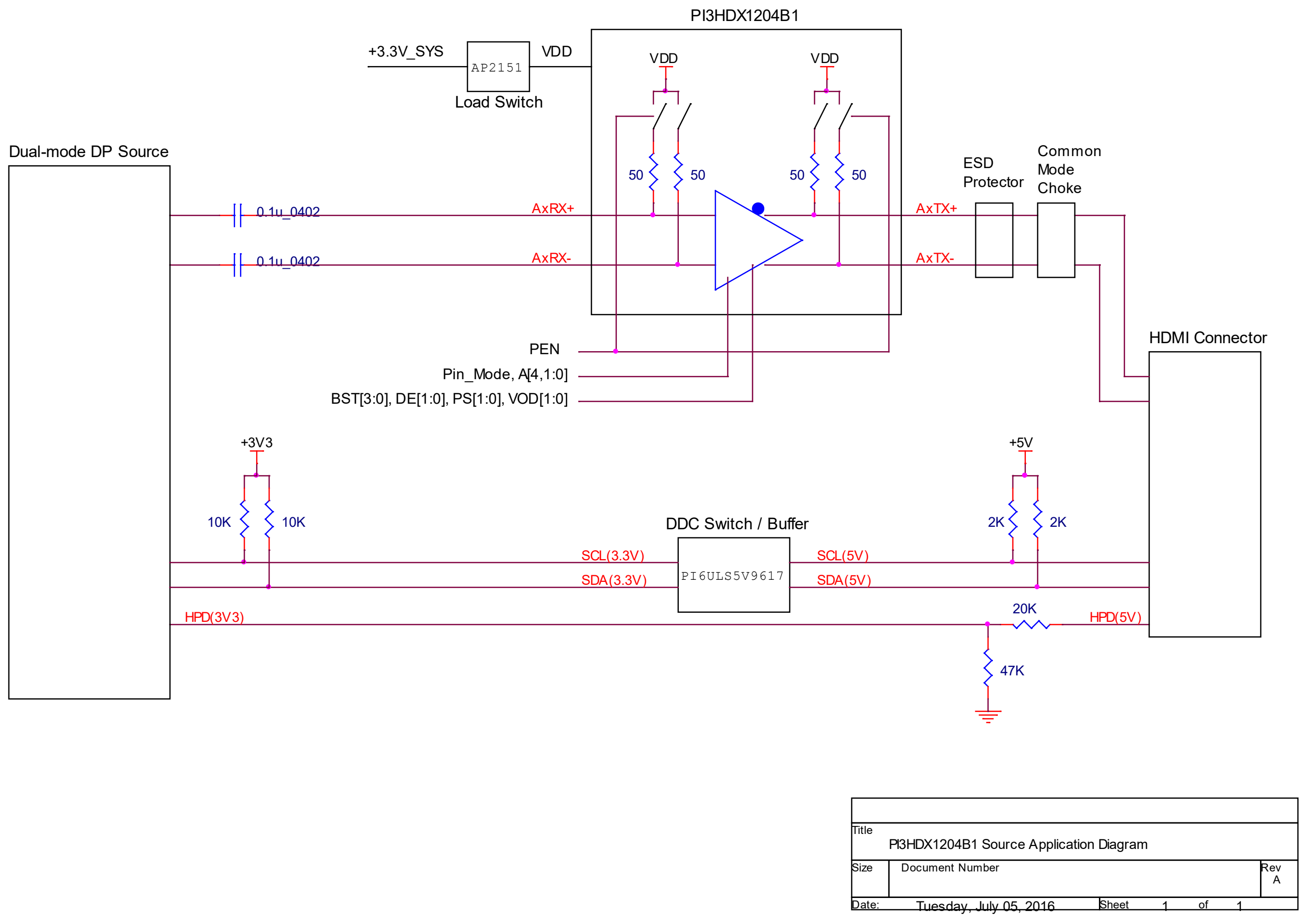


Figure 6-1 PI3HDX1204B1 Source Application Circuit

6.1.1 ESD Protectors on Output TMDS

As 8kV contact ESD is commonly required, ESD protectors are implemented at the output TMDS pins of PI3HDX1204B1 for source application. ESD8104 HDMI2.0 ESD protector can be considered to protect the 3.3V TMDS paths as its reverse working voltage is 3.3V.

6.1.2 Extra Component for Rise/fall Time Control

Per HDMI2.0 specification, rise/fall time of TMDS clock is kept at minimal 75ps while that of TMDS data is decreased to minimal 42.5ps if data rate is between 3.4Gbps and 6Gbps.

Table 7-3 Source TMDS Electrical - 6G – T_{RISE}, T_{FALL} Requirements

Reference	Requirement
[HDMI 2.0: Table 6-2] AC Characteristics for 3.4 Gbps < R_{bit} ≤ 6.0 Gbps at TP1	Rise/Fall time: Data (20% to 80%): ≥42.5 ps Rise/Fall time: Clock (20% to 80%): ≥75 ps

Figure 6-2 HDMI2.0 Trise/fall Requirement

PI3HDX1204B1 is designed to meet the rise/fall time of TMDS data. If output trace length is short, maybe 1" only, common-mode choke or external inductor can be considered for slowing down the rise/fall time for TMDS clock of PI3HDX1204B1.

6.1.3 Leakage Blockage for VOFF Test

When performing VOFF test specified in HDMI 1.4a Compliance Test Specification, each output TMDS of PI3HDX1204B1 will be pulled to 3.3V via an external 50kΩ resistor. In this case, current will pass through an internal ESD protector at the output TMDS pin of PI3HDX1204B1 and leakage will be found at VCC pin of PI3HDX1204B1.

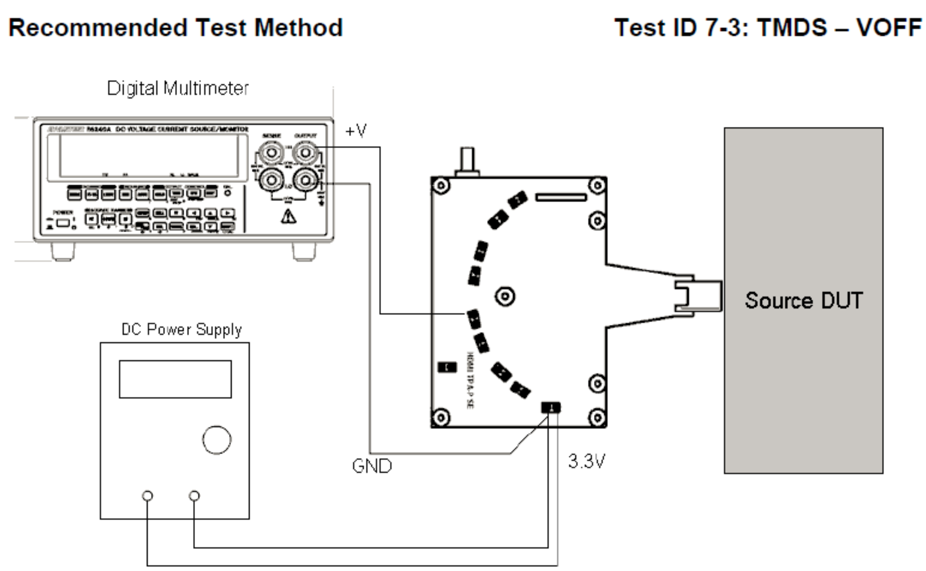


Figure 6-3 HDMI VOFF Test Setup

Test ID 7-3: TMDS – V_{OFF}

Reference	Requirement
[HDMI: Table 4-23] Source DC Characteristics at TP1	TMDS single-ended standby (off) output voltage, V_{OFF} must be within AVcc ±10mVolts.

Figure 6-4 HDMI VOFF Requirement

To avoid this leakage, AP2151A power switch can be employed between the main 3.3V supply on a system and the VCC power plane of PI3HDX1204B1. Below is an example borrowed from an evaluation board schematic.

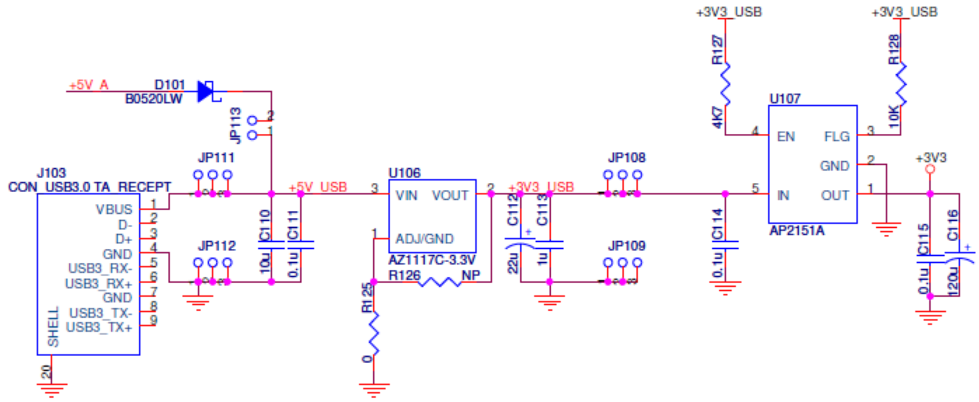


Figure 6-5 Power Distribution Switch Example

6.2 Sink Application

PI3HDX1204B1 can also be employed in a sink application as it offers a range of equalization setting.

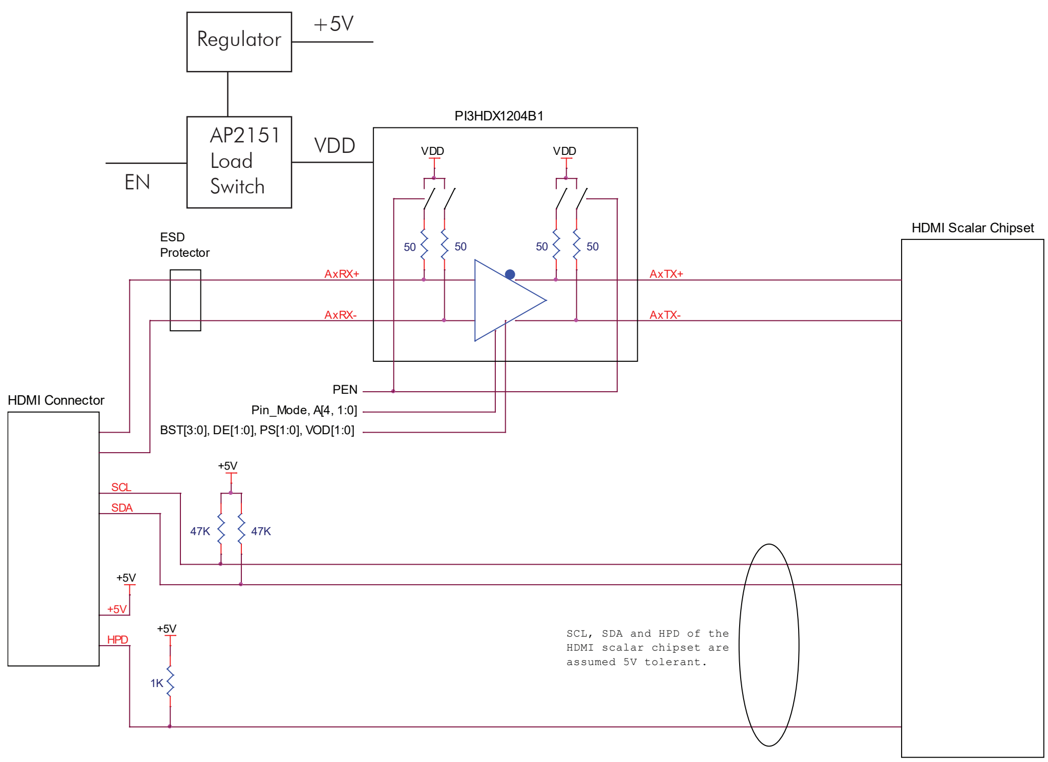
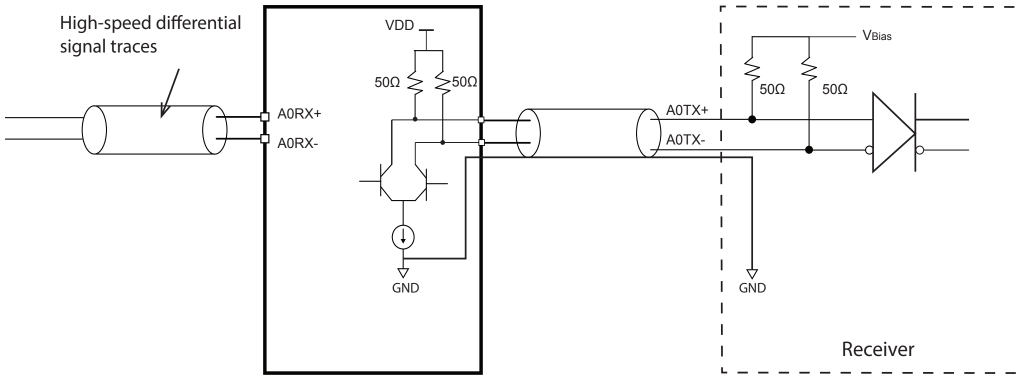


Figure 6-6 PI3HDX1204B1 Sink Application Circuit

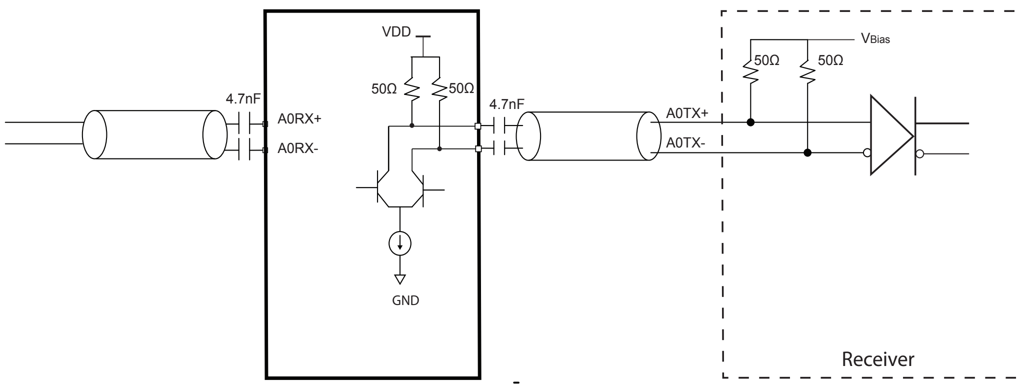
6.2.1 ESD Protectors on Output TMDS

ESD protector selection guidance for source and sink applications is the same.

6.3 DC/AC-coupled Application



DC-Coupled Differential Signaling Application Circuits



AC-Coupled Differential Signaling Application Circuits

Figure 6-7 DC/AC-coupled application diagram

6.4 Product Layout Guideline

6.4.1 AC Coupling Capacitor

Below is an example of placing AC coupling capacitors on high-speed channels

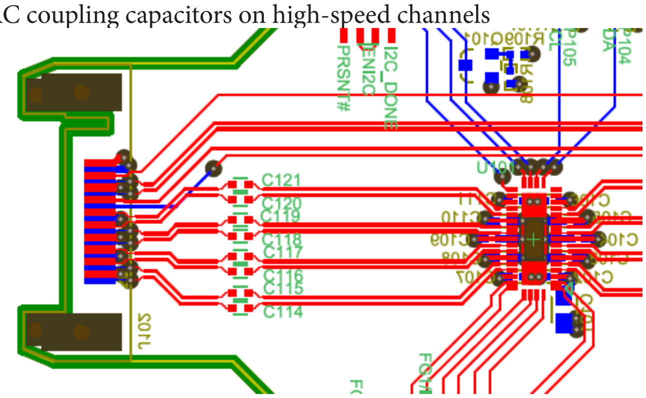


Figure 6-8 AC Coupling Capacitor Placement

6.4.2 Output Trace Length

To fulfill minimal 75ps rise/fall time requirement of TMDS clock, 1.5 – 4.5” TMDS trace length between PI3HDX1204B1 and HDMI connector for source application is recommended. This trace length varies with PCB trace width, characteristics of common-mode choke/ESD protector and connector quality. If trace width is 5 mil, 2.7 – 3.3” is recommended. Isolation space should be larger than 5 mil to minimize the crosstalk so thus jitter. Below is the PI3HDX1204B1 placement on its evaluation board.

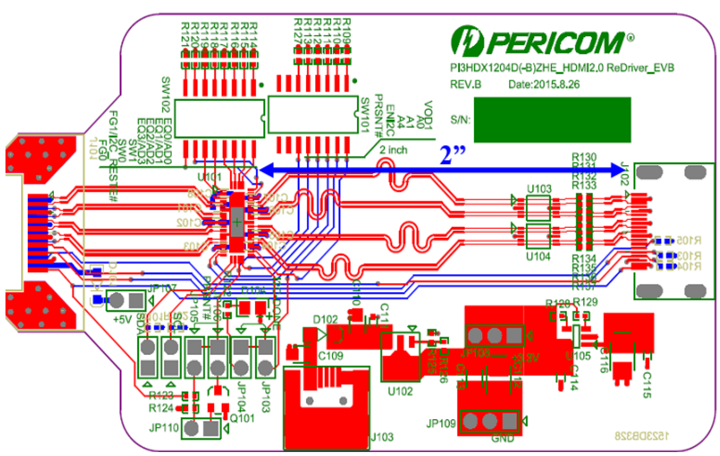


Figure 6-9 Source-side placement near to the HDMI connectors

6.4.3 Differential Impedance (TDR)

Layout guideline especially for high-speed transmission is critical. Please refer to PI3DPxxx_PI3HDxxx_Layout Guideline for detailed recommendations. Differential impedance test is required for both source and sink applications per HDMI 2.0 specification.

Table 7-17 Source TMDS Electrical - 6G – Differential Impedance Requirements

Reference	Requirement
[HDMI 2.0: Table 6-3] Source Impedance Characteristics for (3.4 Gbps < R_{bit} ≤ 6.0 Gbps) at TP1	Through Connection ImpedanceΔ: 100 Ω +/- 15%◊ ◊ single excursion is permitted out to a max/min of 100 Ω +/- 25% and of a duration less than 250 ps. Δ Impedance from TP1 to Source Termination Source Termination Impedance: 75 to 150 Ω

Figure 6-10 HDMI2.0 Differential Impedance Requirement for Source Application

Table 8-7 Sink TMDS Electrical - 6G – Differential Impedance Requirements

Reference	Requirement
[HDMI 2.0: Table 6-8] Sink Impedance Characteristics for (3.4 Gbps < R_{bit} ≤ 6.0 Gbps) at TP2	Through Connection ImpedanceΔ: 100 Ω +/- 15%◊ ◊ A single excursion is permitted out to a max/min of 100 Ω ±25% and of duration less than 250 ps. Δ Impedance from TP2 to Sink Termination Sink Termination Impedance: 90 Ω to 110 Ω

Figure 6-11 HDMI2.0 Differential Impedance Requirement for Sink Application

The PCB impedance immediately before and after an ESD protector must be adjusted to compensate the capacitance loading of the ESD protector. Below is an example designing RClampe0544M in PI3HDX1204B1 evaluation board. Trace impedances before and after the ESD protector are tuned to compensate the capacitance of RClamp0544M. Semtech's layout guideline is followed.

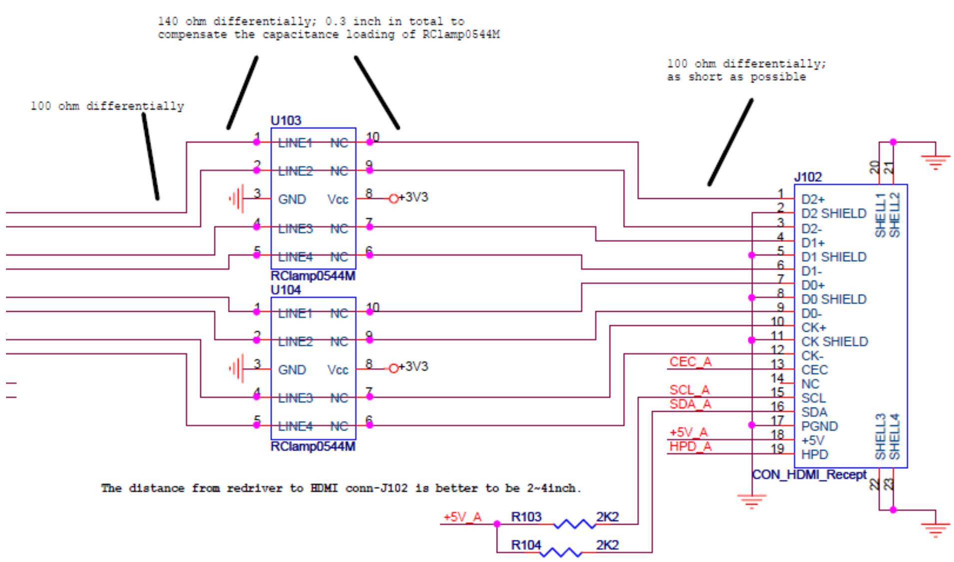


Figure 6-12 ESD Protector on PI3HDX1204B1 Source EVB

6.4.4 GND via on the thermal pad area

Several GND via are "MUST" required on thermal area. The via size is 12/24 mil. Below is the thermal pad via layout recommendation.

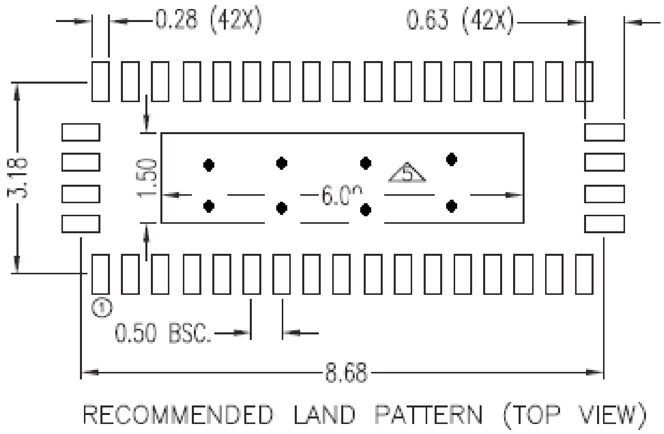


Figure 6-13 Recommended Land patterns

6.5 General Layout Guideline

As transmission data rate increases rapidly, any flaws and/or mis-matches on PCB layout are amplified in terms of signal integrity. Layout guideline for high-speed transmission is highlighted in this application note.

6.5.1 Power and Ground

To provide a clean power supply for Pericom high-speed device, few recommendations are listed below:

- Power (VDD) and ground (GND) pins should be connected to corresponding power planes of the printed circuit board directly without passing through any resistor.
- The thickness of the PCB dielectric layer should be minimized such that the VDD and GND planes create low inductance paths.
- One low-ESR 0.1uF decoupling capacitor should be mounted at each VDD pin or should supply bypassing for at most two VDD pins. Capacitors of smaller body size, i.e. 0402 package, is more preferable as the insertion loss is lower. The capacitor should be placed next to the VDD pin.
- One capacitor with capacitance in the range of 4.7uF to 10uF should be incorporated in the power supply decoupling design as well. It can be either tantalum or an ultra-low ESR ceramic.
- A ferrite bead for isolating the power supply for Pericom high-speed device from the power supplies for other parts on the printed circuit board should be implemented.
- Several thermal ground vias must be required on the thermal pad. 25-mil or less pad size and 14-mil or less finished hole are recommended.

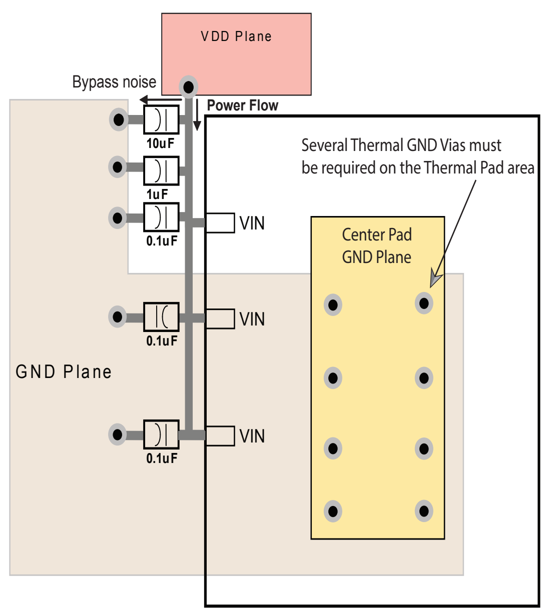
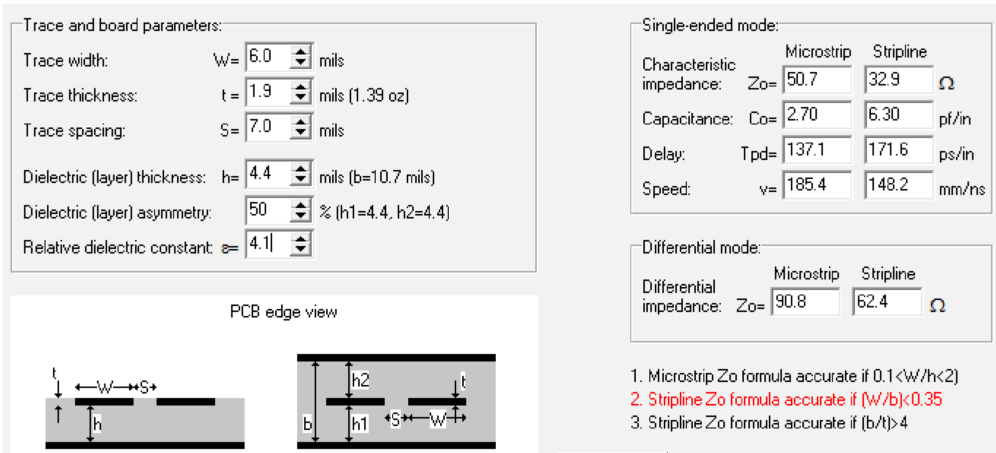


Figure 6-14 Decoupling Capacitor Placement Diagram

6.5.2 High-speed signal Routing

Well-designed layout is essential to prevent signal reflection:

- For 90Ω differential impedance, width-spacing-width micro-strip of 6-7-6 mils is recommended; for 100Ω differential impedance, width-spacing-width micro-strip of 5-7-5 mils is recommended.
- Differential impedance tolerance is targeted at ±15%.



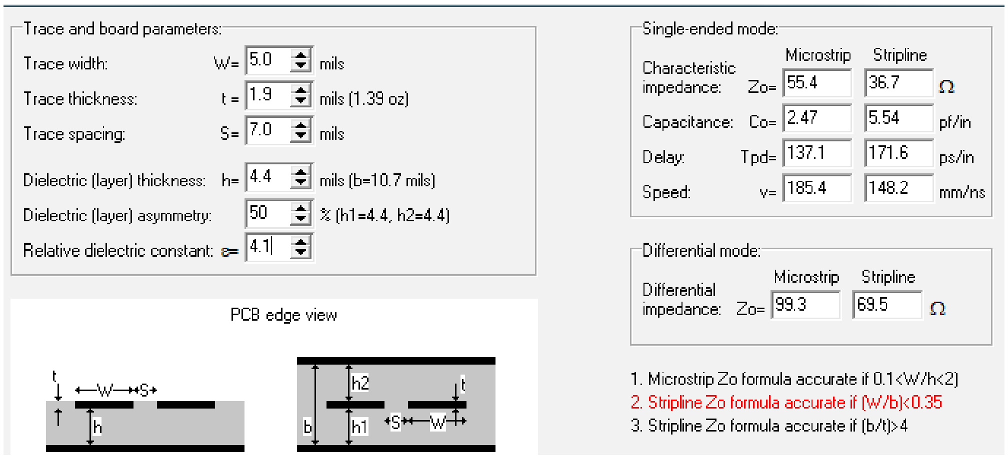


Figure 6-15 Trace Width and Clearance of Micro-strip and Strip-line

- For micro-strip, using 1/2oz Cu is fine. For strip-line in 6+ PCB layers, 1oz Cu is more preferable.

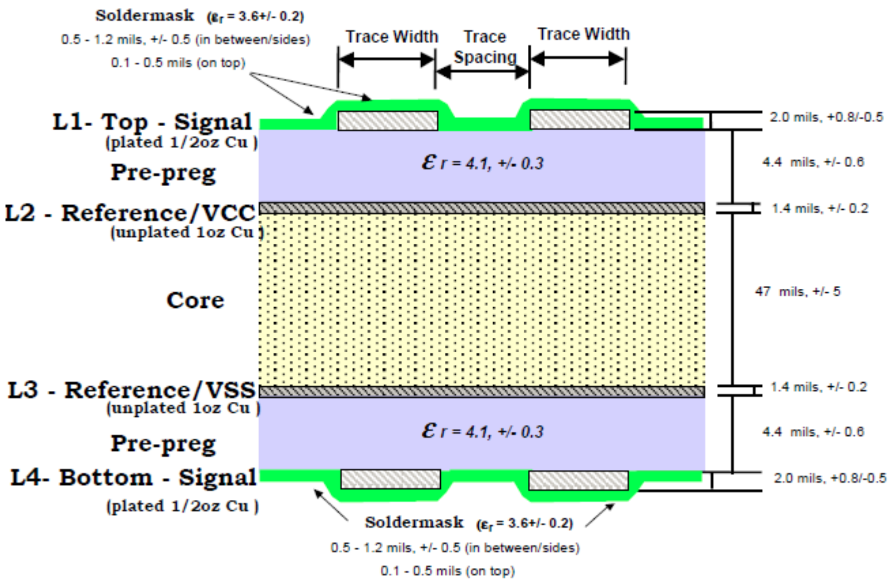


Figure 6-16 4-Layer PCB Stack-up Example

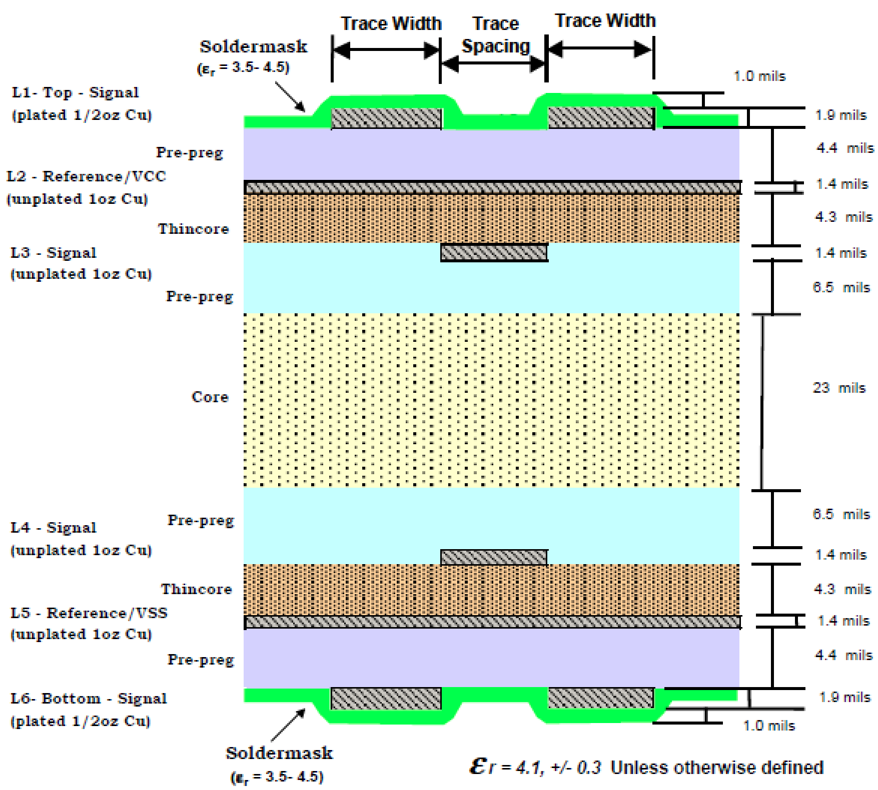


Figure 6-17 6-Layer PCB Stack-up Example

- Ground referencing is highly recommended. If unavoidable, stitching capacitors of 0.1uF should be placed when reference plane is changed.

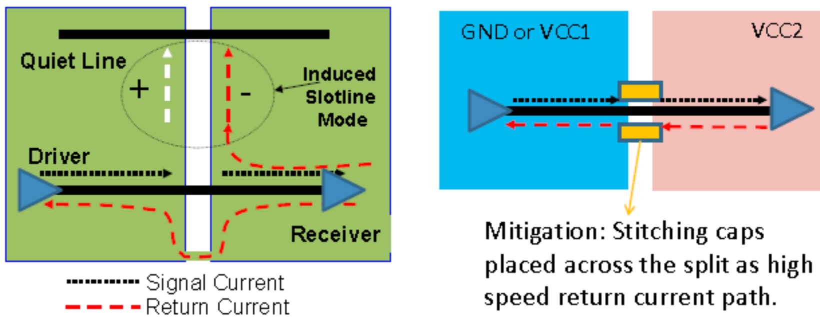


Figure 6-18 Stitching Capacitor Placement

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

- To keep the reference unchanged, stitching vias must be used when changing layers.
- Differential pair should maintain symmetrical routing whenever possible. The intra-pair skew of micro-strip should be less than 5 mils.

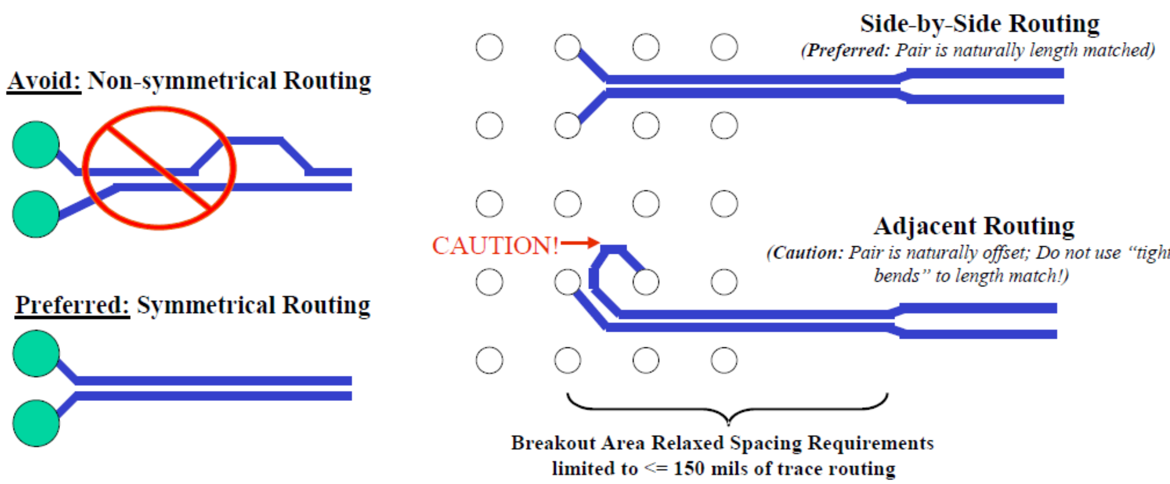


Figure 6-19 Layout Guidance of Matched Differential Pair

- For minimal crosstalk, inter-pair spacing between two differential micro-strip pairs should be at least 20 mils or 4 times the dielectric thickness of the PCB.
- Wider trace width of each differential pair is recommended in order to minimize the loss, especially for long routing. More consistent PCB impedance can be achieved by a PCB vendor if trace is wider.
- Differential signals should be routed away from noise sources and other switching signals on the printed circuit board.
- To minimize signal loss and jitter, tight bend is not recommended. All angles α should be at least 135 degrees. The inner air gap A should be at least 4 times the dielectric thickness of the PCB.

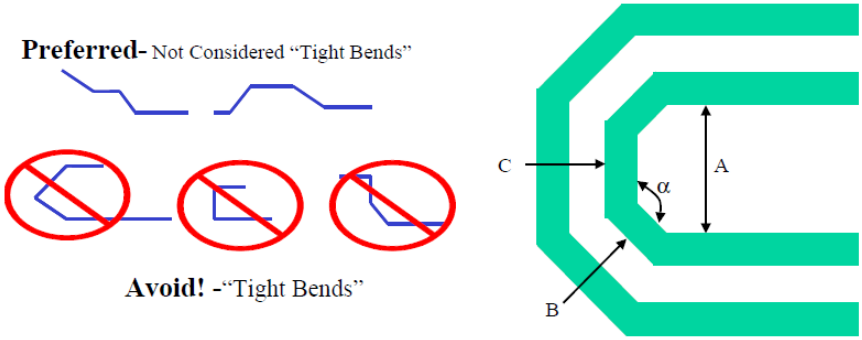


Figure 6-20 Layout Guidance of Bends

- Stub creation should be avoided when placing shunt components on a differential pair.

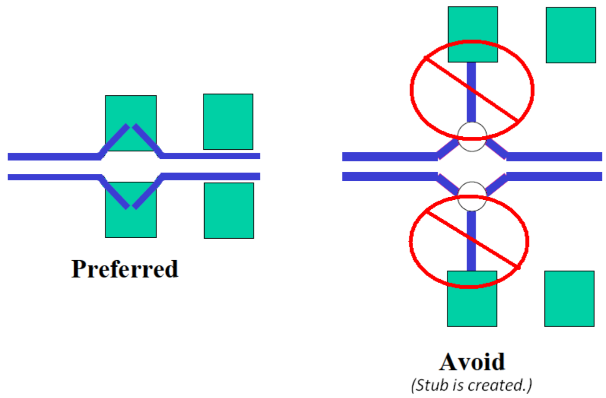


Figure 6-21 Layout Guidance of Shunt Component

- Placement of series components on a differential pair should be symmetrical.

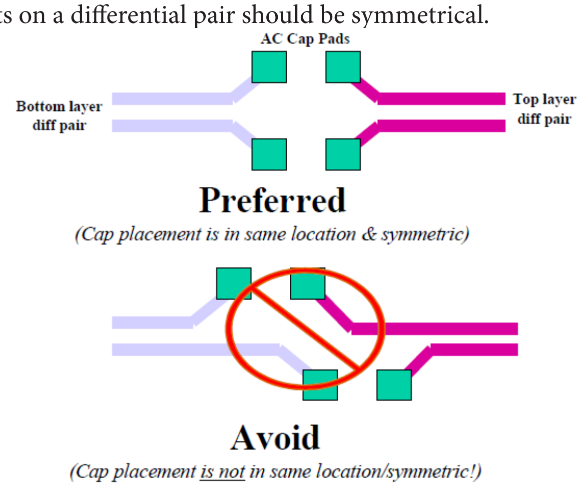


Figure 6-22 Layout Guidance of Series Component

- Stitching vias or test points must be used sparingly and placed symmetrically on a differential pair.

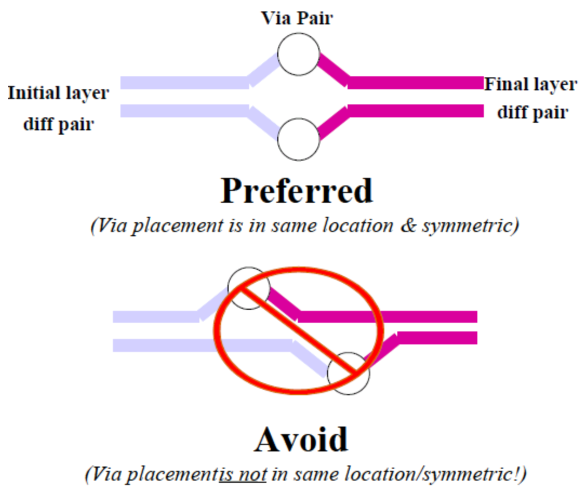


Figure 6-23 Layout Guidance of Stitching Via

6.6 CTS Test Report

6.6.1 HDMI 2.0 Compliance Test Set-up

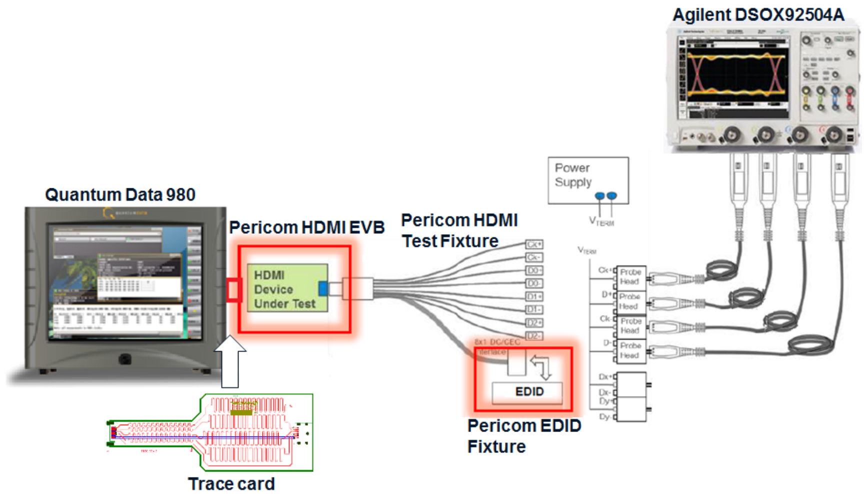


Figure 6-24 HDMI 2.0 CTS test setup

Note: Application Trace Card Information for CTS test

HDMI FR4 trace	0 in	6 in	12 in	18 in	24 in	30 in	36 in
Insertion loss @ 6Gbps	-5.91 dB	-9.75 dB	-10.47 dB	-13.05 dB	-15.87 dB	-16.97 dB	-21.20 dB

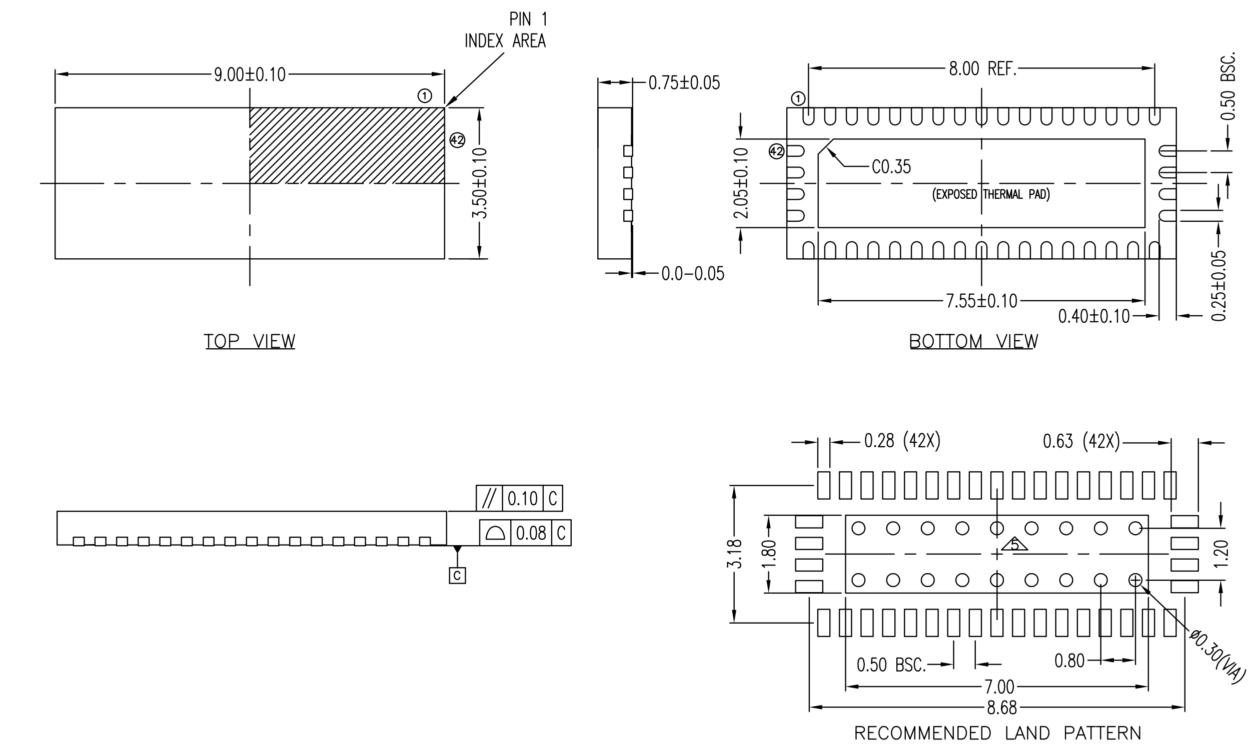
6.6.2 HDMI 2.0 Compliance Report

Test Summary

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-9 : Source Clock Jitter	CK	Clock Jitter < 0.25*Tbit;	0.061*Tbit	Pass
2	7-10 : Source Eye Diagram	CK - D0	Data Jitter < 0.3*Tbit;	0.06*Tbit	Pass
3	7-10 : Source Eye Diagram	CK - D1	Data Jitter < 0.3*Tbit;	0.07*Tbit	Pass
4	7-10 : Source Eye Diagram	CK - D2	Data Jitter < 0.3*Tbit;	0.07*Tbit	Pass
5	7-6 : Source Inter-Pair Skew	D0 - D1	Skew < 0.2*TPixel;	0*TPixel	Pass
6	7-6 : Source Inter-Pair Skew	D1 - D2	Skew < 0.2*TPixel;	0.006*TPixel	Pass
7	7-6 : Source Inter-Pair Skew	D2 - D0	Skew < 0.2*TPixel;	0.006*TPixel	Pass
8	7-4 : Source Rise Time	CK	75.00ps < TRISE;	171.37ps	Pass
9	7-4 : Source Rise Time	D0	75.00ps < TRISE;	149.40ps	Pass
10	7-4 : Source Rise Time	D1	75.00ps < TRISE;	145.49ps	Pass
11	7-4 : Source Rise Time	D2	75.00ps < TRISE;	150.62ps	Pass
12	7-4 : Source Fall Time	CK	75.00ps < TFALL;	170.68ps	Pass
13	7-4 : Source Fall Time	D0	75.00ps < TFALL;	148.94ps	Pass
14	7-4 : Source Fall Time	D1	75.00ps < TFALL;	142.33ps	Pass
15	7-4 : Source Fall Time	D2	75.00ps < TFALL;	144.95ps	Pass
16	7-8 : Max Duty Cycle	CK	Max Duty Cycle < 60.0%;	50.79%	Pass
17	7-8 : Min Duty Cycle	CK	40.0% < Min Duty Cycle;	49.6%	Pass
18	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	CK+	2.700V < VL < 2.900V;	2.8600V	Pass
19	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D0+	2.700V < VL < 2.900V;	2.8475V	Pass
20	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	CK-	2.700V < VL < 2.900V;	2.8425V	Pass
21	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D0-	2.700V < VL < 2.900V;	2.8475V	Pass
22	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D1+	2.700V < VL < 2.900V;	2.8250V	Pass
23	7-2 : Source Low Amplitude +(Supported Sink <= 165MHz)	D2+	2.700V < VL < 2.900V;	2.8650V	Pass
24	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D1-	2.700V < VL < 2.900V;	2.8275V	Pass
25	7-2 : Source Low Amplitude -(Supported Sink <= 165MHz)	D2-	2.700V < VL < 2.900V;	2.8650V	Pass
26	7-7 : Source Intra-Pair Skew	CK	Skew < 0.15*Tbit;	0.015*Tbit	Pass
27	7-7 : Source Intra-Pair Skew	D0	Skew < 0.15*Tbit;	0.021*Tbit	Pass
28	7-7 : Source Intra-Pair Skew	D1	Skew < 0.15*Tbit;	0.007*Tbit	Pass
29	7-7 : Source Intra-Pair Skew	D2	Skew < 0.15*Tbit;	0.051*Tbit	Pass

7. Mechanical/Packaging Information

7.1 Mechanical



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL IS RECOMMENDED).

DIODES INCORPORATED / PERICOM ENABLING SERIAL CONNECTIVITY	DATE: 09/05/16
DESCRIPTION: 42-Contact, Very Thin Quad Flat No-Lead (TQFN)	
PACKAGE CODE: ZH (ZH42)	
DOCUMENT CONTROL #: PD-2035(S)	REVISION: F

Note:
(1) For latest package info, please check: http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/

7.2 Part Marking Information

Our standard product mark follows our standard part number ordering information, except for those products with a speed letter code. The speed letter code mark is placed after the package code letter, rather than after the device number as it is ordered. After electrical test screening and speed binning has been completed, we then perform an “add mark” operation which places the speed code letter at the end of the complete part number.

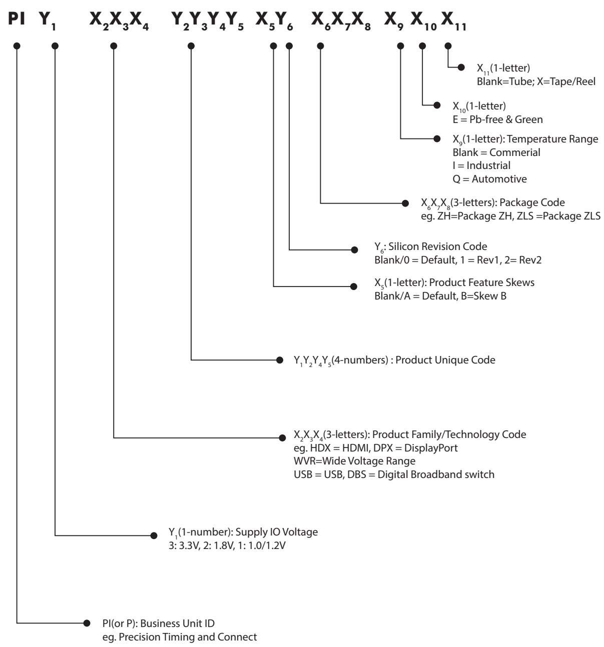


Figure 7-1 Part marketing information

7.3 Tape & Reel Materials and Design

Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene plus Carbon material (or equivalent). The surface resistivity is 10^6Ohm/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See Figures 3 and 4 for carrier tape dimensions.

Cover Tape

Cover tape is made of Anti-static Transparent Polyester film.The surface resistivity is 10^7Ohm/Sq. Minimum to 10^{11}Ohm sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20 to 80gm (2N to 0.8N).

Reel

The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel, (Figure 4) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 10^7Ohm/sq. minimum to 10^{11}Ohm/sq. max.

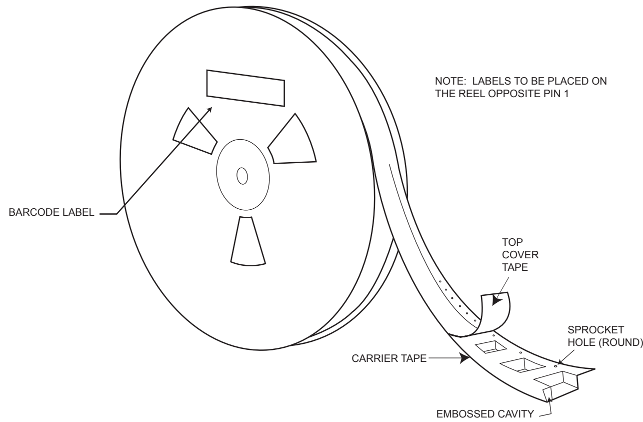


Figure 7-2 Tape & Reel label information

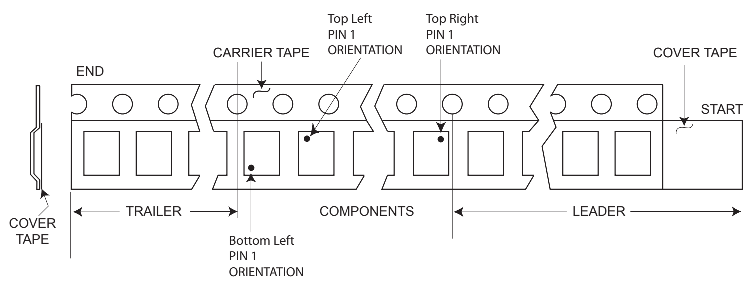


Figure 7-3 Tape leader and trailer pin 1 orientation

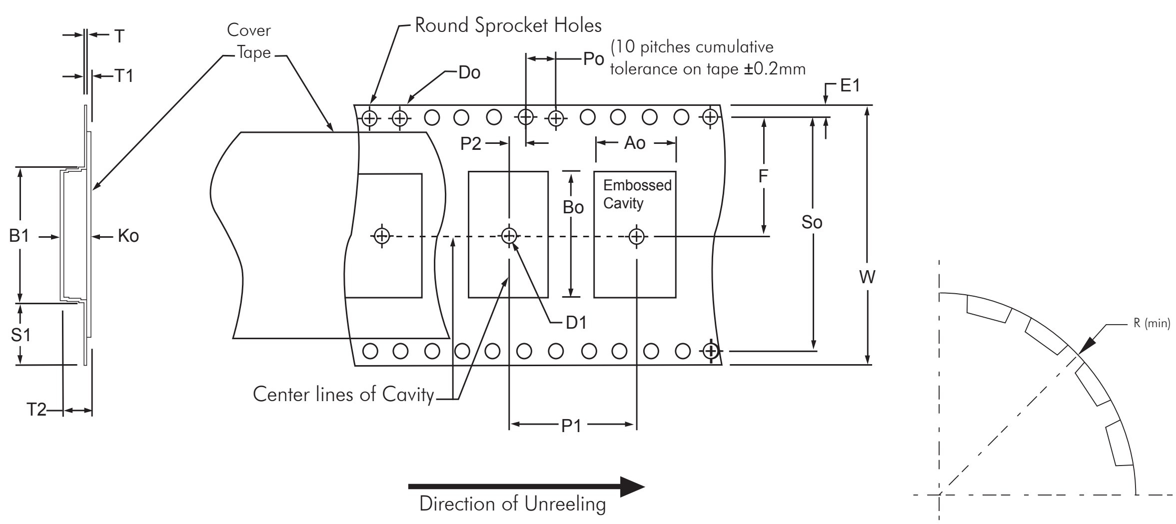


Figure 7-4 Standard embossed carrier tape dimension

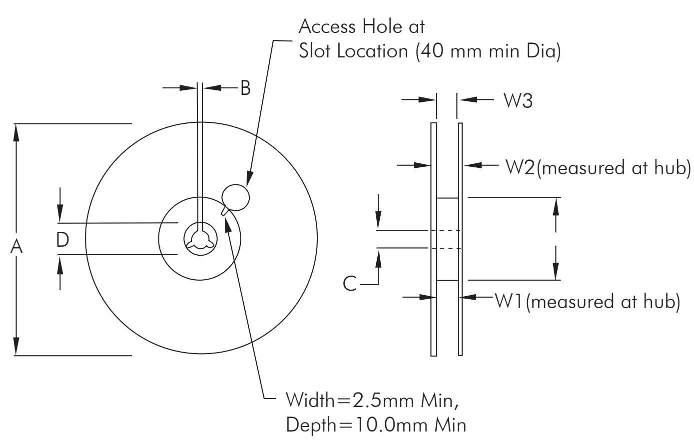
Constant Dimensions

Tape Size	D0	D1 (Min)	E1	P0	P2	R (See Note 2)	S1 (Min)	T (Max)	T1 (Max)
8mm	1.5 +0.1 -0.0	1.0	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	25	0.6	0.6	0.1
12mm		1.5				30			
16mm					2.0 ± 0.1				
24mm									
32mm		2.0				50	N/A (See Note 3)		
44mm					2.0 ± 0.15				

Variable Dimensions

Tape Size	P_1	B_1 (Max)	E_2 (Min)	F	So	T_2 (Max.)	W (Max)	A_0, B_0, & K_0
8mm	Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information) or visit www.pericom.com/pdf/gen/tapereel.pdf	4.35	6.25	3.5 ± 0.05	N/A (see note 4)	2.5	8.3	See Note 1
12mm		8.2	10.25	5.5 ± 0.05		6.5	12.3	
16mm		12.1	14.25	7.5 ± 0.1		8.0	16.3	
24mm		20.1	22.25	11.5 ± 0.1		12.0	24.3	
32mm		23.0	N/A	14.2 ± 0.1	28.4± 0.1		32.3	
44mm		35.0	N/A	20.2 ± 0.15	40.4 ± 0.1	16.0	44.3	

NOTES:
(1) A0, B0, and K0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16,24,32, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16 through 44mm.
(2) Tape and components will pass around reel with radius "R" without damage.
(3) S1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where Do≥S1.
(4) So does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.



Reel dimensions by tape size

Tape Size	A	N (Min) (1)	W1	W2(Max)	W3	B (Min)	C	D (Min)
8mm	178±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	8.4 +1.5/-0.0 mm	14.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm	178±2.0mm or 330±2.0mm	60 ±2.0mm or 100±2.0mm	12.4 +2.0/-0.0 mm	18.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
16mm	330±2.0mm	100 ±2.0mm	16.4 +2.0/-0.0 mm	22.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
24mm	330±2.0mm	100 ±2.0mm	24.4 +2.0/-0.0 mm	30.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
32mm	330±2.0mm	100 ±2.0mm	32.4 +2.0/-0.0 mm	38.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
44mm	330±2.0mm	100 ±2.0mm	44.4 +2.0/-0.0 mm	50.4 mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm

NOTE:
(1) If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

7.4 Products Information

Part Number	Product Description
PI3DPX1203	DisplayPort 1.3 Linear ReDriver for Source/Sink/Cable Application
PI3WVR12412	Wide Voltage Range 1:2 DP 1.2 & HDMI 2.0 Passive Switch
PI3WVR31310	Wide Voltage Range 1:3 DP 1.2 & HDMI 2.0 Passive Switch
PI3HDX414	HDMI 1.4b Splitter 1:4 with Signal Conditioning for 3.4Gbps Application
PI3HDX412BD	HDMI 1.4b Splitter 1:2 with Signal Conditioning for 3.4Gbps Application
PI3HDX511D/E	Ultra Low Power HDMI 1.4b ReDriver and DP++ Level Shifter
PI3HDX511F	High EQ HDMI 1.4b ReDriver and DP++ Level Shifter for Sink/Source Application
PI3EQXDP1201	DisplayPort 1.2 ReDriver with built-in AUX Listener
PI3HDX621	HDMI 1.4 2:1 Active Switch with built-in ARC and Fast Switching support
PI3HDMI336	Active HDMI 3:1 Switch/Re-driver with I2C control and ARC Transmitter

7.5 Product Status Definition

Datasheet Identification	Product Status	Definition
Advanced Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Diodes Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Diodes Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Diodes Semiconductor. The datasheet is for reference information only.