A Product Line of
Diodes Incorporated

PI3HDX612

6Gbps HDMI 2.0 1:2 Signal Duplicator

Description

The DIODES PI3HDX612 active-drive Signal Duplicator solution is targeted for high-resolution video networks that are based on HDMI™ 2.0 standards signal processing.

The PI3HDX612 is an active single-channel to two-channel Signal Duplicator. The device drives differential signals to multiple video display units. Depending on the mode select pin, the PI3HDX612 provides controllable equalizer, flat gain and output swing linearity that can be manipulated through pin control or I^{2}C control.

The maximum HDMI™ data rate of 6Gbps produces a 4K@60Hz resolution or 2K@144Hz, required for 4K HDTV, PC graphics products and other peripheral device. For PC graphics application, the device sits at the driver's side and fans out differential signals to multiple display units including PC LCD monitors, projectors, and TVs. The CTLE equalizers are implemented at the inputs of the ReDriver to reduce the ISI jitters and compensate channel loss. The PI3HDX612 ensures the transmittal of high bandwidth video streams from video sources to the end-display units.

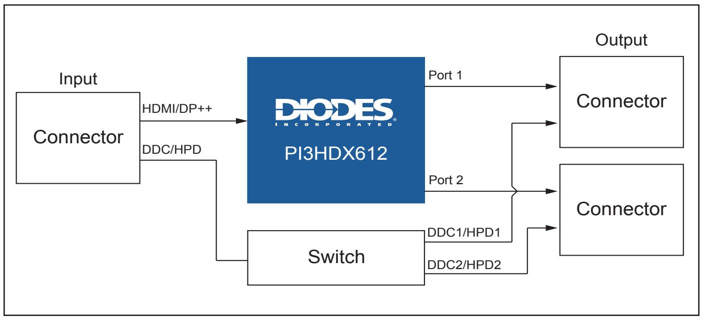
Features

- 1-to-2 Active Signal Duplicator for 4-Lane HDMI 2.0 Operation
- Data Rate Supports Up to 6Gbps and Supports 4K2K Pixel Resolution
- Quad-Level Equalizer Gain Value Selection Controlled By Pin Strap or I^{2}C Mode Programming
- Quad-Level Flat Gain and Output Swing Linearity Selection Controlled By Pin Strap or I^{2}C Mode Programming
- ESD Protection on I/O Pins: 2KV HBM
- Single Power Supply: 3.3V
- Temperature Support: -40°C to +70°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 40-pin TQFN, 3 x 6 mm (0.4 mm pitch) (ZLD)

Application(s)

- Display Peripheral Boxes
- Digital Signage Displays
- Multi-Screen Splicing

Application Diagram



Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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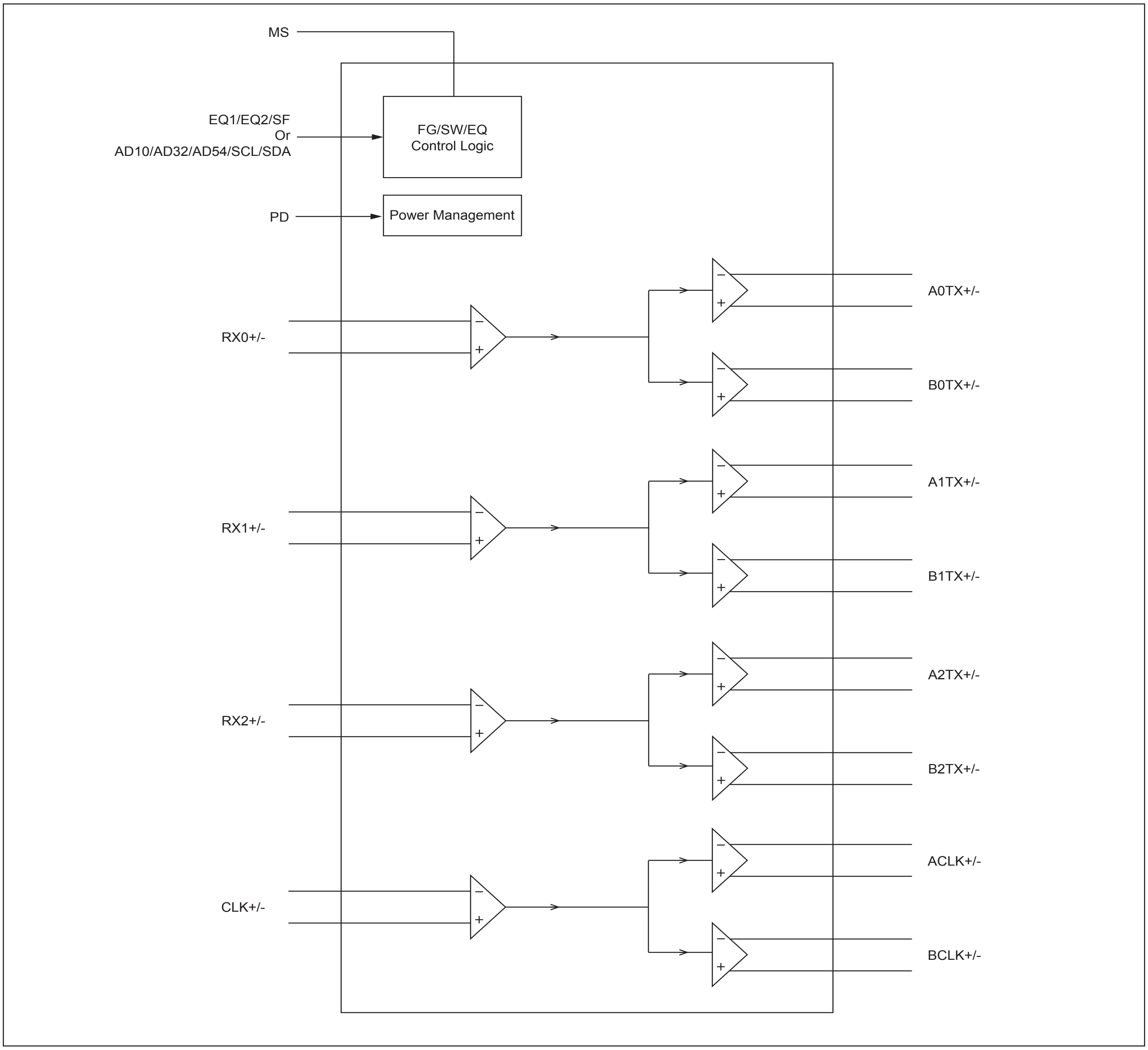
Block Diagram



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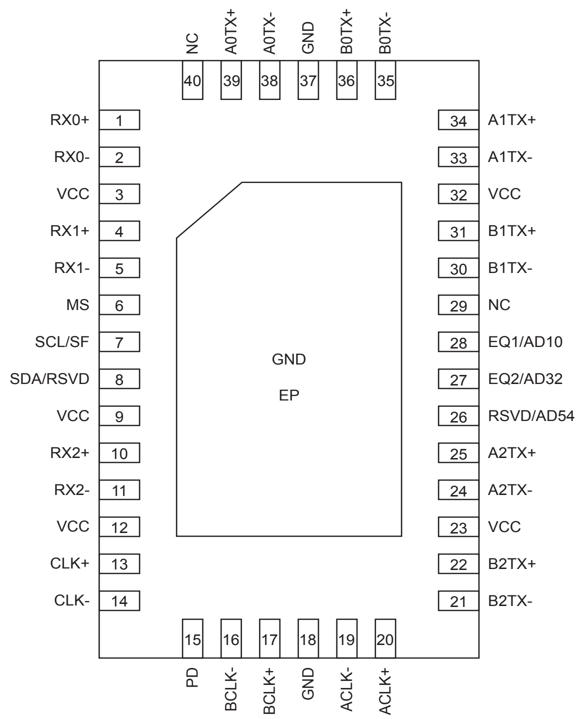
Pin Configuration (Top View)



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Pin Configuration (Top View)

Pin #	Pin Name	Type	Description
Data Signals			
1, 2	RX0+, RX0-	I	CML inputs for channel 0 with internal 50Ω to VCC or HIZ.
39, 38 36, 35	A0TX+, A0TX- B0TX+, B0TX-	O	CML outputs for channel A0/B0 with internal 50Ω pullup or HIZ.
4, 5	RX1+, RX1-	I	CML inputs for channel 1 with internal 50Ω to VCC or HIZ.
34, 33 31, 30	A1TX+, A1TX- B1TX+, B1TX-	O	CML outputs for channel A1/B1 with internal 50Ω pullup or HIZ.
10, 11	RX2+, RX2-	I	CML inputs for channel 2 with internal 50Ω to VCC or HIZ.
25, 24 22, 21	A2TX+, A2TX- B2TX+, B2TX-	O	CML outputs for channel A2/B2 with internal 50Ω pullup or HIZ.
13, 14	CLK+, CLK-	I	CML inputs for CLK channel with internal 50Ω to VCC or HIZ.
20, 19 17, 16	ACLK+, ACLK- BCLK+, BCLK-	O	CML outputs for CLKA/B channel with internal 50Ω pullup or HIZ.
Control Pins			
28, 27, 26	EQ1, EQ2, RSVD	I	4-Level input pins with internal 100KΩ pullup and 200KΩ pulldown resistor. Sets the amount of equalizer boost on A & B channel. Reserved pin must tie to ground.
	AD10, AD32, AD54	I	4-Level input pins with internal 100KΩ pullup and 200KΩ pulldown resistor. Sets the I^2C slave address.
7, 8	SF, RSVD	I	4-Level input pins with internal 100KΩ pullup and 200KΩ pulldown resistor. Sets the output swing and flat gain level on A & B channel. Reserved pin must tie to ground.
	SCL, SDA	I	I^2C clock input and data input.
6	MS	I	Input with internal 300KΩ pullup resistor. Pin mode enable pin Tie High = Pin mode Tie Low = Register access I^2C slave mode
29, 40	NC		Not Connected
15	PD	I	Input with internal 300KΩ pullup resistor. When High, the device is put in Power Down Mode. When Low, the device is Enable and in Normal Operation.
Power Pins			
3, 9, 12, 23, 32	VCC	PWR	3.3V supply voltage.
18, 37, EP	GND	PWR	Exposed pad. Supply ground.

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Functional Description & Circuit Block Description

Power Enable Function

When PD is set to high, the IC goes into power down mode, both input and output termination set to high impedance. Individual channel enabling is done through the I^2C register programming.

EQ Setting in Pin Mode and I^2C Mode

Table 1. EQ1/EQ2 are the Selection Pins for the Equalization Setting

Equalizer Setting (dB)					
EQ1	EQ2	I^2C EQ<2:0>	@1.25GHz	@1.7GHz	@3GHz
0	0	000	0.5	0.9	2.5
0	F	001	0.6	1.1	3.1
R	0	010	2.0	2.5	4.1
R	F	011	2.2	2.9	4.9
F	0	100	3.1	3.8	5.9
F	F	101	3.4	4.2	6.7
1	0	110	4.3	5.1	7.7
1	F	111	4.8	5.8	8.9

Swing and Flat Gain Setting

Table 2. Swing and Flat Gain Setting for SF

SF	Swing (mVp-p)	Flat Gain (dB)
0	1000	-3.5
R	1000	-0.5
F	1200	-3.5
1	1200	-0.5

Table 3. Swing Settings in I^2C Mode

SW1	SW0	Swing (mVp-p)
0	0	800
0	1	1000 (default)
1	0	1100
1	1	1200

Table 4. Flat Gain Setting in I^2C Mode

FG1	FG0	Flat Gain (dB)
0	0	-3.5
0	1	-2
1	0	-0.5 (default)
1	1	1

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Table 5. I²C Address Settings

AD54	AD5	AD4
0	0	0
R	0	1
F	1	0
1	1	1

AD32	AD3	AD2
0	0	0
R	0	1
F	1	0
1	1	1

AD10	AD1	AD0
0	0	0
R	0	1
F	1	0
1	1	1

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I²C Programming

Address Assignment							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
1	AD5	AD4	AD3	AD2	AD1	AD0	1=R, 0=W

BYTE 0					
Bit	**Type**	**Power up Condition**	**Field**	**Control Affected**	**Comment**
7	R	0		Reserved	
6	R	0		Reserved	
5	R	1		Reserved	
4	R	1		Reserved	
3	R	0		Rev. ID = 0x0	
2	R	0			
1	R	0			
0	R	0			

BYTE 1					
Bit	**Type**	**Power up Condition**	**Field**	**Control Affected**	**Comment**
7	R	0		Reserved	Reserved
6	R	0		Reserved	
5	R	0		Reserved	
4	R	0		Reserved	
3	R	0		Reserved	
2	R	0		Reserved	
1	R	0		Reserved	
0	R	0		Reserved	

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BYTE 2					
Bit	**Type**	**Power up Condition**	**Field**	**Control Affected**	**Comment**
7	R/W	0		Channel 3 Power down	1 = Power down
6	R/W	0		Channel 2 Power down	
5	R/W	0		Channel 1 Power down	
4	R/W	0		Channel 0 Power down	
3	R/W	1		Reserved	
2	R/W	1		Reserved	
1	R/W	0		Reserved	
0	R/W	1		Reserved	

BYTE 3					
Bit	**Type**	**Power up Condition**	**Field**	**Control Affected**	**Comment**
7	R/W	0	Channel 0 configuration	Reserved	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	1		FG1	Flat Gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	1		SW0	

BYTE 4					
Bit	**Type**	**Power up Condition**	**Field**	**Control Affected**	**Comment**
7	R/W	0	Channel 1 configuration	Reserved	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	1		FG1	Flat Gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	1		SW0	

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BYTE 5					
Bit	**Type**	**Power up Condition**	**Field**	**Control Affected**	**Comment**
7	R/W	0	Channel 2 configuration	Reserved	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	1		FG1	Flat Gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	1		SW0	

BYTE 6					
Bit	**Type**	**Power up Condition**	**Field**	**Control Affected**	**Comment**
7	R/W	0	Channel 3 configuration	Reserved	Equalizer
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	1		FG1	Flat Gain
2	R/W	0		FG0	
1	R/W	0		SW1	Swing
0	R/W	1		SW0	

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I²C Operation

The integrated I²C interface operates as slave device when 'MS" set to logic low. Standard mode (100Kbps) is supported with 7-bit addressing. The data byte format is 8-bit bytes and supports the format of indexing to be compatible with other bus devices. In the Slave mode (MS = LOW), the device supports Read/Write. The bytes must be accessed in sequential order from the lowest to the highest byte with the ability to stop after any complete byte has been transferred.

Address bits A5 to A0 are configurable by hardware strap pin to support multiple chips environment.

Transferring Data

Every byte put on the SDA line must be 8-bits long. Each byte must be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see the I²C Data Transfer diagram). The device never holds the clock line SCL to low to force the master into a wait state.

Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, the device pulls down the SDA line during the acknowledge clock pulse, so it remains stable LOW during the HIGH period of this clock pulse as indicated in the I²C Data Transfer diagram. The device generates an acknowledge after each byte has been received.

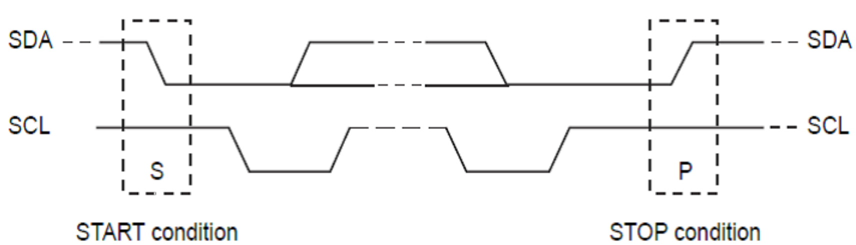
Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, the device watches the next byte of information for a match with its address setting. When a match is found it responds with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit except for the last byte of a read cycle, which ends with a stop bit. For a write cycle, the first data byte following the address byte is an index byte that is used by the device. Data is transferred with the most significant bit (MSB) first.

I²C Data Transfer

Start & Stop Conditions

A HIGH-to-LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW-to-HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below.



I²C START and STOP conditions.

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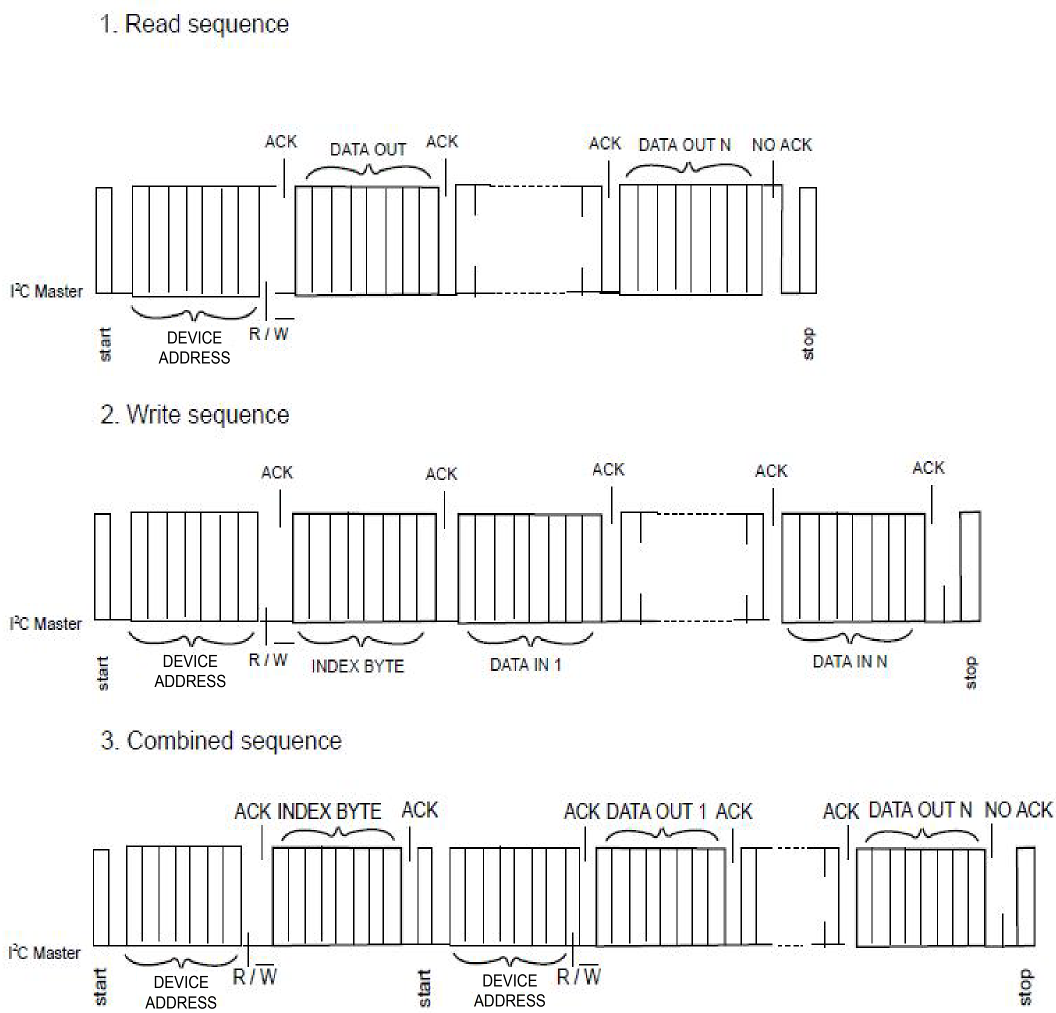
I²C Data Transfer



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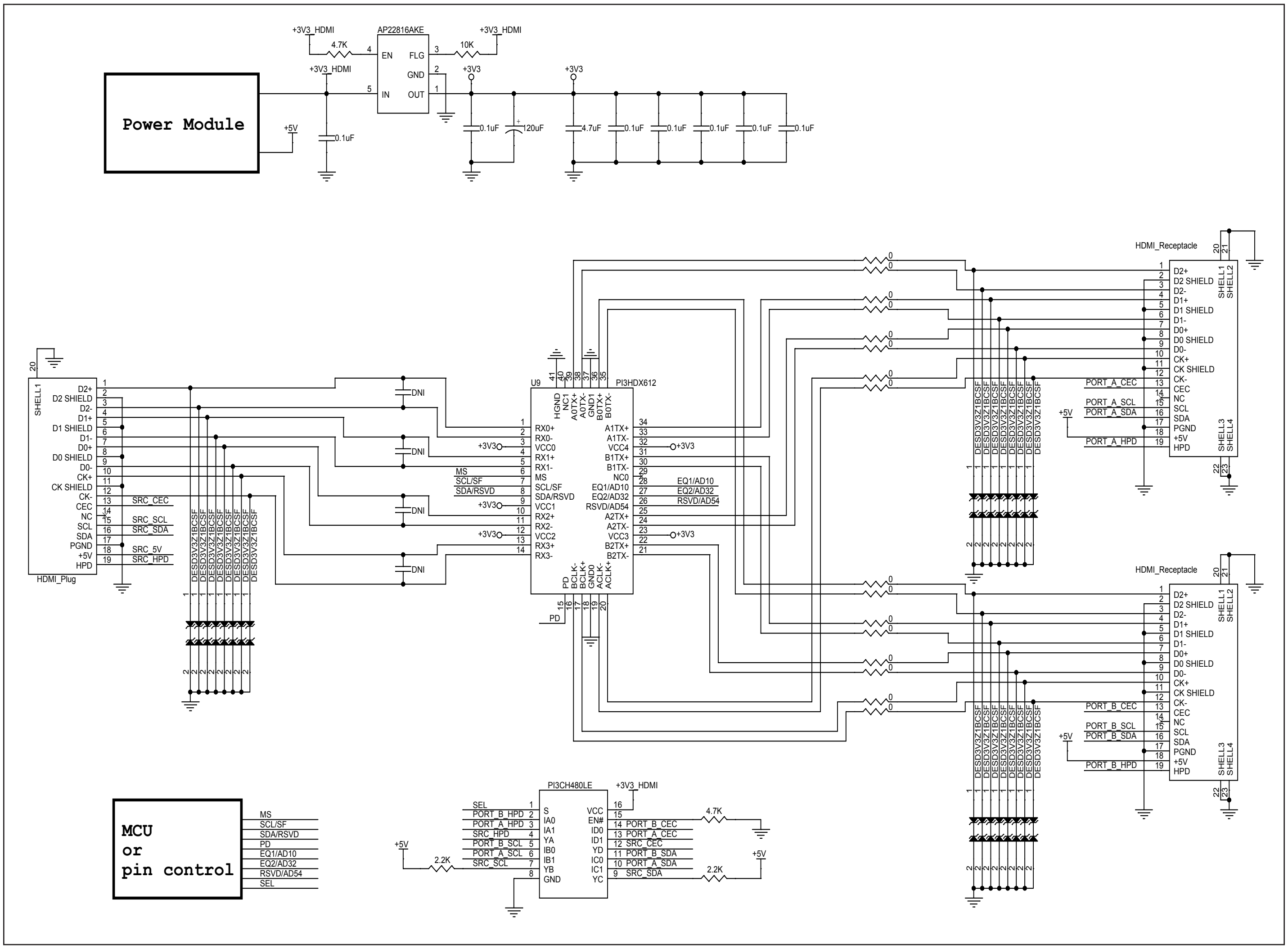
Application Schematics



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Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5V to +3.8V
DC SIG Voltage	−0.5V to V_{CC}+0.5V
ESD, HBM	−2kV to +2kV

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Thermal Information

Symbol	Parameter	40-pin TQFN (ZLD) Package	Units
Theta JA	Junction to Ambient Thermal Resistance	17.91	°C/W

Rommended Operating Condidtions

Symbol	Parameter	Min.	Typ.	Max.	Units
VCC	Supply Voltage	3.0	3.3	3.6	V
TA	Ambient Temperature	−40		+70	°C

Electrical Characteristics - LVCMOS I/O DC Specifications

V_{CC} = 3.3 ± 0.3V, T_A = -40°C to 70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC Input Logic High		0.44 VCC		VCC + 0.3	V
V_{IL}	DC Input Logic Low		-0.3		0.1 VCC	V
4-Level Control Pins						
V_{IH}	DC Input Logic “High”		0.92×VCC	VCC		V
V_{IF}	DC Input Logic “Float”		0.59×VCC	0.67×VCC	0.75×VCC	V
V_{IR}	DC Input Logic “With Rext to GND”		0.25×VCC	0.33×VCC	0.41×VCC	V
V_{IL}	DC Input Logic “Low”			GND	0.08×VCC	V
I_{IH}	Input High Current				50	µA
I_{IL}	Input Low Current		-50			µA
Rext	External Resistance Connects to GND (±5%)		64.6	68	71.4	kΩ

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Electrical Characteristics - SDA and SCL I/O for I²C-bus

V_{CC} = 3.3 ± 0.3V, T_A = -40°C to 70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC Input Logic High		V_{CC}/2 + 0.7		V_{CC} + 0.3	V
V_{IL}	DC Input Logic Low		-0.3		V_{CC}/2 - 0.7	V
V_{OL}	DC Output Logic Low	I_{OL} = 3mA			0.4	V
V_{hys}	Hysteresis of Schmitt Trigger Input		0.8			V
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax} with Bus Capacitance 10-400pF				250	ns
f_{SCL}	SCL Clock Frequency				100	kHz

Electrical Characteristics - High Speed I/O AC/DC Specifications

V_{CC} = 3.3 ± 0.3V, T_A = -40°C to 70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{RX}	RX AC Coupling Capacitance			220		nF
S_{11}	Input Return Loss	10MHz to 3GHz Differential		-21		dB
		1GHz to 3GHz Common Mode		-7		
S_{22}	Output Return Loss	10MHz to 3GHz Differential		-20		dB
		1GHz to 3GHz Common Mode		-9		
R_{IN}	DC Single-Ended Input Impedance			50		Ω
	DC Differential Input Impedance			100		
R_{OUT}	DC Single-Ended Output Impedance			50		Ω
	DC Differential Output Impedance			100		
$Z_{RX\text{-}HIZ}$	DC Input CM Input Impedance During Reset or Power Down			78		kΩ
$V_{RX\text{-}DIFF\text{-}PP}$	Differential Input Peak-to-Peak Voltage	Operational			1.2	Vppd
V_{RX_CM}	Input Source Common-Mode Noise	DC – 200MHz			150	mVpp
P_{active}	Supply Power @ Active Mode, with Signal	PD = 0			1656	mW
I_{active}	Supply Current @ Active Mode, with Signal				460	mA
$I_{standby}$	Supply Current @ Standby Mode	PD = 1			110	uA
t_{pd}	Latency	From Input to Output		0.5		ns

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
G_P	Peaking Gain (Compensation at 3GHz, Relative to 100MHz, 100mVp-p Sine Wave Input)	EQ<2:0> = 111 EQ<2:0> = 000		8.9 2.5		dB
		Variation Around Typical	-3		+3	dB
G_F	Flat Gain (100MHz)	SF = R/1 SF = 0/F		-0.5 -3.5		dB
		Variation Around Typical	-3		+3	dB
V_{1dB_100M}	-1dB Compression Point of Output Swing (at 100MHz)	SF = 1, EQ<2:0> = 111 SF = R, EQ<2:0> = 111		1200 1100		mVppd
V_{1dB_3G}	-1dB Compression Point of Output Swing (at 3GHz)	SF = 1, EQ<2:0> = 111 SF = R, EQ<2:0> = 111		1100 900		mVppd
V_{Coup}	Channel Isolation	100MHz to 3GHz, at EQ = 000 Figure 1 (Note 1)		-50		dB
V_{noise_input}	Input-Referred Noise	100MHz to 3GHz, SF = 1, EQ<2:0> = 000, Figure 2		0.8		mV_{RMS}
		100MHz to 3GHz, SF = 1, EQ<2:0> = 111, Figure 2		0.5		
V_{noise_output}	Output-Referred Noise(2)	100MHz to 3GHz, SF = 1, EQ<2:0> = 000, Figure 2		0.7		mV_{RMS}
		100MHz to 3GHz, SF = 1, EQ<2:0> = 111, Figure 2		1.0		

Note:
1. Measured using a vector-network analyzer (VNA) with -30dBm power level applied to the adj cent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.
2. Guaranteed by design and characterization.

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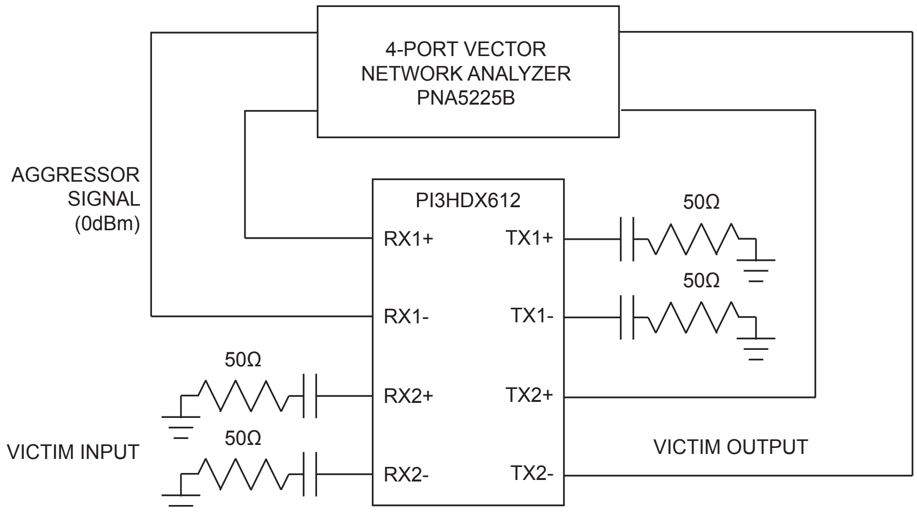


Figure 1. Channel-Isolation Test Configuration

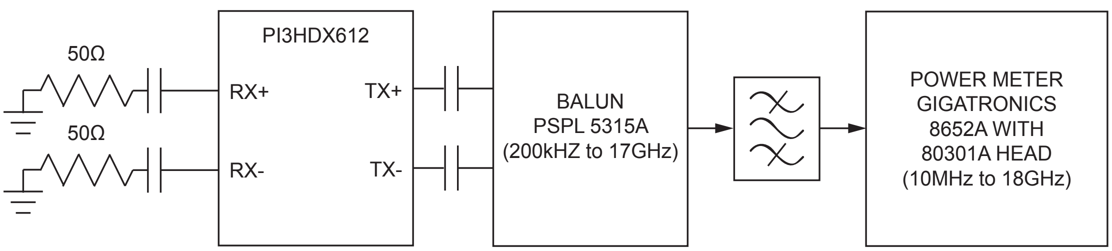
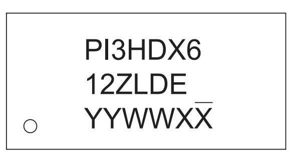


Figure 2. Noise Test Configuration

Part Marking



YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

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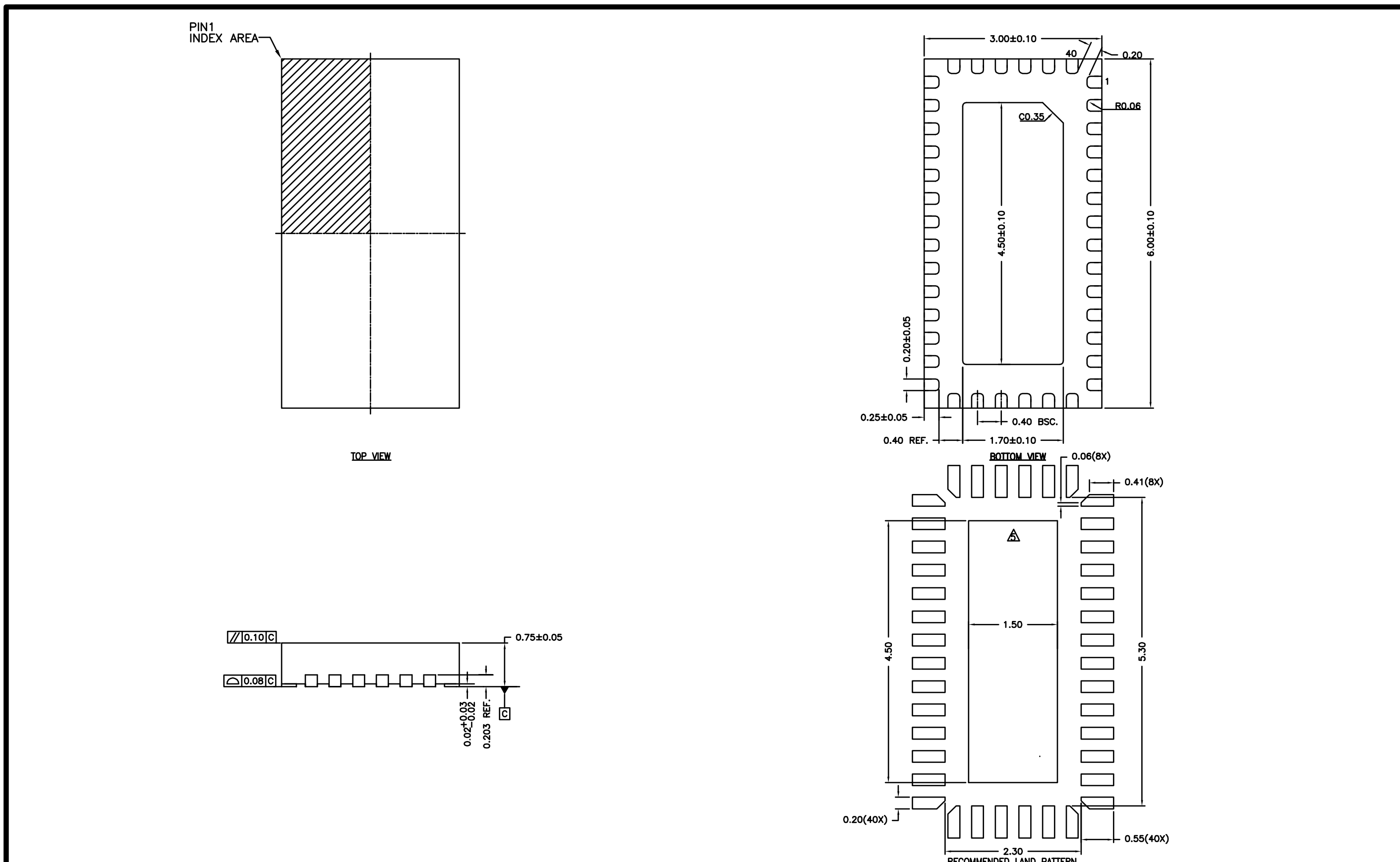
Packaging Mechanical

40-TQFN (ZLD)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

DIODES INCORPORATED / PERICOM	DATE: 05/09/22
DESCRIPTION: TQFN (W-QFN3060-40)	
PACKAGE CODE: ZLD (ZLD40)	
DOCUMENT CONTROL #: PD-2239	REVISION: A

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Number	Package Code	Package Description
PI3HDX612ZLDEX	ZLD	TQFN (W-QFN3060-40)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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