

**3.3V PCI Express® 3.0 2-Lane Exchange Switch**

**Features**

- 8 Differential Channel (2-lane) Exchange
- PCI Express® 3.0 performance, 8.0 Gbps
- Bi-directional operation
- Low Bit-to-Bit Skew: 10ps (between ± signals)
- Low Crosstalk: -29dB @ 2.5GHz (5Gbps)  
-20dB @ 4.0GHz (8Gbps)
- Low Insertion Loss: -1.1dB @ 2.5GHz (5Gbps)  
-1.45dB @ 4.0GHz (8Gbps)
- V<sub>DD</sub> Operating Range: 3.3V ±10%
- Industrial Temperature Range: -40°C to 85°C
- ESD Tolerance: 2kV HBM
- Packaging (Pb-free & Green):
  - 42-contact, TQFN (ZH42), 3.5x9mm.
  - 40-contact, TQFN (ZL40), 3x6mm.

**Description**

Pericom semiconductor's PI3PCIE3442 is a differential exchange switch featuring pass-through pinout. It supports two full PCI Express® lanes operating at 8.0Gbps PCIe® 3.0 performance.

With the select control input low, Port A connects to Port B, and Port C connects to port D for an 8-channel differential pass-through. When the select control input is high Port A connects to Port D, and Port B connects to Port C.

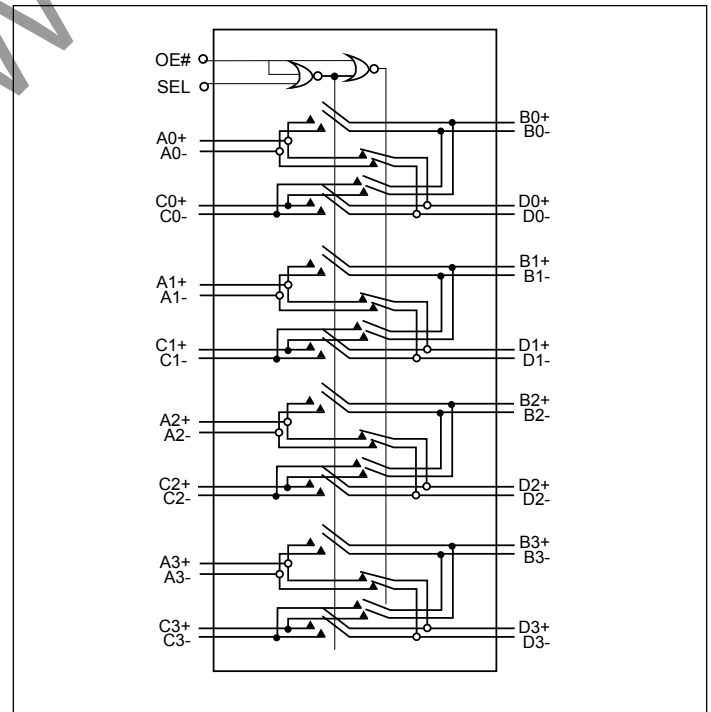
**Application**

Switching 4 lanes of DP1.2 from PC/Notebook/Tablet to Display monitor

**Truth Table**

Function	SEL	OE#
Ax = Bx Cx = Dx	0	0
Ax = Dx Cx = Bx	1	0
Ax, Bx, Cx, Dx = Hi-Z (disconnect)	x	1

**Block Diagram**



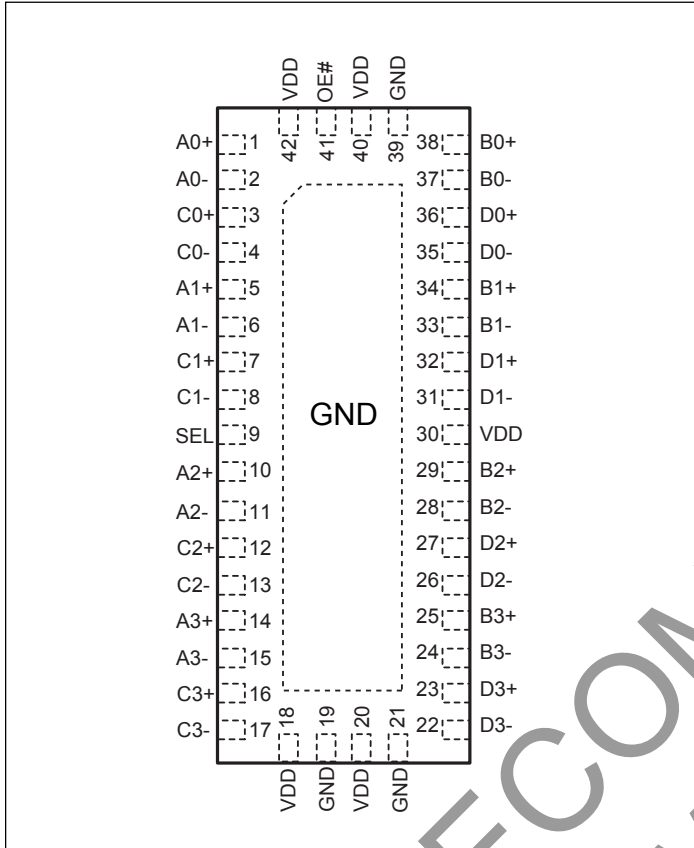


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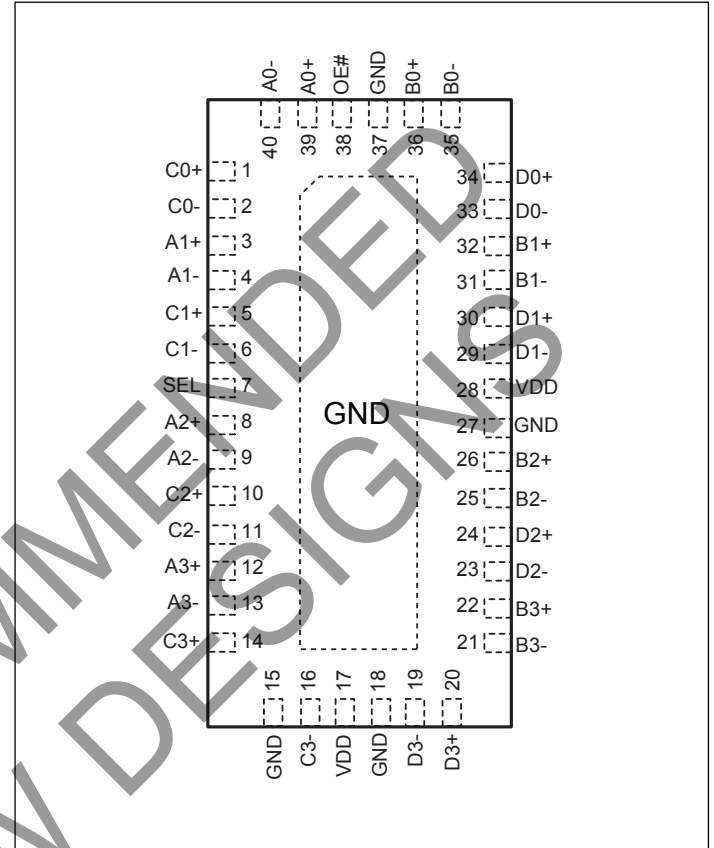


PI3PCIE3442

**Pin Diagram 42-TQFN**

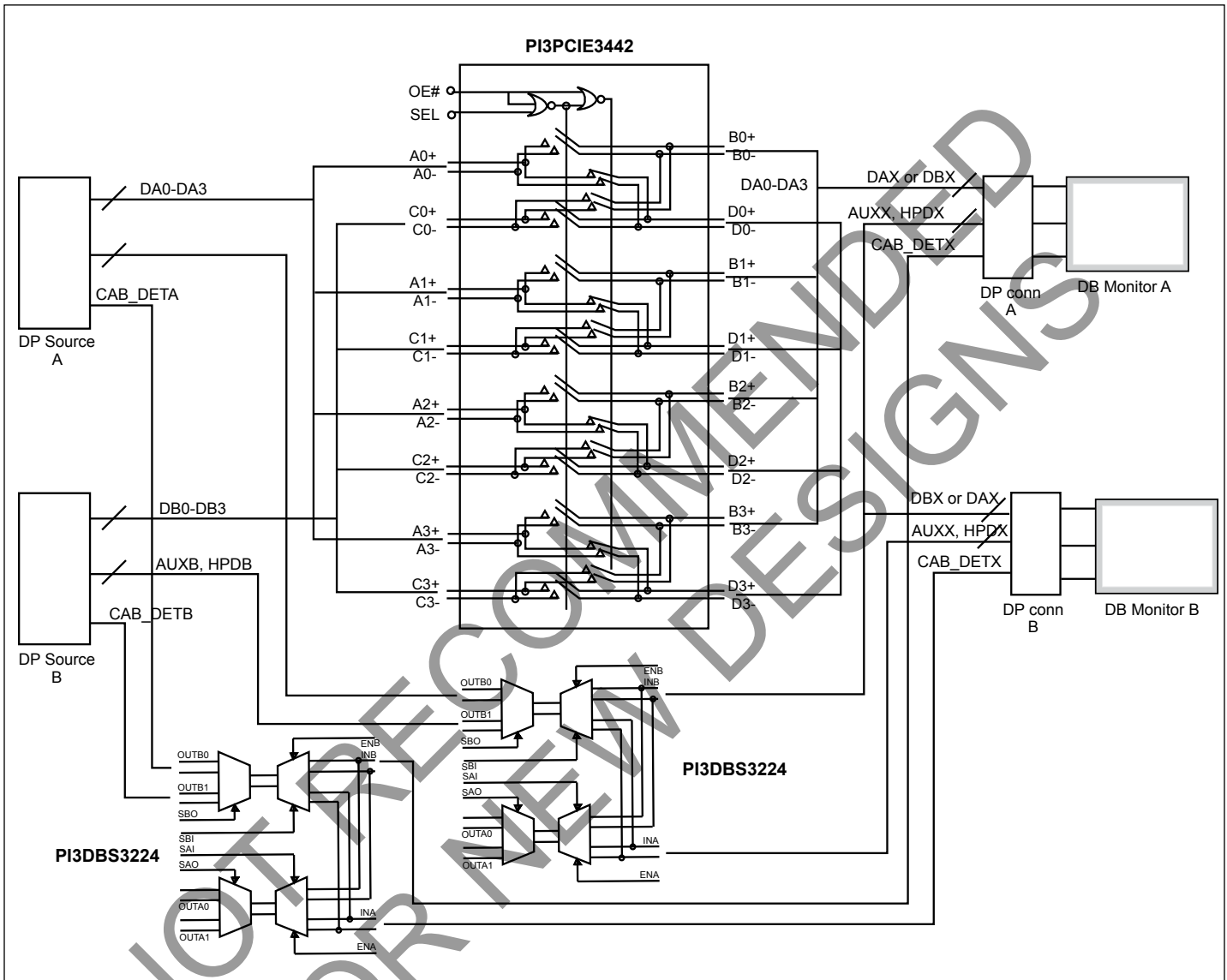


**Pin Diagram 40-TQFN**



NOT RECOMMENDED FOR NEW DESIGNS

**Application Diagram**



**Generic 2 x 2 DP1.2 Switching Using PI3PCIE3442 (3x6mm 40 pad QFN)**

**Pin Description (42-TQFN)**

Pin #	Pin Name	I/O	Description
1	A0+	I/O	Signal I/O, Channel 0, Port A
2	A0-		
5	A1+	I/O	Signal I/O, Channel 1, Port A
6	A1-		
10	A2+	I/O	Signal I/O, Channel 2, Port A
11	A2-		
14	A3+	I/O	Signal I/O, Channel 3, Port A
15	A3-		
38	B0+	I/O	Signal I/O, Channel 0, Port B
37	B0-		
34	B1+	I/O	Signal I/O, Channel 1, Port B
33	B1-		
29	B2+	I/O	Signal I/O, Channel 2, Port B
28	B2-		
25	B3+	I/O	Signal I/O, Channel 3, Port B
24	B3-		
3	C0+	I/O	Signal I/O, Channel 0, Port C
4	C0-		
7	C1+	I/O	Signal I/O, Channel 1, Port C
8	C1-		
12	C2+	I/O	Signal I/O, Channel 2, Port C
13	C2-		
16	C3+	I/O	Signal I/O, Channel 3, Port C
17	C3-		
36	D0+	I/O	Signal I/O, Channel 0, Port D
35	D0-		
32	D1+	I/O	Signal I/O, Channel 1, Port D
31	D1-		
27	D2+	I/O	Signal I/O, Channel 2, Port D
26	D2-		
23	D3+	I/O	Signal I/O, Channel 3, Port D
22	D3-		
41	OE#	I	Output Enable, active low. When OE# = 0 the device I/O is enabled. When OE#=1, all I/O are high impedance
9	SEL	I	Operation mode Select (when SEL=0: A→B, C→D, when SEL=1: A→D, C→B)
18, 20, 30, 40, 42	V <sub>DD</sub>	Pwr	3.3V ±10% Positive Supply Voltage
19, 21, 39, Center Pad	GND	Pwr	Power ground

**Pin Description (40-TQFN)**

Pin #	Pin Name	I/O	Description
39	A0+	I/O	Signal I/O, Channel 0, Port A
40	A0-		
3	A1+	I/O	Signal I/O, Channel 1, Port A
4	A1-		
8	A2+	I/O	Signal I/O, Channel 2, Port A
9	A2-		
12	A3+	I/O	Signal I/O, Channel 3, Port A
13	A3-		
36	B0+	I/O	Signal I/O, Channel 0, Port B
35	B0-		
32	B1+	I/O	Signal I/O, Channel 1, Port B
31	B1-		
26	B2+	I/O	Signal I/O, Channel 2, Port B
25	B2-		
22	B3+	I/O	Signal I/O, Channel 3, Port B
21	B3-		
1	C0+	I/O	Signal I/O, Channel 0, Port C
2	C0-		
5	C1+	I/O	Signal I/O, Channel 1, Port C
6	C1-		
10	C2+	I/O	Signal I/O, Channel 2, Port C
11	C2-		
14	C3+	I/O	Signal I/O, Channel 3, Port C
16	C3-		
34	D0+	I/O	Signal I/O, Channel 0, Port D
33	D0-		
30	D1+	I/O	Signal I/O, Channel 1, Port D
29	D1-		
24	D2+	I/O	Signal I/O, Channel 2, Port D
23	D2-		
20	D3+	I/O	Signal I/O, Channel 3, Port D
19	D3-		
38	OE#	I	Output Enable, active low. When OE# = 0 the device I/O is enabled. When OE#=1, all I/O are high impedance
7	SEL	I	Operation mode Select (when SEL=0: A→B, C→D, when SEL=1: A→D, C→B)
17, 28	V <sub>DD</sub>	Pwr	3.3V ±10% Positive Supply Voltage
15, 18, 27, 37, Center Pad	GND	Pwr	Power ground



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**PI3PCIE3442**

### Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Supply Voltage to Ground Potential .....	-0.5V to +4.6V
DC Input Voltage .....	-0.5V to V <sub>DD</sub>
DC Output Current .....	120mA
Power Dissipation .....	0.5W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Electrical Characteristics Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>DD</sub>	3.3V Power Supply		3.0	3.3	3.6	V
I <sub>DD</sub>	Total current from V <sub>DD</sub> 3.3V supply	SEL and OE# at OV or V <sub>DD</sub>			300	μA
T <sub>A</sub>	Operating temperature range		-40		85	°C

### DC Electrical Characteristics for Switching over Operating Range

Parameters	Description	Test Conditions <sup>(1)</sup>	Min	Typ <sup>(1)</sup>	Max	Units
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed HIGH level	0.65 x V <sub>DD</sub>			V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed LOW level	-0.5		0.35 x V <sub>DD</sub>	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>DD</sub> = Max., I <sub>IN</sub> = -18mA		-0.7	-1.2	μA
I <sub>IH</sub>	Input HIGH Current, SEL	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>DD</sub>	-10		+10	
I <sub>IL</sub>	Input LOW Current, SEL	V <sub>DD</sub> = Max., V <sub>IN</sub> = GND	-10		+10	
I <sub>IH</sub>	Input HIGH Current, A <sub>X</sub> , B <sub>X</sub> , C <sub>X</sub> , D <sub>X</sub>	V <sub>DD</sub> = Max., V <sub>IN</sub> = 1.8V	-10		+10	μA
I <sub>IL</sub>	Input LOW Current, A <sub>X</sub> , B <sub>X</sub> , C <sub>X</sub> , D <sub>X</sub>	V <sub>DD</sub> = Max., V <sub>IN</sub> = 0V	-10		+10	

Note:

1. Typical values are at V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 25°C ambient and maximum loading.

### Switching Characteristics

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t <sub>PZH</sub> , t <sub>PZL</sub>	Line Enable Time - SEL to A <sub>N</sub> , B <sub>N</sub> , C <sub>N</sub> , D <sub>N</sub>		0.5		45	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Line Disable Time - SEL to A <sub>N</sub> , B <sub>N</sub> , C <sub>N</sub> , D <sub>N</sub>		0.5		25	
t <sub>b-b</sub>	Bit-to-bit skew within the same differential pair				10	ps
t <sub>ch-ch</sub>	Channel-to-channel skew				20	

### Dynamic Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Units
DDIL	Differential Insertion Loss ( $V_{IN} = -10\text{dBm}$ , DC = 0V)	f=1.2GHz		-0.8	-1.0	dB
		f=2.5GHz		-1.0	-1.2	
		f=4.0GHz		-1.3	-1.5	
		f=5.0GHz		-1.8	-2.0	
		f=7.5GHz		-4.5	-5.0	
DDIL <sub>OFF</sub>	Differential Off Isolation	f= 4.0GHz		-19		dB
DDRL	Differential Return Loss	f= 0 to 2.8GHz		-26		dB
		f= 2.8 to 5.0GHz		-14		
		f= 5.0 to 8.0GHz		-7.5		
DDNEXT	Near End Crosstalk	f= 0 to 2.8GHz		-26		dB
		f= 2.8 to 5.0GHz		-20		
		f= 5.0 to 8.0GHz		-16		
V <sub>IF</sub>	Max Signal Frequency Range	Insertion loss 1.5dB, $V_{IN}=0.623\text{Vpp}$ , DC=0V		4.0		GHz
		Insertion loss 1.5dB, $V_{IN}=0.623\text{Vpp}$ , DC=0.9V		4.0		
		Insertion loss 3dB, $V_{IN}=0.623\text{Vpp}$ , DC=0V		8.0		
		Insertion loss 3dB, $V_{IN}=0.623\text{Vpp}$ , DC=0.9V		8.0		
BW	-3dB Bandwidth			6.5		GHz

## Notes:

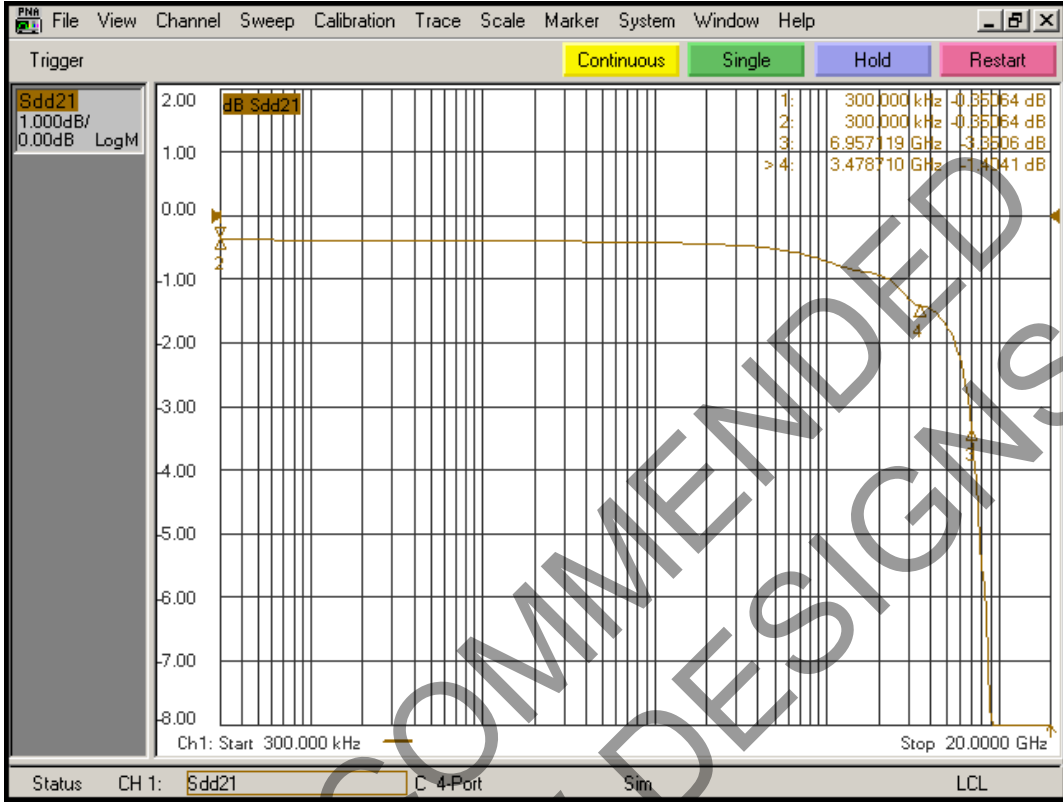
- Guaranteed by design. Typical values are at  $V_{DD} = 3.3\text{V}$ ,  $T_A = 25^\circ\text{C}$  ambient and maximum loading.



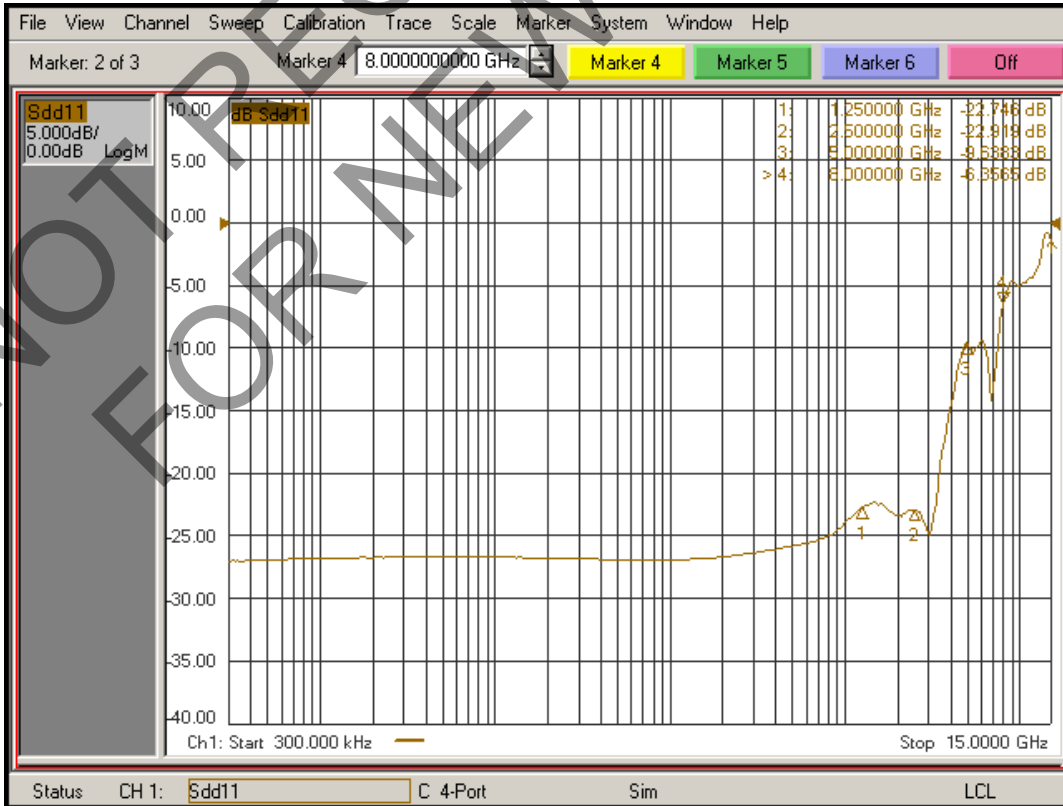
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**PI3PCIE3442**



**Differential Insertion Loss**



**Differential Return Loss**

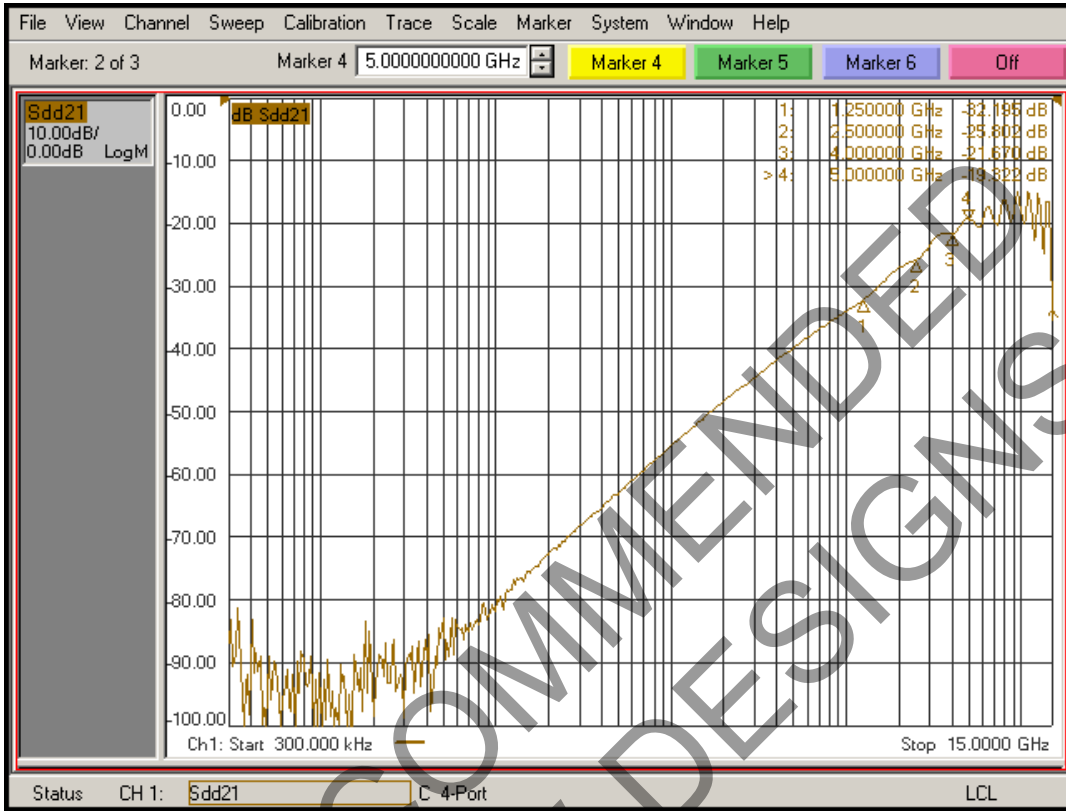




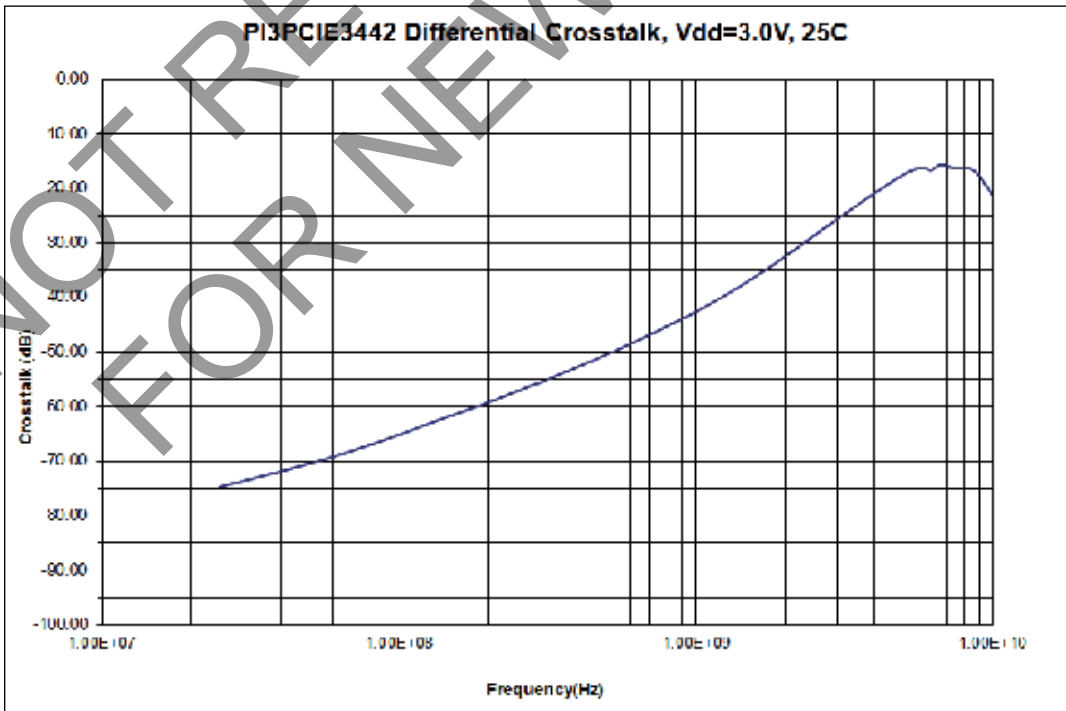
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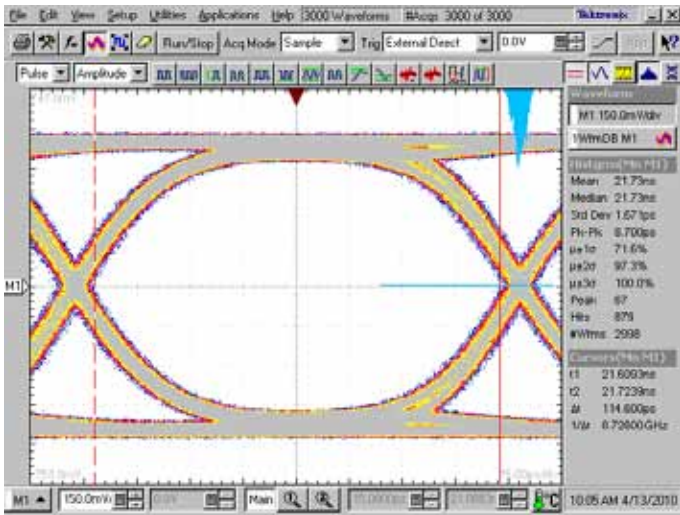
PI3PCIE3442



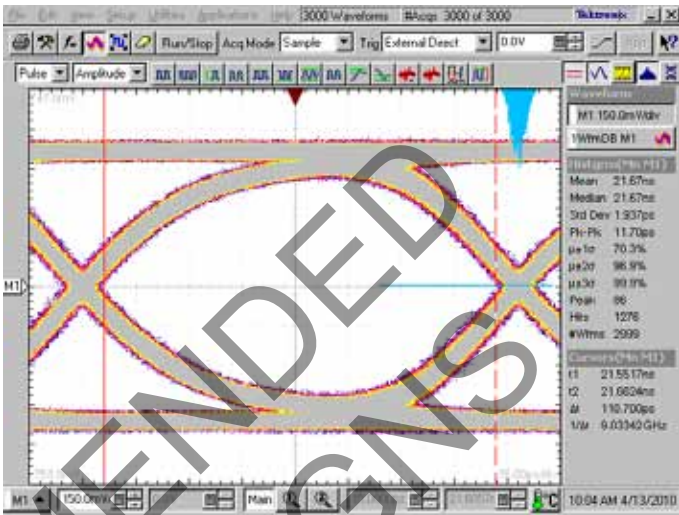
**Differential Off Isolation**



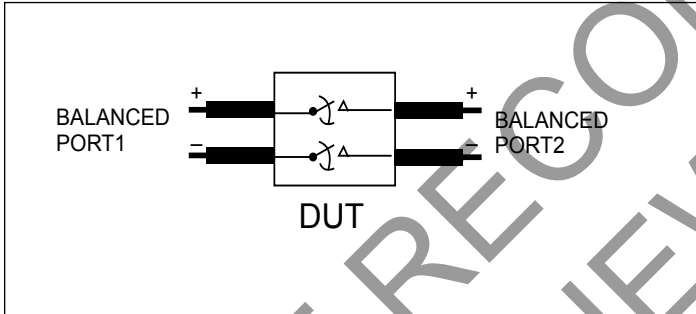
**Differential Crosstalk**



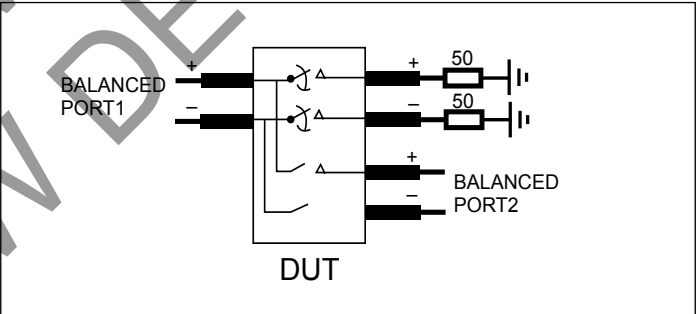
**8.0 Gbps RX signal eye without PI3PCIE3442**



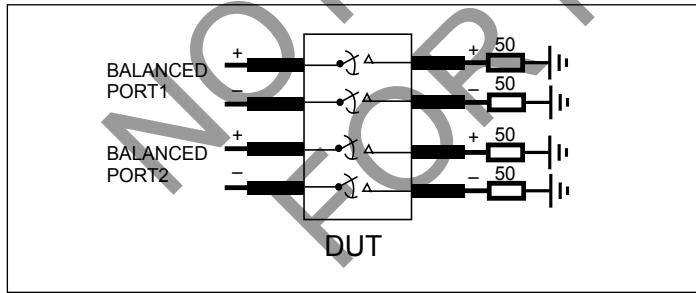
**8.0 Gbps RX signal eye with PI3PCIE3442**



**Differential Insertion Loss and Return Test Circuit**

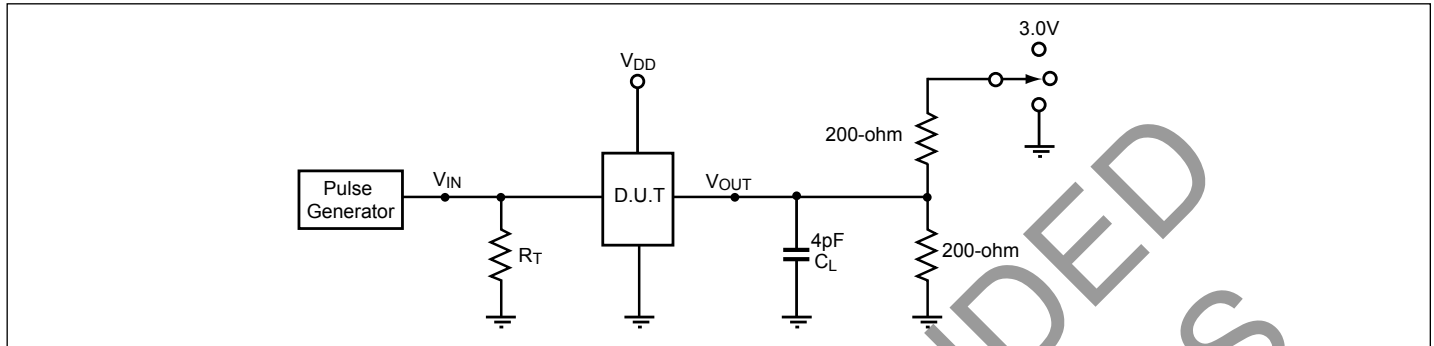


**Differential Off Isolation Test Circuit**



**Differential Near End Xtalk Test Circuit**

### Test Circuit for Electrical Characteristics(1-5)



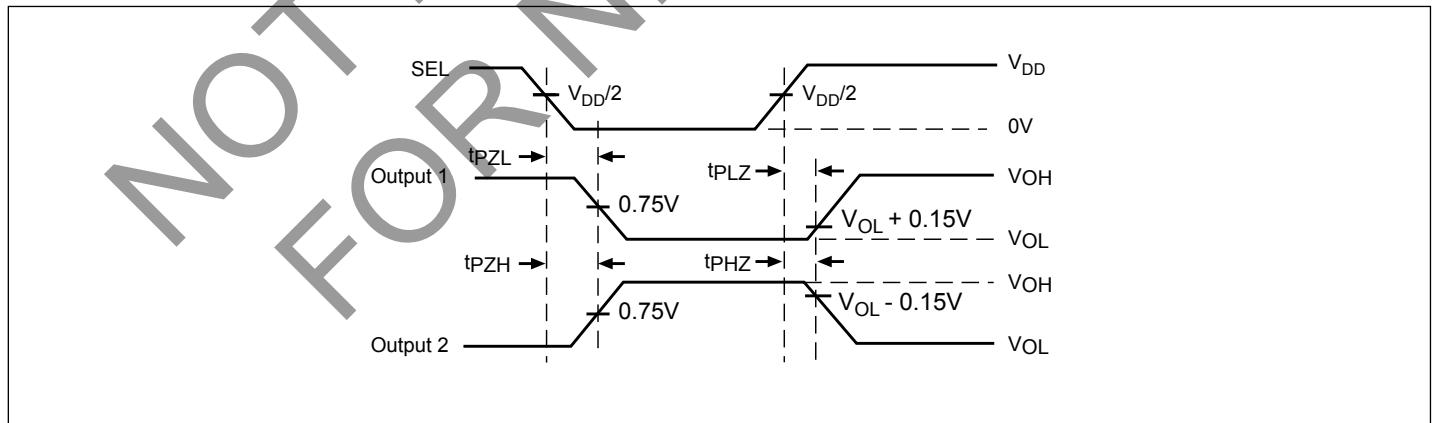
Notes:

1.  $C_L$  = Load capacitance: includes jig and probe capacitance.
2.  $R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: PRR  $\leq$  MHz,  $Z_O = 50\Omega$ ,  $t_r \leq 2.5ns$ ,  $t_f \leq 2.5ns$ .
5. The outputs are measured one at a time with one transition per measurement.

### Switch Positions

Test	Switch
$t_{PLZ}$ , $t_{PZL}$	3.0V
$t_{PHZ}$ , $t_{PZH}$	GND
Prop Delay	Open

### Switching Waveforms



Voltage Waveforms Enable and Disable Times

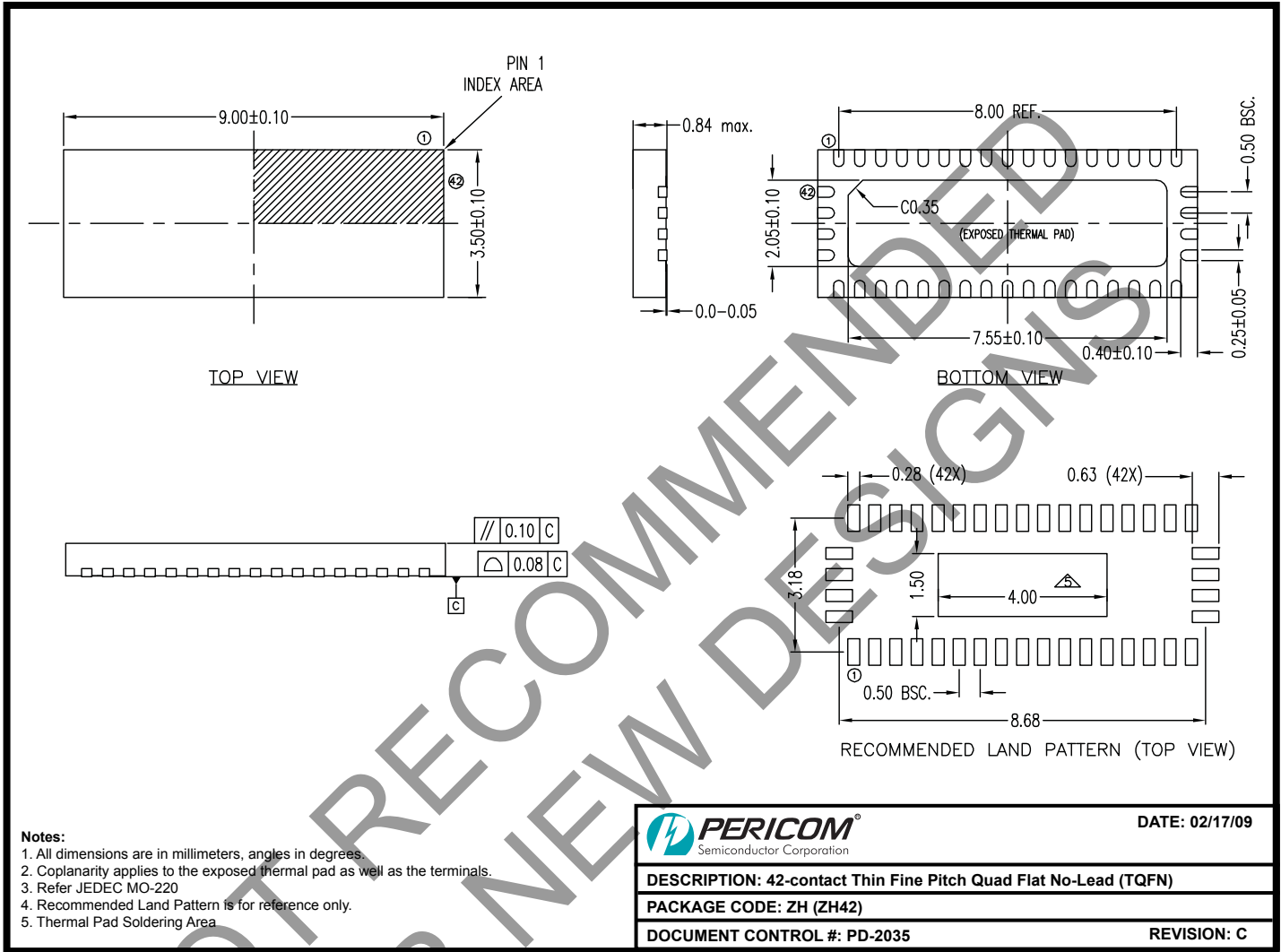


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**PI3PCIE3442**

**Packaging Information: 42-Contact TQFN (3.5x9mm)**



09-0116



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**PI3PCIE3442**

**Packaging Information: 40-Contact TQFN (3x6mm)**

**NOTE :**

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

	DATE: 07/20/15
DESCRIPTION: 40-Pin, TQFN 3X6mm	
PACKAGE CODE: ZL (ZL40)	
DOCUMENT CONTROL #: PD-2165	REVISION: B

15-0162

Note: For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

**Ordering Information**

Ordering Code	Package Code	Package Description
PI3PCIE3442ZHE	ZH	42-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)
PI3PCIE3442ZHEX	ZH	42-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN), Tape & Reel
PI3PCIE3442ZLE	ZL	40-contact, 3 x 6mm (TQFN)
PI3PCIE3442ZLEX	ZL	40-contact, 3 x 6mm (TQFN), Tape & Reel

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging

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