PI3VDP12412

4-Lane DisplayPort™ Rev 1.2 Compliant Switch

Features

- 4-lane, 1:2 mux/demux that will support RBR, HBR1, or HBR2
- 1-channel 1:2 mux/demux for DP_HPD signal
- 1-differential channel 1:2 mux/demux for DP_Aux signal with support up to 720Mbps
- -1.6dB Insertion Loss for Dx channels @ 2.7 GHz (TQFN)
- -3dB Bandwidth for Dx channels: 4.6GHz (TQFN)
- Return loss for Dx channels @ 2.7GHz: -16dB (TQFN)
- Low Bit-to-Bit Skew , 5ps typ (between '+' and '-' bits)
- Low Crosstalk for high speed channels: -28dB@5.4 Gbps
- Low Off Isolation for high speed channels: -22dB@5.4 Gbps
- V_{DD} Operating Range: 3.3V +/-10%
- ESD Tolerance: 2kV HBM
- Low channel-to-channel skew, 35ps max
- Packaging (Pb-free & Green):
  - 42 TQFN (ZHE)
  - 48 BGA (NEE)

Description

Pericom Semiconductor's PI3VDP12412 mux/demux is targeted for next generation digital video signals. This device can be used to connect a DisplayPort™ Source to two Independent DisplayPort Sinks or to connect two DisplayPort sources to a single DP display.

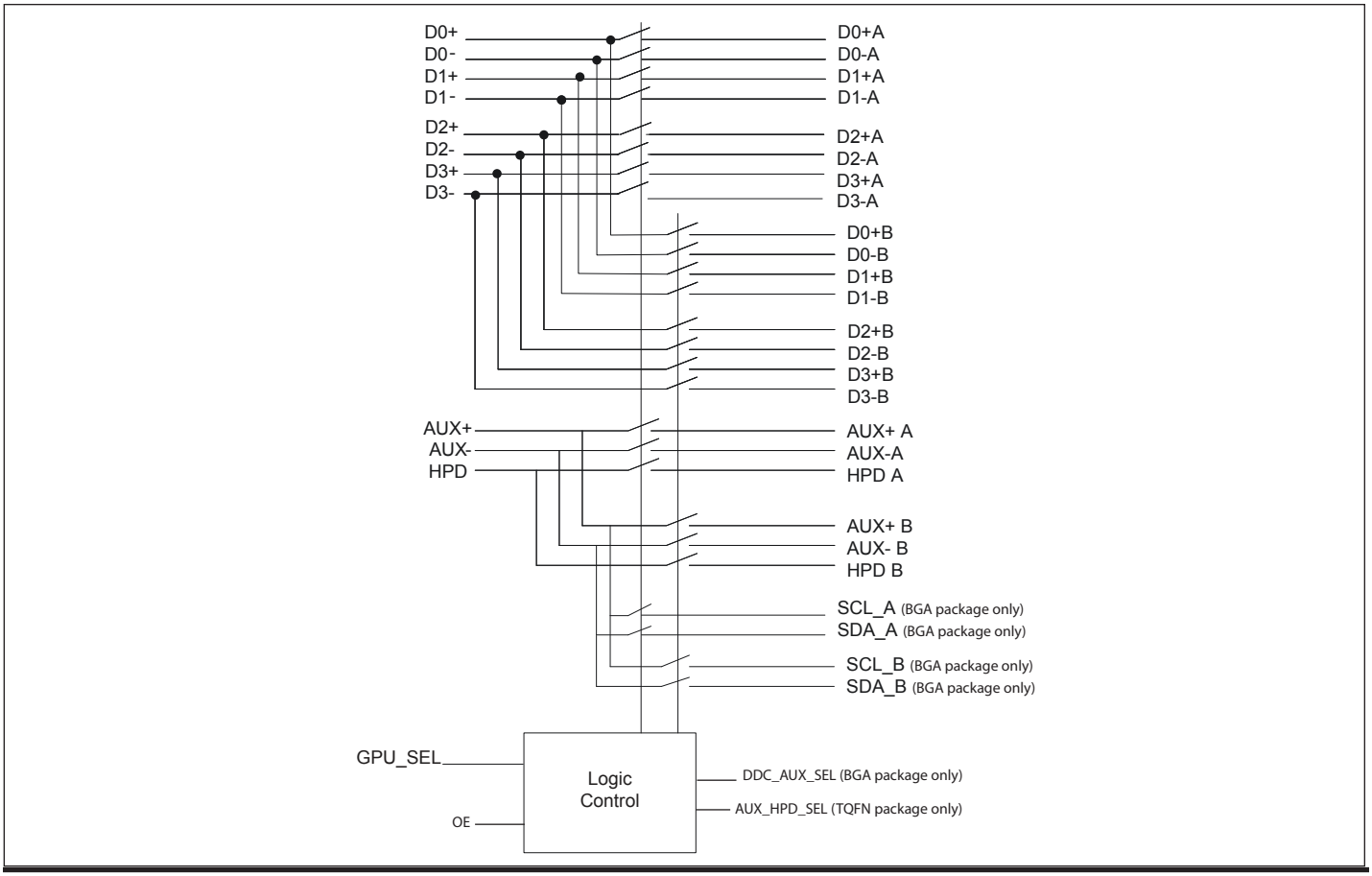
PI3VDP12412 supports DisplayPort 1.2 which requires a data rate of 5.4 Gbps. PI3VDP12412 offers excellent signal integrity at this high data rate with very low insertion loss, good return loss, and very small crosstalk.

PI3VDP12412 is available in two package types, a 5 mm x 5 mm 48 BGA and a 3.5 mm x 9 mm 42 TQFN. The BGA consumes less board space. The TQFN achieves slightly better signal integrity.

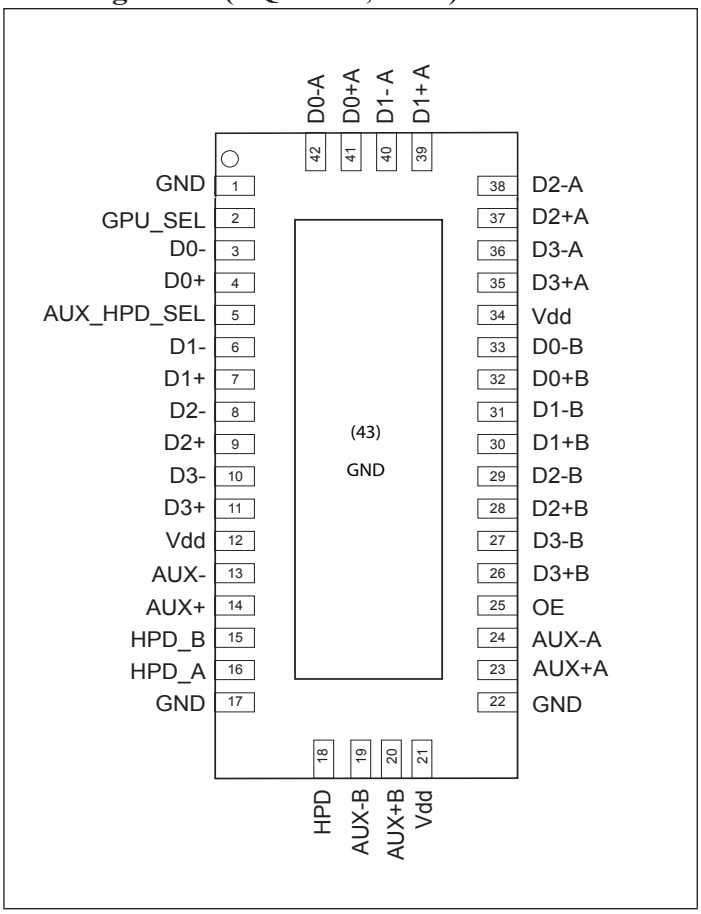
Application

Routing of DisplayPort signals with low signal attenuation between source and sink.

Block Diagram



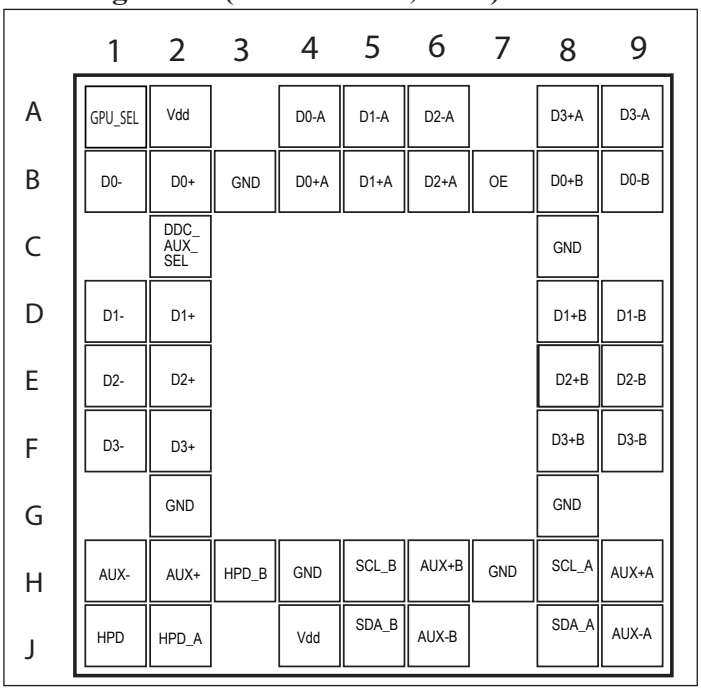
Pin Assignment (TQFN-42, ZHE)



Truth Table for 42 pin package

OE	GPU_ SEL	AUX_ HPD_ SEL	Function
High	Low	Low	Port A active for all channels
High	Low	High	Port A for HS, port B for HPD/AUX
High	High	Low	Port B for HS, port A for HPD/AUX
High	High	High	Port B active for all channels
Low	x	x	All I/O's are hi-z and IC is power down

Pin Assignment (48-Ball BGA, NEE)



OE	GPU_ SEL	DDC_ AUX_ SEL	Function
High	Low	Low	Port A active for AUX, HPD & HS channel
High	Low	High	Port A active for DDC, HPD, & HS channel
High	High	Low	Port B active for AUX, HPD & HS channel
High	High	High	Port B active for DDC, HPD & HS channel
Low	x	x	all I/Os are hi-z and IC is power down

42ZHE pin#	48NEE pin#	pin Name	Signal Type	Description
2	A1	GPU_SEL	I	switch logic control. different function for different package options: 42pin TQFN package: If HIGH, then path B is selected for high speed channels only If LOW, then path A is selected for high speed channels only 48ball BGA package: If HIGH, then path B is selected for all channels If LOW, then path A is selected for all channels
3	B1	D0-	I/O	negative differential signal 0 for COM port
4	B2	D0+	I/O	positive differential signal 0 for COM port
6	D1	D1-	I/O	negative differential signal 1 for COM port
7	D2	D1+	I/O	positive differential signal 1 for COM port
8	E1	D2-	I/O	negative differential signal 2 for COM port
9	E2	D2+	I/O	positive differential signal 2 for COM port
10	F1	D3-	I/O	negative differential signal 3 for COM port
11	F2	D3+	I/O	positive differential signal 3 for COM port
1	B3	GND	Ground	Ground
13	H1	AUX-	I/O	negative differential signal for AUX COM port
14	H2	AUX+	I/O	positive differential signal for AUX COM port
18	J1	HPD	I/O	HPD for COM port
16	J2	HPD_A	I/O	HPD for port A
15	H3	HPD_B	I/O	HPD for port B
17	C8	GND	Ground	Ground
12	J4	VDD	Pwr	3.3V +/-10% power supply
	G2	GND	Ground	Ground
20	H6	AUX+B	I/O	positive differential signal for AUX, port B
19	J6	AUX-B	I/O	negative differential signal for AUX, port B
23	H9	AUX+A	I/O	positive differential signal for AUX, port A
24	J9	AUX-A	I/O	negative differential signal for AUX, port A
22	G8	GND	Ground	Ground
26	F8	D3+B	I/O	positive differential signal 3 for portB
27	F9	D3-B	I/O	negative differential signal 3 for portB
28	E8	D2+B	I/O	positive differential signal 2 for portB
29	E9	D2-B	I/O	negative differential signal 2 for portB
30	D8	D1+B	I/O	positive differential signal 1 for portB
31	D9	D1-B	I/O	negative differential signal 1 for portB
32	B8	D0+B	I/O	positive differential signal 0 for portB

(Continued)

42ZHE pin#	48NEE pin#	pin Name	Signal Type	Description
33	B9	D0-B	I/O	negative differential signal 0 for portB
35	A8	D3+A	I/O	positive differential signal 3 for port A
36	A9	D3-A	I/O	negative differential signal 3 for port A
	H4	GND	Ground	
37	B6	D2+A	I/O	positive differential signal 2 for port A
38	A6	D2-A	I/O	negative differential signal 2 for port A
39	B5	D1+A	I/O	positive differential signal 1 for port A
40	A5	D1-A	I/O	negative differential signal 1 for port A
41	B4	D0+A	I/O	positive differential signal 0 for port A
42	A4	D0-A	I/O	negative differential signal 0 for port A
21	A2	VDD	Pwr	Power
34		VDD	Pwr	Power
N/A	C2	DDC_ AUX_SEL	I	toggles between passing DDC channels through or AUX channels through If HIGH, then path DDC signals are passed through (depending on port selection via GPU_SEL) If LOW, then path AUX signals are passed through (depending on port selection via GPU_SEL)
5	N/A	AUX_HPD_ SEL	I	switches only the AUX and HPD channels from port A vs. port B
N/A	H5	SCL_B	I/O	DDC_clock channel for port B
N/A	H7	GND	Ground	
N/A	H8	SCL_A	I/O	DDC_clock channel for port A
N/A	J5	SDA_B	I/O	DDC_data channel for port B
N/A	J8	SDA_A	I/O	DDC_data channel for port A
25	B7	OE	I	Output enable. if OE is high, IC is enabled. If OE is low, then IC is power down and all I/Os are hi-z
43	N/A	Center pad	Ground	Ground

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +4.2V
DC Input Voltage	–0.5V to V_{DD}
DC Output Current	120mA
Power Dissipation	0.5W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics for Switching over Operating Range (T_A = –40°C to +105°C, V_{DD} = 3.3V ±10%)

Parameter	Description	Test Conditions(1)	Min	Typ(2)	Max	Units
V_{IH}	Input HIGH Voltage	Guaranteed HIGH level	1.5			V
V_{IL}	Input LOW Voltage	Guaranteed LOW level			0.75	
V_{IK}	Clamp Diode Voltage (HS Channel)	V_{DD} = Max., I_{IN} = –18mA		–1.6V	–1.8	
V_{IK}	Clamp Diode Voltage (Aux, Cntrl)	V_{DD} = Max., I_{IN} = –18mA		–0.7	–1.5	
I_{IH}	Input HIGH Current	V_{DD} = Max., V_{IN} = V_{DD}			±5	µA
I_{IL}	Input LOW Current	V_{DD} = Max., V_{IN} = GND			±5	
I_{OFF_SB}	I/O leakage when part is off for side-band signals only (DDC, AUX, HPD)	V_{DD} = 0V, V_{INPUT} = 0V to 3.6V			20	
R_{ON_HS}	On resistance between input to output for high speed signals	V_{DD} = 3.0V, Vinput = -0.35V to 2V, I_{INPUT} = 20mA		10.0		Ohm
R_{ON_AUX}	On resistance between input to output for side-band signals (AUX)	V_{DD} = 3.0V, Vinput = 0 to 3.3V, I_{INPUT} = 20mA		7		Ohm
R_{ON_DDC}	On resistance between input to output for DDC channel	V_{DD} = 3.0V, Vinput = 0V, I_{INPUT} = 20mA		10		Ohm
Aux_ss	Signal Swing Tolerance in Aux path	V_{DD} = 3.0V	–0.5		3.6	V
HPD_I	Input voltage on HPD path				5.5	V
HPD_O	Output voltage tolerance on HPD path	HPD input from 3.3V to 5.25V		3.3	3.6	V

Power Supply Characteristics (T_A = –40°C to +105°C)

Parameter	Description	Test Conditions(1)	Min	Typ(2)	Max	Units
I_{DD}	Power Supply Current	V_{DD} = 3.3V, OE = 3.3V, V_{IN} = GND or V_{DD}		0.4	1	mA
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = 3.3V, OE = GND		1		µA

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Dynamic Electrical Characteristics over Operating Range (T_A = -40° to +105°C, V_{DD} = 3.3V ±10%)

Parameter	Description	Test Conditions[1]		Min	Typ[2]	MAX	Units
X_{TALK}	Crosstalk on High Speed Channels	See Fig. 1 for Measurement Setup	f= 2.7 GHz		-28	-25	dB
			f = 1.35 GHz		-32	-28	
O_{IRR}	OFF Isolation on High Speed Channels	See Fig. 2 for Measurement Setup,	f= 2.7 GHz		-22	-20	
			f = 1.35 GHz		-30	-27	
I_{LOSS}	Differential Insertion Loss on High Speed Channels	@5.4Gbps (see figure 3)	TQFN package	-1.8	-1.6		dB
			BGA package	-2.0	-1.8		
R_{loss}	Differential Return Loss on high speed channels	@ 2.7GHz (5.4Gbps)	TQFN package		-16.0	-14	dB
			BGA package		-14	-12.5	
BW_Dx±	Bandwidth -3dB for Main high speed path (Dx±)	See figure 3	TQFN package	4.1	4.6		GHz
			BGA package	3.7	4.1		
BW_AUX/ HPD	-3dB BW for AUX and HPD signals	See figure 3		1.35	1.5		GHz
Tsw a-b	time it takes to switch from port A to port B					1	us
Tsw b-a	time it takes to switch from port B to port A					1	us
Tstartup	V_{DD} valid to channel enable					10	us
Twakeup	Enabling output by changing OE from low to High					10	us

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Switching Characteristics (T_A= -40° to +105°C, V_{DD} = 3.3V±10%)

Parameter	Description	Min.	Typ.	Max.	Units
T_{pd}	Propagation delay (input pin to output pin) on all channels		80		ps
t_{b-b}	Bit-to-bit skew within the same differential pair of Dx± channels		5	7	ps
t_{ch-ch}	Channel-to-channel skew of Dx± channels			35	ps

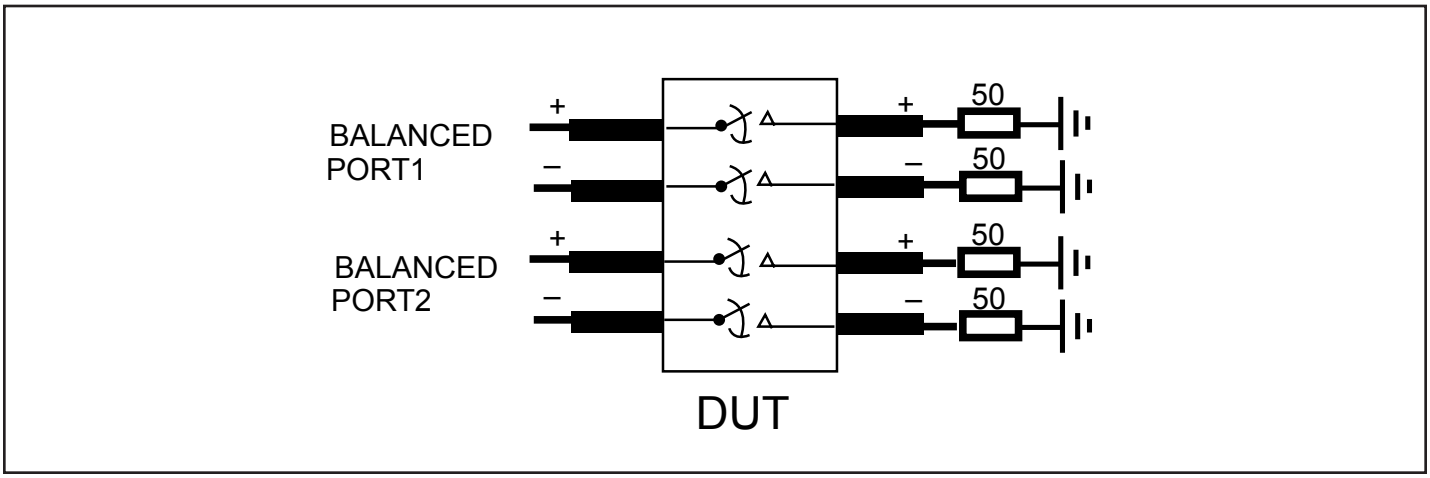


Fig 1. Crosstalk Setup

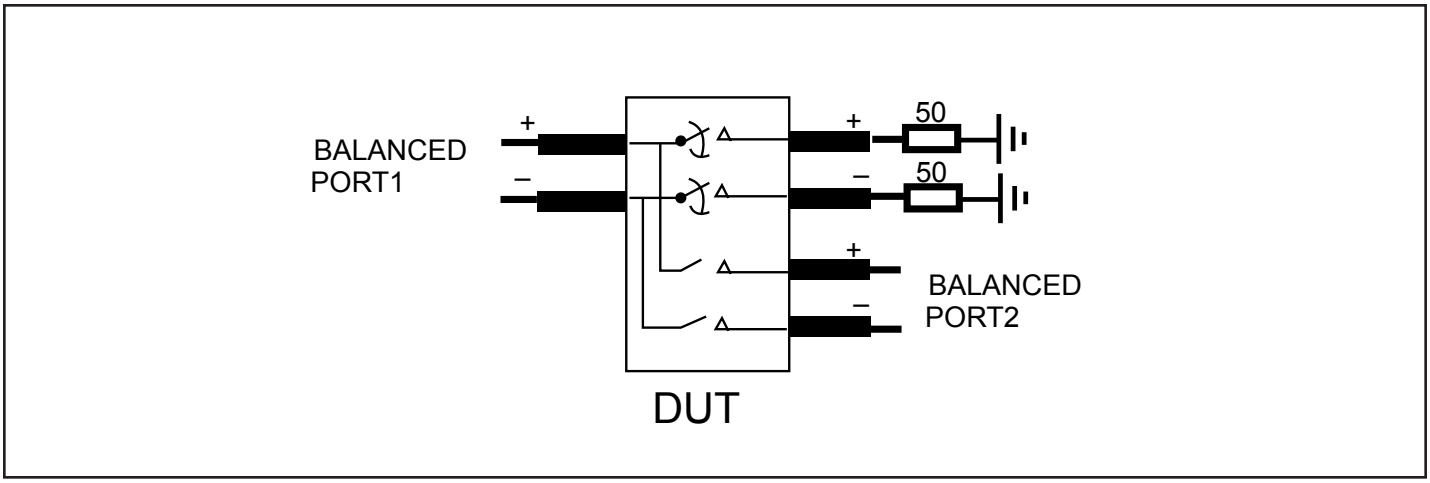


Fig 2. Off-isolation setup

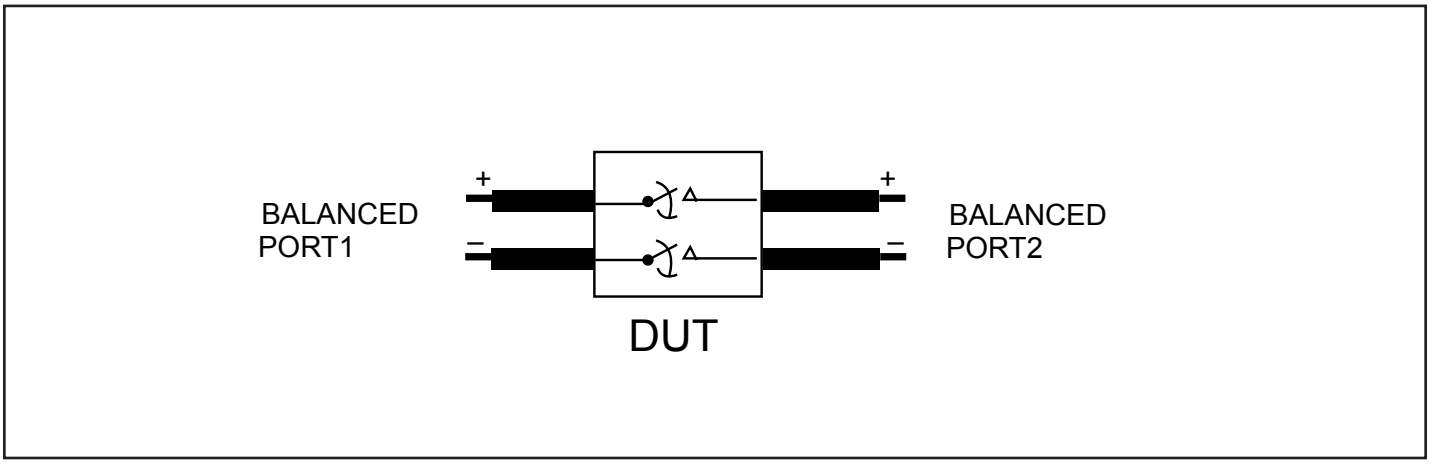
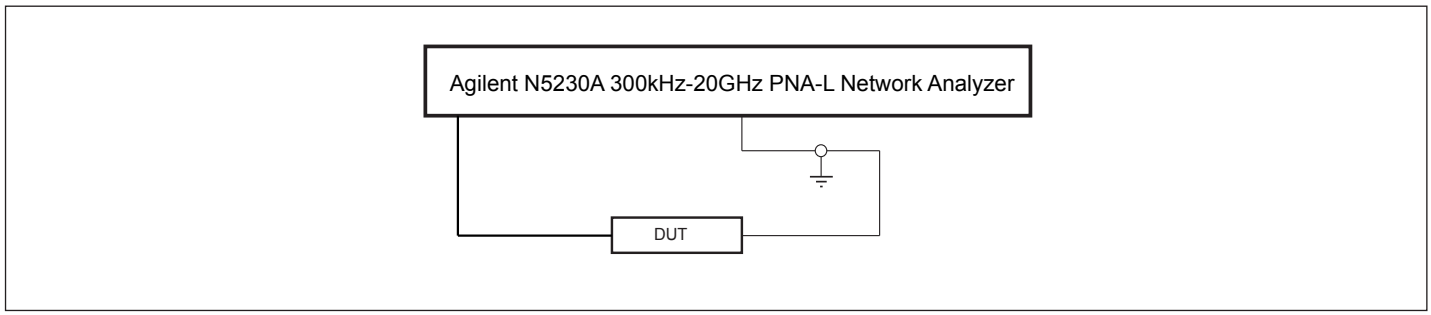


Fig 3. Differential Insertion Loss

Test Circuit for Dynamic Electrical Characteristics



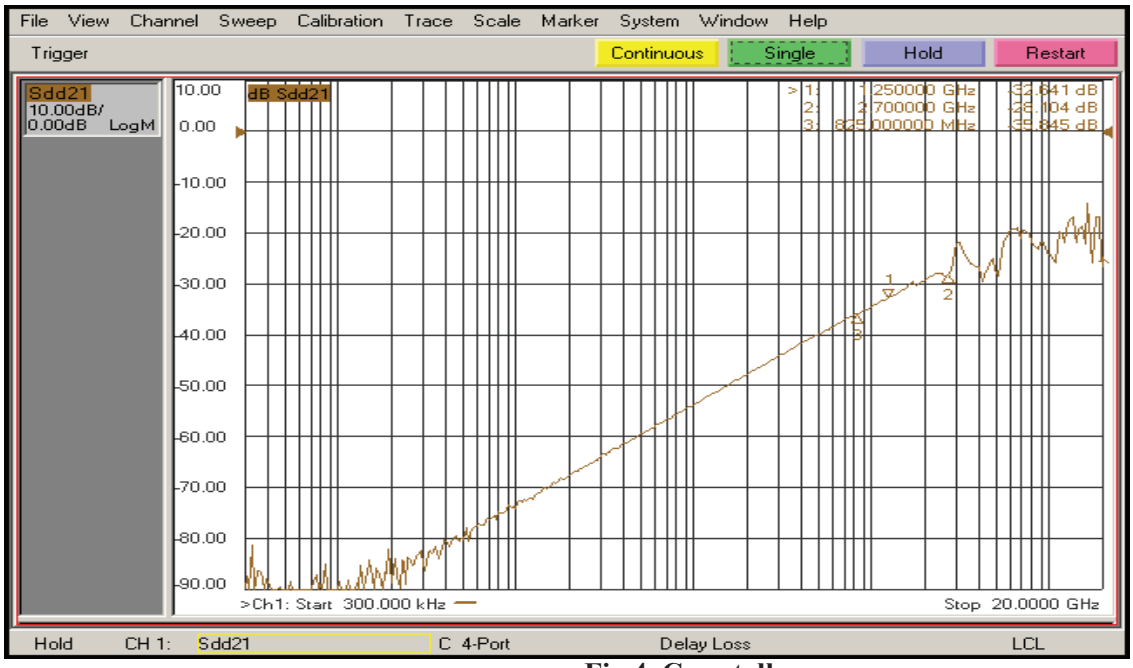


Fig 4. Crosstalk

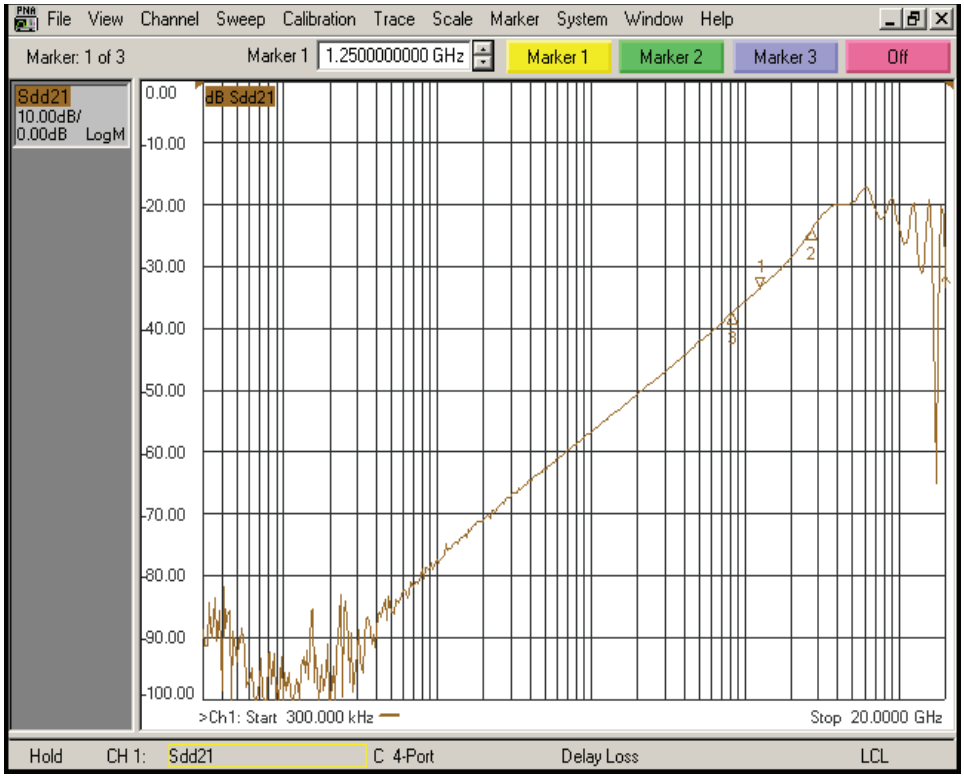


Fig 5. Off Isolation

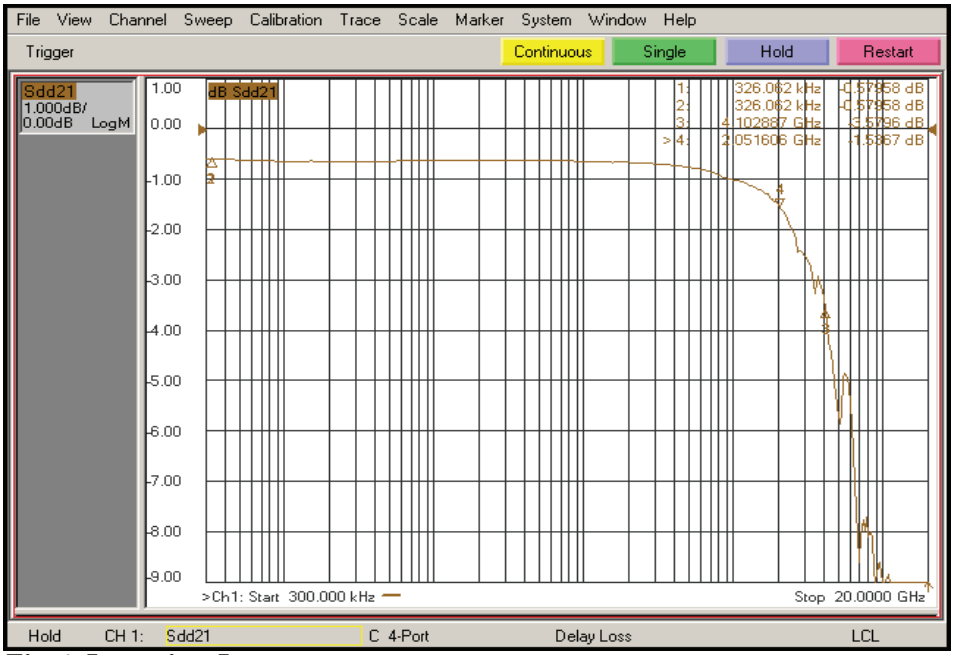
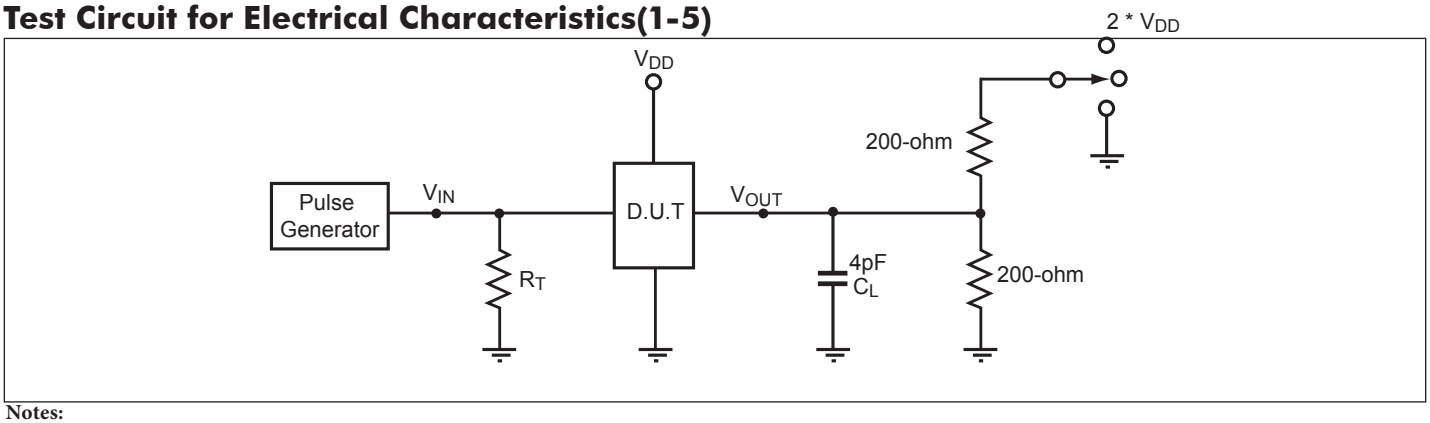


Fig 6. Insertion Loss

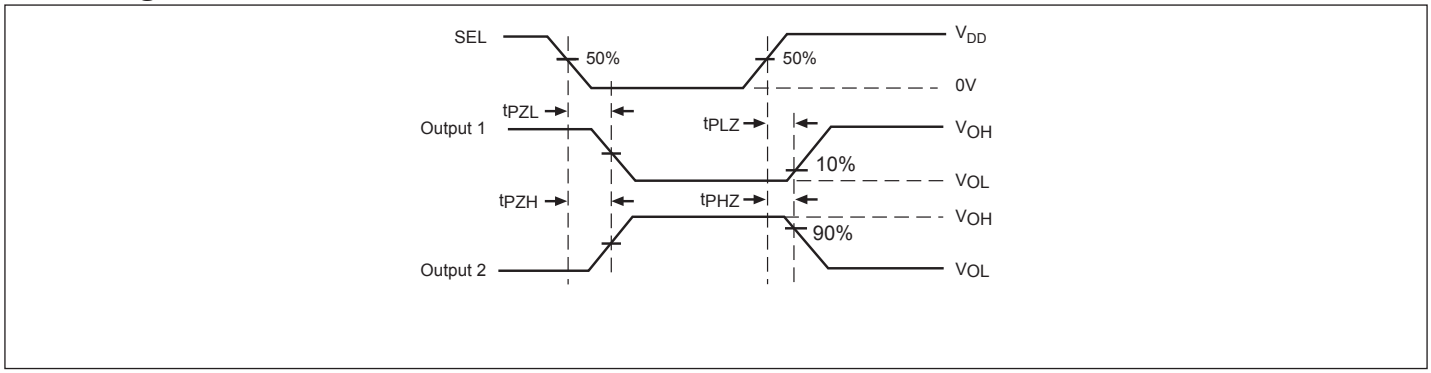
Test Circuit for Electrical Characteristics(1-5)



Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
4. Output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
5. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, $Z_O = 50\Omega$, $t_R \leq 2.5$ns, $t_F \leq 2.5$ns.
6. The outputs are measured one at a time with one transition per measurement.

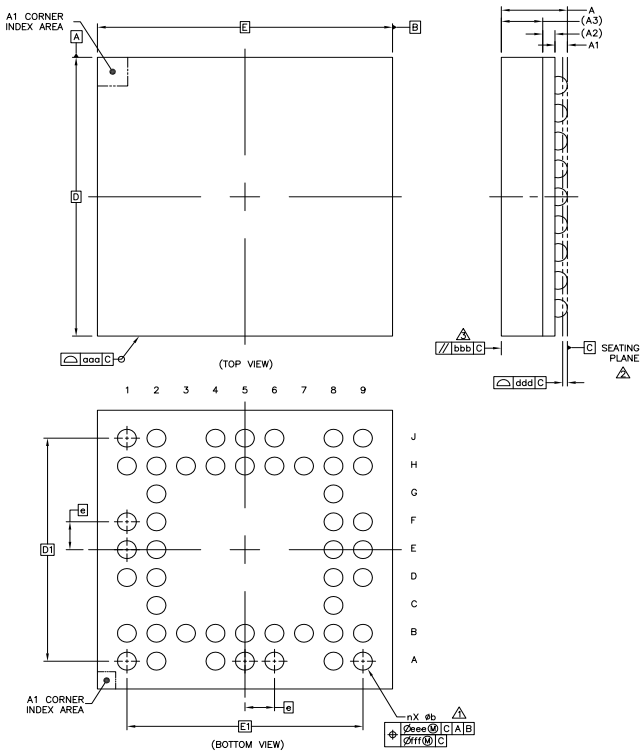
Switching Waveforms



Voltage Waveforms Enable and Disable Times

Switch Positions

Test	Switch
t_{PLZ}, t_{PZL} (output on B-side)	$2*V_{DD}$
t_{PHZ}, t_{PZH} (output on B-side)	GND
Prop Delay	Open



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.1
STAND OFF	A1	0.16	---	0.26
SUBSTRATE THICKNESS	A2		0.21	REF
MOLD THICKNESS	A3		0.54	REF
BODY SIZE	D		5	BSC
	E		5	BSC
BALL DIAMETER			0.3	
BALL OPENING			0.275	
BALL WIDTH	b	0.27	---	0.37
BALL PITCH	e		0.5	BSC
BALL COUNT	n		48	
EDGE BALL CENTER TO CENTER	D1		4	BSC
	E1		4	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

Notes:
1. Controlling dimensions in millimeters
2. Ref: JEDEC MO-195C

PERICOM Enabling Serial Connectivity

DATE: 07/15/11

DESCRIPTION: 48-Pin, Thin Fine Pitch Ball Grid Array TFBGA

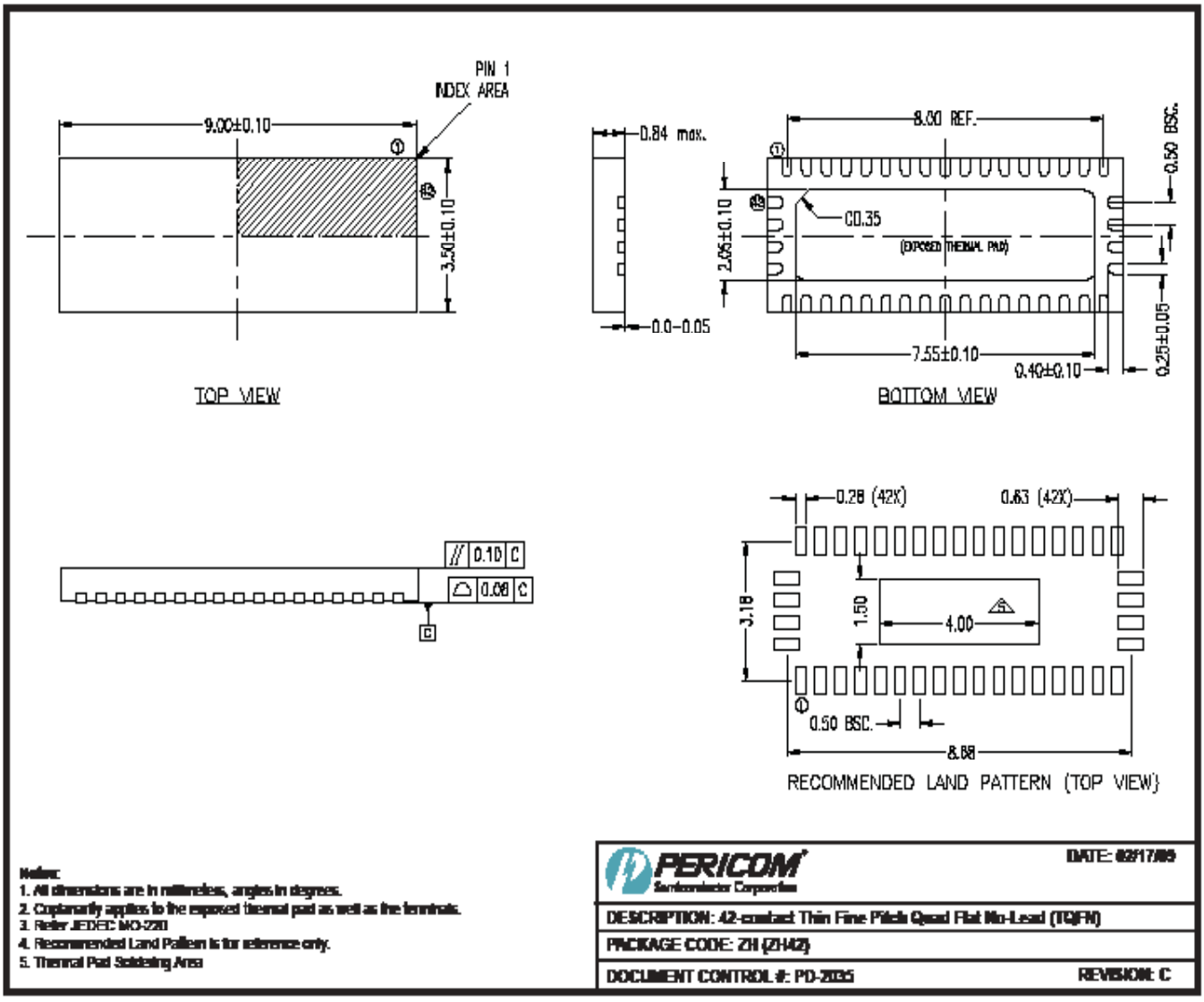
PACKAGE CODE: NE48

DOCUMENT CONTROL #: PD-2101 **REVISION: --**

12-0332

Note:

For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php



Note:

For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Code	Package Code	Package Description
PI3VDP12412ZHE	ZH	Pb-free & Green, 42-contact TQFN
PI3VDP12412NEE	NE	Pb-free & Green, 48-ball BGA

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging

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