

PI6C20400B

1:4 Clock Driver for Intel PCIe® 3.0 Chipsets

Features

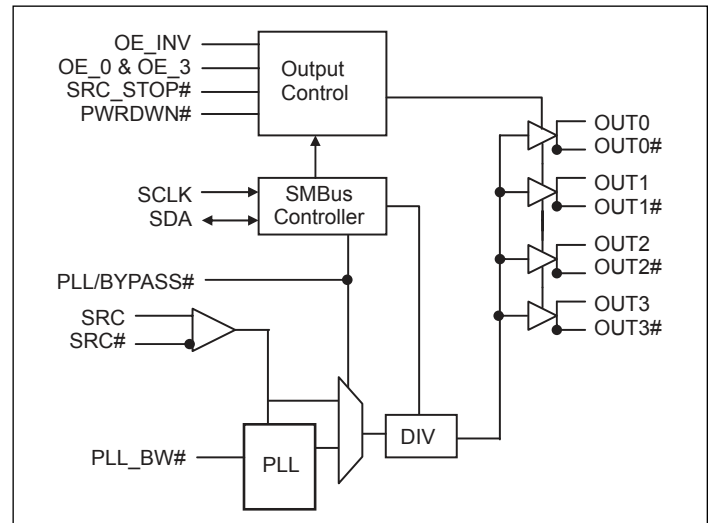
- Phase jitter filter for PCIe 3.0 application
- Four Pairs of Differential Clocks
- Low skew < 50ps
- Low jitter < 50ps cycle-to-cycle
- < 1 ps additive RMS phase jitter
- Output Enable for all outputs
- Outputs tristate control via SMBus
- Programmable PLL Bandwidth
- 100 MHz PLL Mode operation
- 100 - 400 MHz Bypass Mode operation
- 3.3V Operation
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/contact-us) or your local Diodes representative.
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free and Green):
 - 28-Pin, SSOP (H28)
 - 28-Pin, TSSOP (L28)

Description

The PI6C20400B is a PCIe 3.0 compliant high-speed, low-noise differential clock buffer designed to be companion to PCIe 3.0 clock generator. It is backward compatible with PCIe 1.0 and 2.0 specification.

The device distributes the differential SRC clock from PCIe 3.0 clock generator to four differential pairs of clock outputs either with or without PLL. The clock outputs are controlled by input selection of SRC_STOP#, PWRDWN# and SMBus, SCLK and SDA. When input of either SRC_STOP# or PWRDWN# is low, the output clocks are Tristated. When PWRDWN# is low, the SDA and SCLK inputs must be Tri-stated.

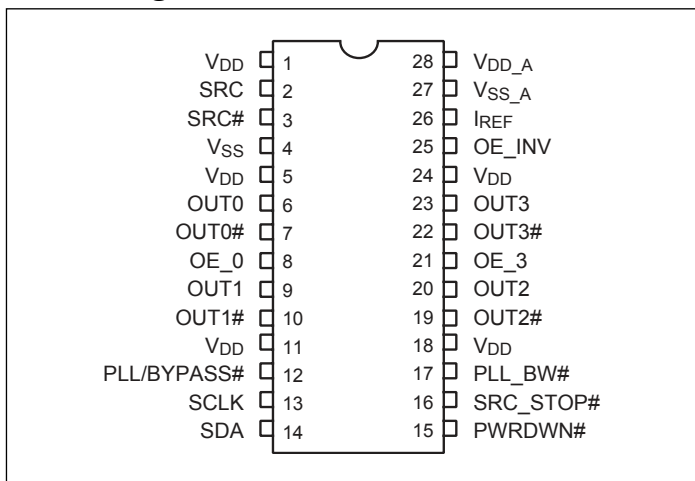
Block Diagram



Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
2, 3	SRC & SRC#	Input	0.7V Differential SRC input from PI6C410 clock synthesizer
8, 21	OE_0 & OE_3	Input	3.3V LVTTTL input for enabling outputs, active high. OE_0 for OUT0 / OUT0# OE_3 for OUT3 / OUT3#
25	OE_INV	Input	3.3V LVTTTL input for inverting the OE, SRC_STOP# and PWRDWN# pins. When 0 = same stage When 1 = OE_0, OE_3, SRC_STOP#, PWRDWN# inverted.
6, 7, 9, 10, 19, 20, 22, 23	OUT[0:3] & OUT[0:3]#	Output	0.7V Differential outputs
12	PLL/BYPASS#	Input	3.3V LVTTTL input for selecting fan-out of PLL operation.
13	SCLK	Input	SMBus compatible SCLOCK input
14	SDA	I/O	SMBus compatible SDATA
26	IREF	Input	External resistor connection to set the differential output current
16	SRC_STOP#	Input	3.3V LVTTTL input for SRC stop, active low
17	PLL_BW#	Input	3.3V LVTTTL input for selecting the PLL bandwidth
15	PWRDWN#	Input	3.3V LVTTTL input for Power Down operation, active low
1, 5, 11, 18, 24	V _{DD}	Power	3.3V Power Supply for Outputs
4	V _{SS}	Ground	Ground for Outputs
27	V _{SS_A}	Ground	Ground for PLL
28	V _{DD_A}	Power	3.3V Power Supply for PLL

Serial Data Interface (SMBus)

This part is a slave only SMBus device that supports indexed block read and indexed block write protocol using a single 7-bit address and read/write bit as shown below.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	1	1	0	0/1

Data Protocol

1 bit	7 bits	1	1	8 bits	1	8 bits	1	8 bits	1	...	8 bits	1	1 bit
Start bit	Slave Addr	R/W	Ack	Register offset	Ack	Byte Count = N	Ack	Data Byte 0	Ack	...	Data Byte N - 1	Ack	Stop bit

Notes:

1. Register offset for indicating the starting register for indexed block write and indexed block read. Byte Count in write mode cannot be 0.

Data Byte 0: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Source Pin
0	Outputs Mode 0 = Divide by 2 1 = Normal	RW	1 = Normal	OUT[0:3], OUT[0:3]#	NA
1	PLL/BYPASS# 0 = Fanout 1 = PLL	RW	1 = PLL	OUT[0:3], OUT[0:3]#	NA
2	PLL Bandwidth 0 = High Bandwidth, 1 = Low Bandwidth	RW	1 = Low	OUT[0:3], OUT[0:3]#	NA
3	Reserved				NA
4	Reserved				NA
5	Reserved				NA
6	SRC_STOP# 0 = Driven when stopped 1 = Tristate	RW	0 = Driven when stopped	OUT[0:3], OUT[0:3]#	NA
7	PWRDWN# 0 = Driven when stopped 1 = Tristate	RW	0 = Driven when stopped	OUT[0:3], OUT[0:3]#	NA

PI6C20400B

Data Byte 1: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Source Pin
0	Reserved				NA
1	OUTPUTS enable	RW	1 = Enabled	OUT0, OUT0#	NA
2	1 = Enabled 0 = Disabled	RW	1 = Enabled	OUT1, OUT1#	NA
3	Reserved				NA
4	Reserved				NA
5	OUTPUTS enable	RW	1 = Enabled	OUT2, OUT2#	NA
6	1 = Enabled 0 = Disabled	RW	1 = Enabled	OUT3, OUT3#	NA
7	Reserved				NA

Data Byte 2: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Source Pin
0	Reserved				NA
1	Allow control of OUTPUTS with assertion of SRC_STOP#	RW	0 = Free running	OUT0, OUT0#	NA
2	0 = Free running 1 = Stopped with SRC_Stop#	RW	0 = Free running	OUT1, OUT1#	NA
3	Reserved				NA
4	Reserved				NA
5	Allow control of OUTPUTS with assertion of SRC_STOP#	RW	0 = Free running	OUT2, OUT2#	NA
6	0 = Free running 1 = Stopped with SRC_Stop#	RW	0 = Free running	OUT3, OUT3#	NA
7	Reserved				NA

PI6C20400B

Data Byte 3: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Source Pin
0	Reserved	RW			
1		RW			
2		RW			
3		RW			
4		RW			
5		RW			
6		RW			
7		RW			

Data Byte 3: Control Register

Bit	Descriptions	Type	Power Up Condition	Output(s) Affected	Pin
0	Pericom ID	R	0	NA	NA
1		R	0	NA	NA
2		R	0	NA	NA
3		R	0	NA	NA
4		R	0	NA	NA
5		R	1	NA	NA
6		R	0	NA	NA
7		R	0	NA	NA

Functionality

PWRDWN#	OUT	OUT#	SRC_Stop#	OUT	OUT#
1	Normal	Normal	1	Normal	Normal
0	$I_{REF} \times 2$ or Float	Low	0	$I_{REF} \times 6$ or Float	Low

Power Down (PWRDWN# assertion)

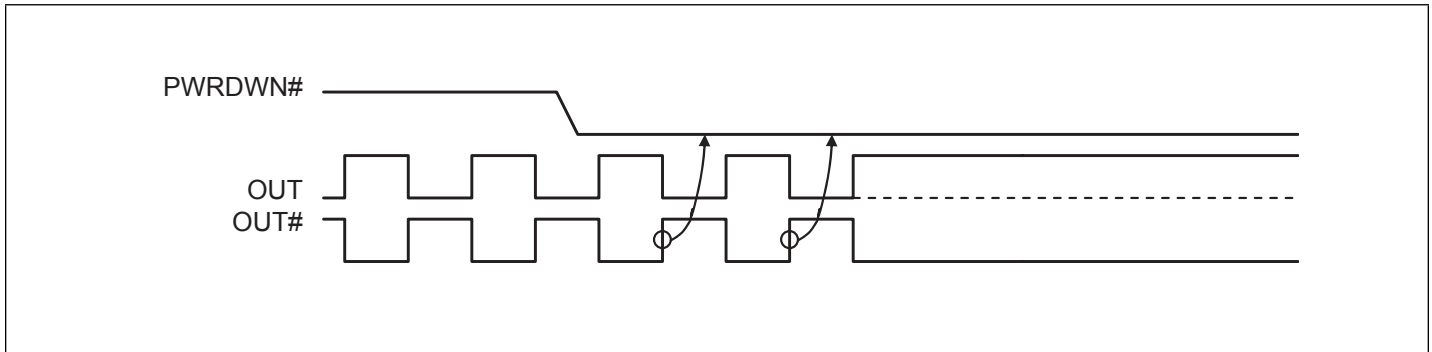


Figure 1. Power down sequence

Power Down (PWRDWN# De-assertion)

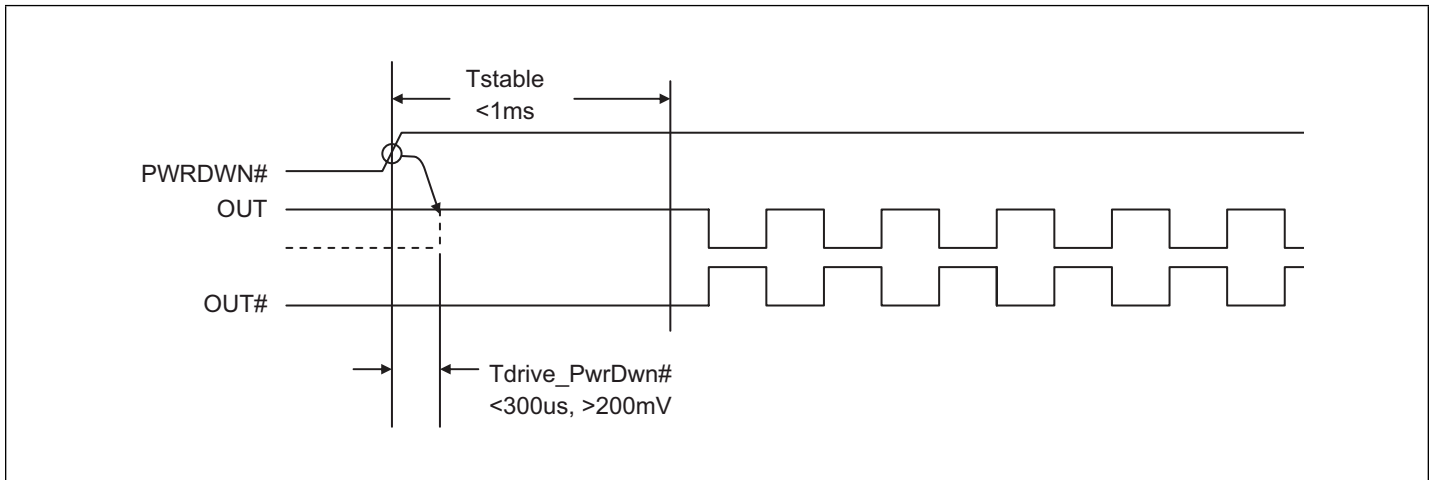
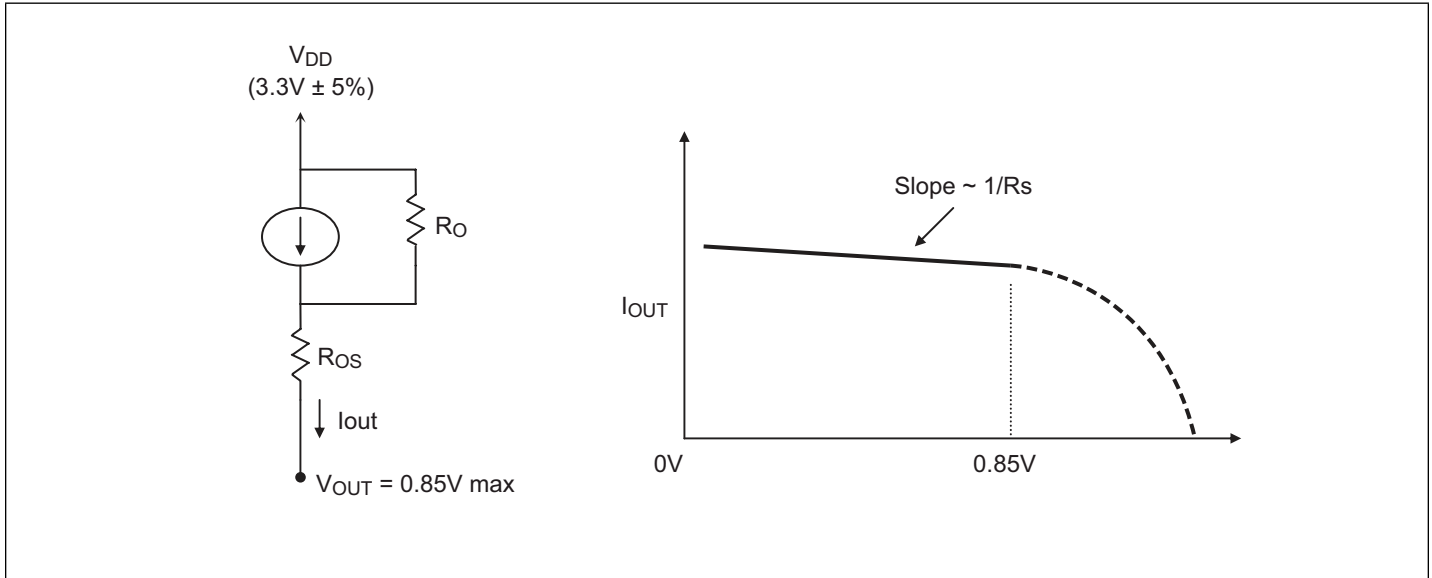


Figure 2. Power down de-assert sequence

Current-mode output buffer characteristics of OUT[0:3], OUT[0:3]#



Differential Clock Buffer characteristics

Symbol	Minimum	Maximum
R_O	3000Ω	N/A
R_{OS}	unspecified	unspecified
V_{OUT}	N/A	850mV

Current Accuracy

Symbol	Conditions	Configuration	Load	Min.	Max.
I_{OUT}	$V_{DD} = 3.30 \pm 5\%$	$R_{REF} = 475\Omega$ 1% $I_{REF} = 2.32mA$	Nominal test load for given configuration	-12% $I_{NOMINAL}$	+12% $I_{NOMINAL}$

Note:

- $I_{NOMINAL}$ refers to the expected current based on the configuration of the device.

Differential Clock Output Current

Board Target Trace/Term Z	Reference R, $I_{ref} = V_{DD}/(3xRr)$	Output Current	$V_{OH} @ Z$
100Ω (100Ω differential ≈ 15% coupling ratio)	$R_{REF} = 475\Omega$ 1%, $I_{REF} = 2.32mA$	$I_{OH} = 6 \times I_{REF}$	0.7V @ 50

Absolute Maximum Ratings (Over operating free-air temperature range)

Symbol	Parameters	Min.	Max.	Units
V_{DD_A}	3.3V Core Supply Voltage	-0.5	4.6	V
V_{DD}	3.3V I/O Supply Voltage	-0.5	4.6	
V_{IH}	Input High Voltage		4.6	
V_{IL}	Input Low Voltage	-0.5		
T_s	Storage Temperature	-65	150	°C
V_{ESD}	ESD Protection	2000		V
T_J	Junction Temperature		125	°C

Note:

- Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

DC Electrical Characteristics ($V_{DD} = 3.3 \pm 5\%$, $V_{DD_A} = 3.3 \pm 5\%$)

Symbol	Parameters	Condition	Min.	Max.	Units
V_{DD_A}	3.3V Core Supply Voltage		3.135	3.465	V
V_{DD}	3.3V I/O Supply Voltage		3.135	3.465	
V_{IH}	3.3V Input High Voltage	V_{DD}	2.0	$V_{DD} + 0.3$	
V_{IL}	3.3V Input Low Voltage		$V_{SS} - 0.3$	0.8	
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{DD}$	-5	+5	μA
V_{OH}	3.3V Output High Voltage	$I_{OH} = -1mA$	2.4		V
V_{OL}	3.3V Output Low Voltage	$I_{OL} = 1mA$		0.4	
I_{OH}	Output High Current	$I_{OH} = 6 \times I_{REF}$ $I_{REF} = 2.32mA$	12.2	15.6	mA
C_{IN}	Input Pin Capacitance		3	5	
C_{OUT}	Output Pin Capacitance			6	pF
L_{PIN}	Pin Inductance			7	
$I_{DD(BYPASS)}$	Power Supply Current (PLL Bypass)	$V_{DD} = 3.465V$, $F_{CPU} = 100MHz$		90	mA
I_{DD}	Power Supply Current	$V_{DD} = 3.465V$	Bypass mode	100	
		$F_{CPU} = 100MHz$	PLL mode	130	
I_{SS}	Power Down Current	Driven outputs		40	
I_{SS}	Power Down Current	Tristate outputs		12	
T_A	Ambient Temperature		-40	85	°C

AC Switching Characteristics ($V_{DD} = 3.3 \pm 5\%$, $V_{DD,A} = 3.3 \pm 5\%$)

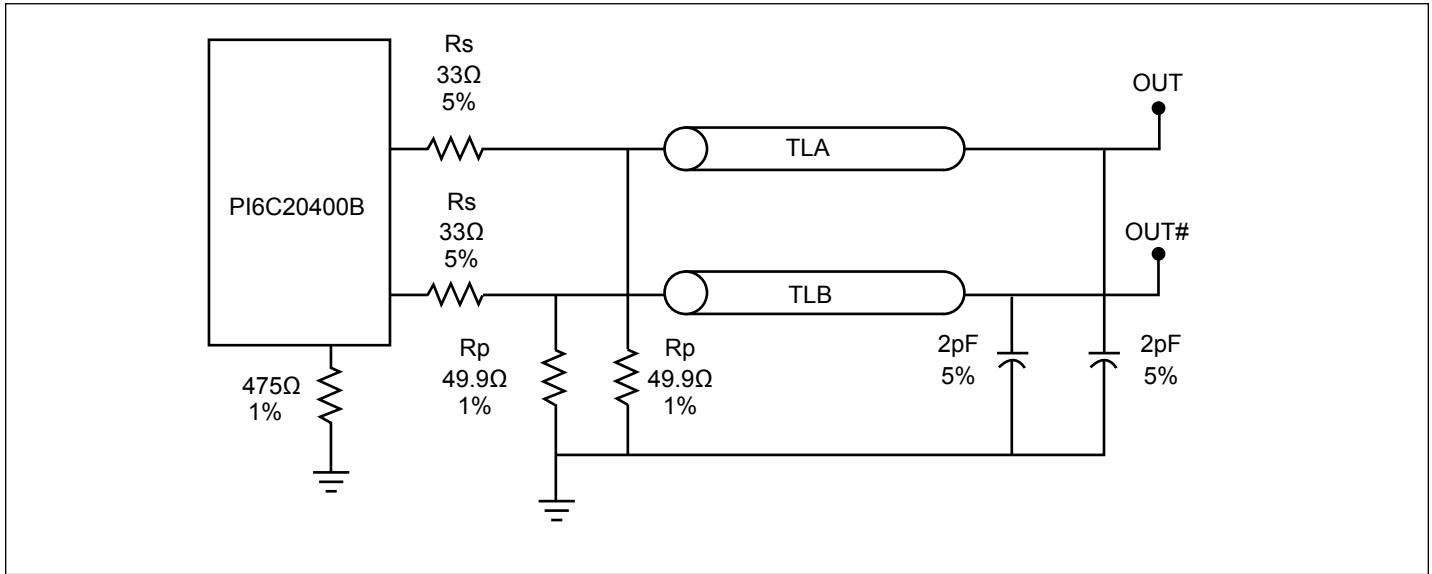
Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
F_{IN}	PLL Mode		95		105	MHz
	Bypass Mode		100		400	MHz
T_{rise} / T_{fall}^2	Rise and Fall Time (measured between 0.175V to 0.525V)		175		700	ps
DT_{rise} / DT_{fall}^2	Rise and Fall Time Variation				125	ps
T_{pd}	PLL Mode				± 250	ps
	Non-PLL Mode		2.5		6.5	ns
$T_{jitter}^{3,4}$	Cycle – Cycle Jitter				50	ps
V_{HIGH}^2	Voltage High including overshoot		660		1150	mV
V_{LOW}^2	Voltage Low including undershoot		-300			mV
V_{cross}^2	Absolute crossing point voltages		250		550	mV
DV_{cross}^2	Total Variation of Vcross over all edges				140	mV
T_{DC}^3	Duty Cycle		45		55	%
$t_{jphPCIEG1}$	Phase Jitter, PLL Mode	PCIe Gen1		30	86	ps (p-p)
$t_{jphPCIEG2}$		PCIE_2_0_8MHz_1_5M_H3_STEP, Low Freq.	0.7	3	ps (rms)	
		PCIE_2_0_8MHz_1_5M_H3_STEP, High Freq.	2	3.1		
$t_{jphPCIEG3}$		PCIE_3_0_2MHz_5M_H3_FIRST, Low Freq.	2	3		
		PCIE_3_0_2MHz_5M_H3_FIRST, High Freq.	0.47	1		
$t_{jphPCIEG1}$	Additive Phase Jitter, Bypass Mode	PCIe Gen1		0		0.001
$t_{jphPCIEG2}$		PCIE_2_0_8MHz_1_5M_H3_FIRST, Low Freq.	0	0.001	ps (rms)	
		PCIE_2_0_8MHz_1_5M_H3_FIRST, High Freq.	0	0.001		
$t_{jphPCIEG3}$		PCIE_3_0_2MHz_5M_H3_FIRST, Low Freq.	0	0.001		
		PCIE_3_0_2MHz_5M_H3_FIRST, High Freq.	0	0.001		

Notes:

1. Test configuration is $R_s = 33.2\Omega$, $R_p = 49.9\Omega$, and 2pF.
2. Measurement taken from Single Ended waveform.
3. Measurement taken from Differential waveform.
4. Measurement taken using M1 data capture analysis tool.
5. Additive jitter is calculated from input and output RMS phase jitter by using PCIe 2.0 filter. ($T_{jadd} = \sqrt{(\text{output jitter})^2 - (\text{input jitter})^2}$)

PI6C20400B

Configuration Test Load Board Termination



Part Marking

L Package



Y: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

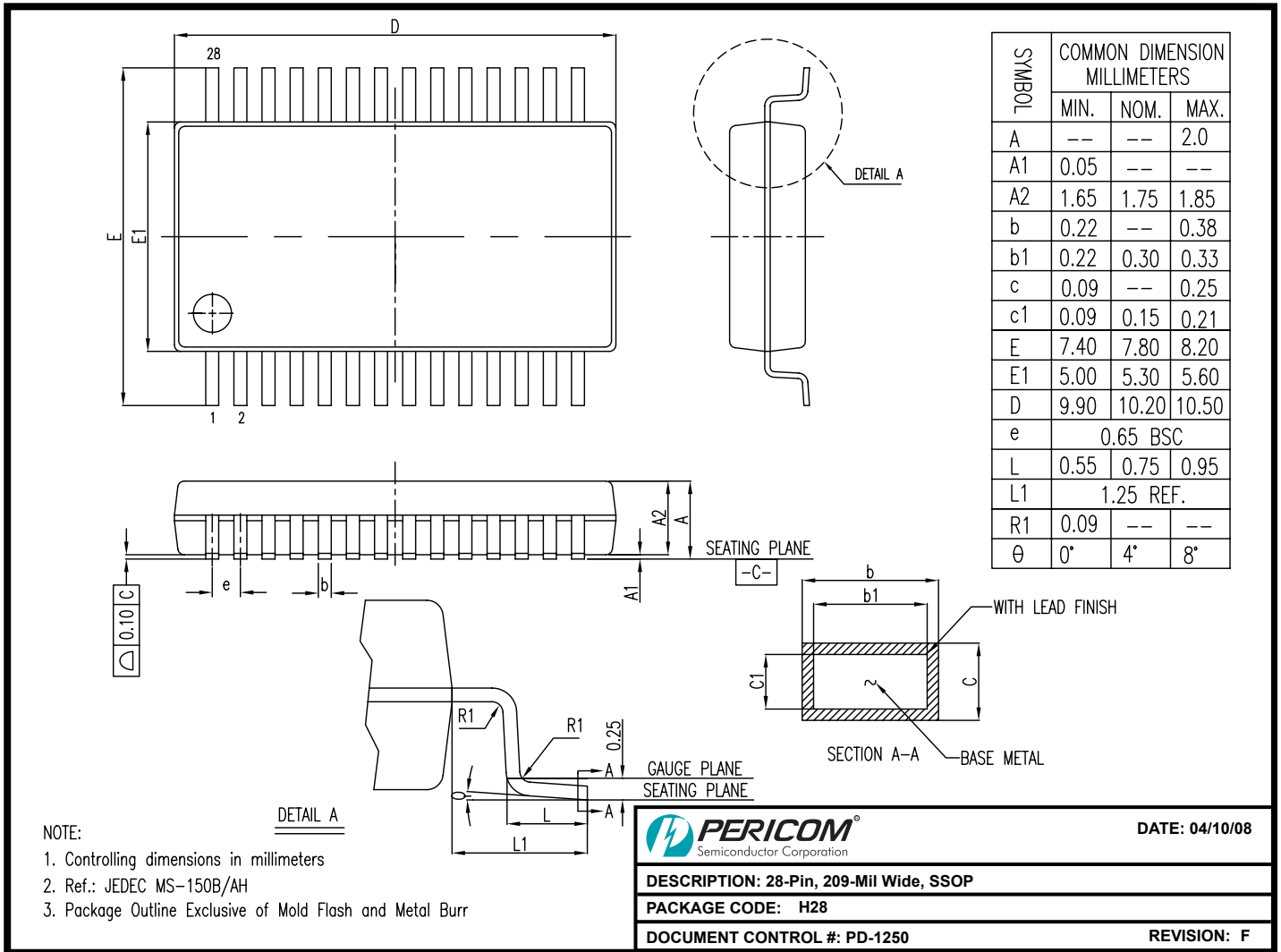
H Package



Y: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

PI6C20400B

Packaging Mechanical: 28-SSOP (H)



08-0143

PI6C20400B

Packaging Mechanical: 28-TSSOP (L)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
 1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
 2. JEDEC MO-153F
 3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	DATE: 03/31/16
DESCRIPTION: 28-Pin, 173mil Wide TSSOP	
PACKAGE CODE: L (L28)	
DOCUMENT CONTROL #: PD-1313	REVISION: F

16-0076

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Ordering Code	Package Code	Package Description
PI6C20400BHEX	H	28-pin, 209-mil wide (SSOP)
PI6C20400BLEX	L	28-pin, 173-mil wide (TSSOP)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

IMPORTANT NOTICE

1. DIODES INCORPORATED AND ITS SUBSIDIARIES (“DIODES”) MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes products. Diodes products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of the Diodes products for their intended applications, (c) ensuring their applications, which incorporate Diodes products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes’ websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes’ website) under this document.

5. Diodes products are provided subject to Diodes’ Standard Terms and Conditions of Sale (<https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/>) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

Copyright © 2021 Diodes Incorporated

www.diodes.com

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [Clock Buffer](#) category:

Click to view products by [Diodes Incorporated](#) manufacturer:

Other Similar products are found below :

[MPC962309EJ-1H](#) [NB4N121KMNG](#) [IDT49FCT805ASO](#) [MK2308S-1HILF](#) [PL133-27GI-R](#) [NB3L02FCT2G](#) [NB3L03FCT2G](#)
[ZL40200LDG1](#) [ZL40205LDG1](#) [9FG1200DF-1LF](#) [9FG1001BGLF](#) [PI49FCT20802QE](#) [PI6C10810HE](#) [NB7L1008MNG](#) [NB7L14MN1G](#)
[PI49FCT20807QE](#) [PI6C4931502-04LIEX](#) [ZL80002QAB1](#) [PI6C4931504-04LIEX](#) [PI6C10806BLEX](#) [ZL40226LDG1](#) [8T73S208B-01NLGI](#)
[SY75578LMG](#) [PI49FCT32805QEX](#) [PL133-27GC-R](#) [MC10LVEP11DG](#) [MC10EP11DTG](#) [MC100LVEP11DG](#) [MC100E111FNG](#)
[MC100EP11DTG](#) [NB7L14MMNG](#) [NB6L14MMNR2G](#) [NB6L611MNG](#) [NB7V58MMNHTBG](#) [NB3N111KMNR4G](#) [ADCLK944BCPZ-R7](#)
[ZL40217LDG1](#) [NB7LQ572MNG](#) [HMC940LC4BTR](#) [9DB801BGLF](#) [ADCLK946BCPZ-REEL7](#) [ADCLK946BCPZ](#) [ADCLK905BCPZ-R2](#)
[ADCLK905BCPZ-R7](#) [ADCLK907BCPZ-R2](#) [ADCLK907BCPZ-WP](#) [ADCLK914BCPZ-R2](#) [ADCLK914BCPZ-R7](#) [ADCLK925BCPZ-R2](#)
[ADCLK925BCPZ-R7](#)