

## 3.3V Low Jitter 1-to-4 Crystal/LVCMOS to LVPECL Fanout Buffer

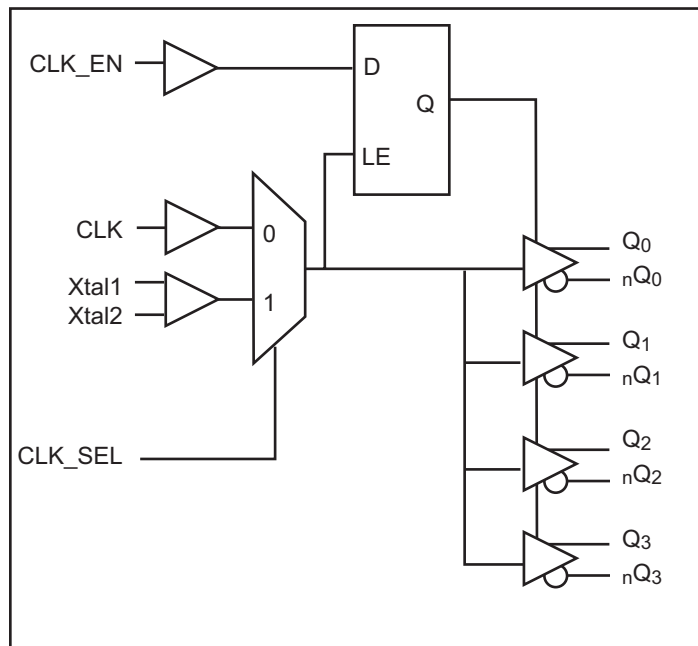
### Features

- Maximum output frequency: 500MHz
- 4 pair of differential LVPECL outputs
- Selectable CLK and crystal inputs
- CLK accepts LVCMOS, LVTTTL input level
- Ultra low additive phase jitter: < 0.05 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Output Skew: 30ps (maximum)
- Part-to-part skew: 200ps (maximum)
- Propagation delay: 1.5ns (maximum)
- 3.3V power supply
- Pin-to-pin compatible to ICS8535-11, ICS8535-31
- Operating Temperature: -40°C to 85°C
- Packaging (Pb-free & Green available):  
- 20-pin TSSOP (L)

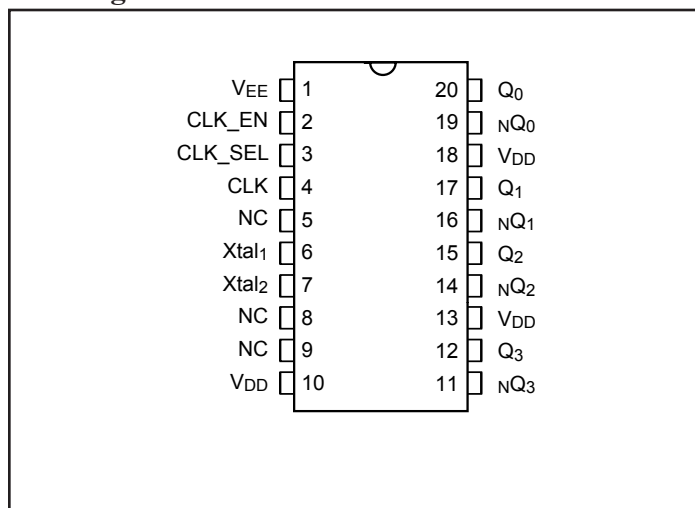
### Description

The PI6C48535-11B is a high-performance low jitter and low-skew LVPECL fanout buffer. PI6C48535-11B features selectable of single-ended clock or crystal inputs and translates to four LVPECL outputs. The CLK input accepts LVCMOS or LVTTTL signals. The outputs are synchronized with input clock during asynchronous assertion /deassertion of CLK\_EN pin. PI6C48535-11B is ideal for crystal or LVCMOS/LVTTTL to LVPECL translation. Typical clock translation and distribution applications are data-communications and telecommunications.

### Block Diagram



### Pin Diagram



### Pin Description

Name	Pin #	Type	Description
V <sub>EE</sub>	1	P	Connect to Negative power supply
CLK_EN	2	I_PU	Synchronizing clock enable. When high, clock outputs follow clock input. When low, Q <sub>x</sub> outputs are forced low, <sub>n</sub> Q <sub>x</sub> outputs are forced high. LVCMOS/LVTTL level with 50KΩ pull up.
CLK_SEL	3	I_PD	Clock select input. When high, selects Xtal (Xtal1, Xtal2) inputs. When low, selects CLK input. LVCMOS/LVTTL level with 50KΩ pull down.
CLK	4	I_PD	LVCMOS / LVTTL clock input
Xtal1, Xtal2	6, 7		Crystal input and output
NC	5, 8, 9		No internal connection.
V <sub>DD</sub>	10, 13, 18	P	Connect to 3.3V
Q <sub>3</sub> , <sub>n</sub> Q <sub>3</sub>	11, 12	O	Differential output pair, LVPECL interface level.
Q <sub>2</sub> , <sub>n</sub> Q <sub>2</sub>	14, 15	O	Differential output pair, LVPECL interface level.
Q <sub>1</sub> , <sub>n</sub> Q <sub>1</sub>	16, 17	O	Differential output pair, LVPECL interface level.
Q <sub>0</sub> , <sub>n</sub> Q <sub>0</sub>	19, 20	O	Differential output pair, LVPECL interface level.

**Notes:**

1. I = Input, O = Output, P = Power supply connection, I\_PD = Input with pull down, I\_PU = Input with pull up

### Pin Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C <sub>IN</sub>	Input Capacitance				4	pF
R <sub>pullup</sub>	Input Pullup Resistance			50		KΩ
R <sub>pulldown</sub>	Input Pulldown Resistance			50		KΩ

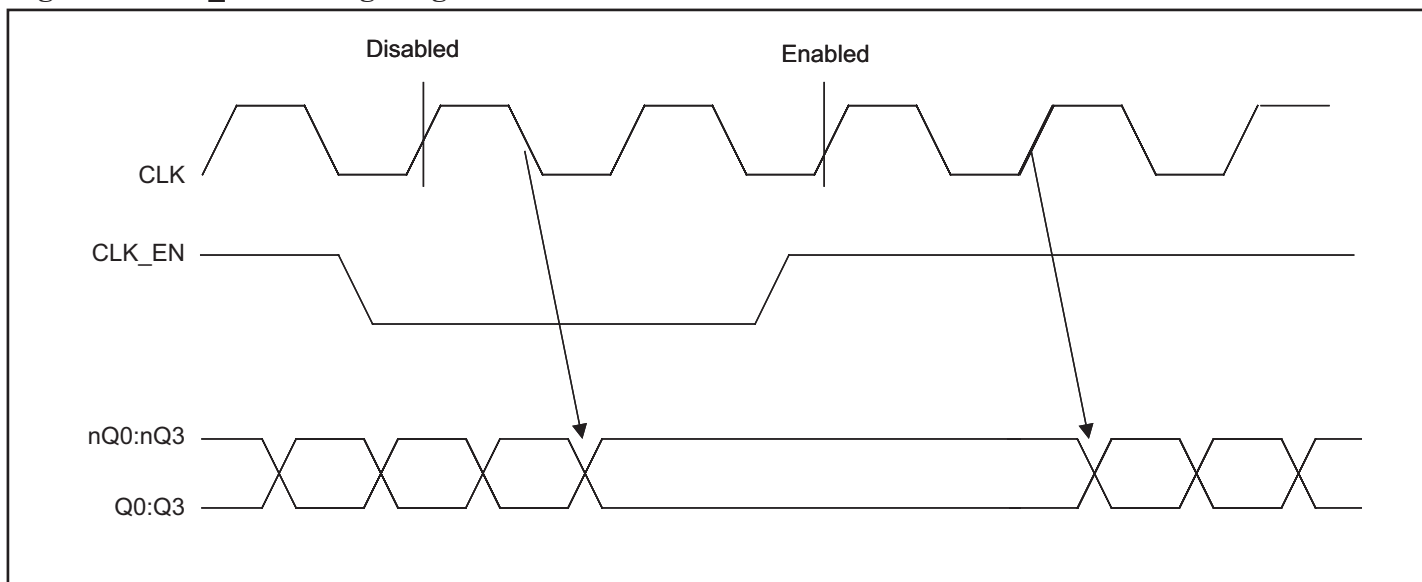
### Control Input Function Table

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q <sub>0</sub> :Q <sub>3</sub>	<sub>n</sub> Q <sub>0</sub> : <sub>n</sub> Q <sub>3</sub>
0	0	CLK	Disabled: Low	Disabled: High
0	1	Xtal1, Xtal2	Disabled: Low	Disabled: High
1	0	CLK	Enabled	Enabled
1	1	Xtal1, Xtal2	Enabled	Enabled

**Notes:**

1. After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show below.

**Figure 1. CLK\_EN Timing Diagram**



**Clock Input Function Table**

Inputs	Outputs	
CLK	Q0:Q3	nQ0:nQ3
0	LOW	HIGH
1	HIGH	LOW

**Absolute Maximum Ratings**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V <sub>DD</sub>	Supply voltage	Referenced to GND			4.6	V
V <sub>IN</sub>	Input voltage	Referenced to GND	-0.5		V <sub>DD</sub> +0.5V	
V <sub>OUT</sub>	Output voltage	Referenced to GND	-0.5		V <sub>DD</sub> +0.5V	
T <sub>STG</sub>	Storage temperature		-65		150	°C

**Notes:**

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**Operating Conditions**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V <sub>DD</sub>	Power Supply Voltage		3.135	3.3	3.465	V
T <sub>A</sub>	Ambient Temperature		-40		85	°C
I <sub>DD</sub>	Power Supply Current	All outputs unloaded			130	mA

**LVCMOS/LVTTL DC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 5\%$  unless otherwise stated below.)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
$V_{IH}$	Input High Voltage			2		$V_{DD}+0.3$	V
$V_{IL}$	Input Low Voltage			-0.3		0.8	
$I_{IH}$	Input High Current	CLK, CLK_SEL	$V_{IN} = V_{DD} = 3.3\text{V}$			150	$\mu\text{A}$
		CLK_EN	$V_{IN} = V_{DD} = 3.3\text{V}$			10	
$I_{IL}$	Input Low Current	CLK, CLK_SEL	$V_{IN} = 0\text{V}, V_{DD} = 3.3\text{V}$	-10			
		CLK_EN	$V_{IN} = 0\text{V}, V_{DD} = 3.3\text{V}$	-150			

**LVPECL DC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{V}$  unless otherwise stated below.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{OH}$	Output High Voltage		2.1		2.6	V
$V_{OL}$	Output Low Voltage		1.3		1.8	

**Crystal Characteristics**

Parameter	Min.	Typ.	Max.	Units
Mode of Oscillation	Fundamental			
Frequency Range	12		40	MHz
Equivalent Series Resistance (ESR)			70	$\Omega$
Shunt Capacitance			7	pF

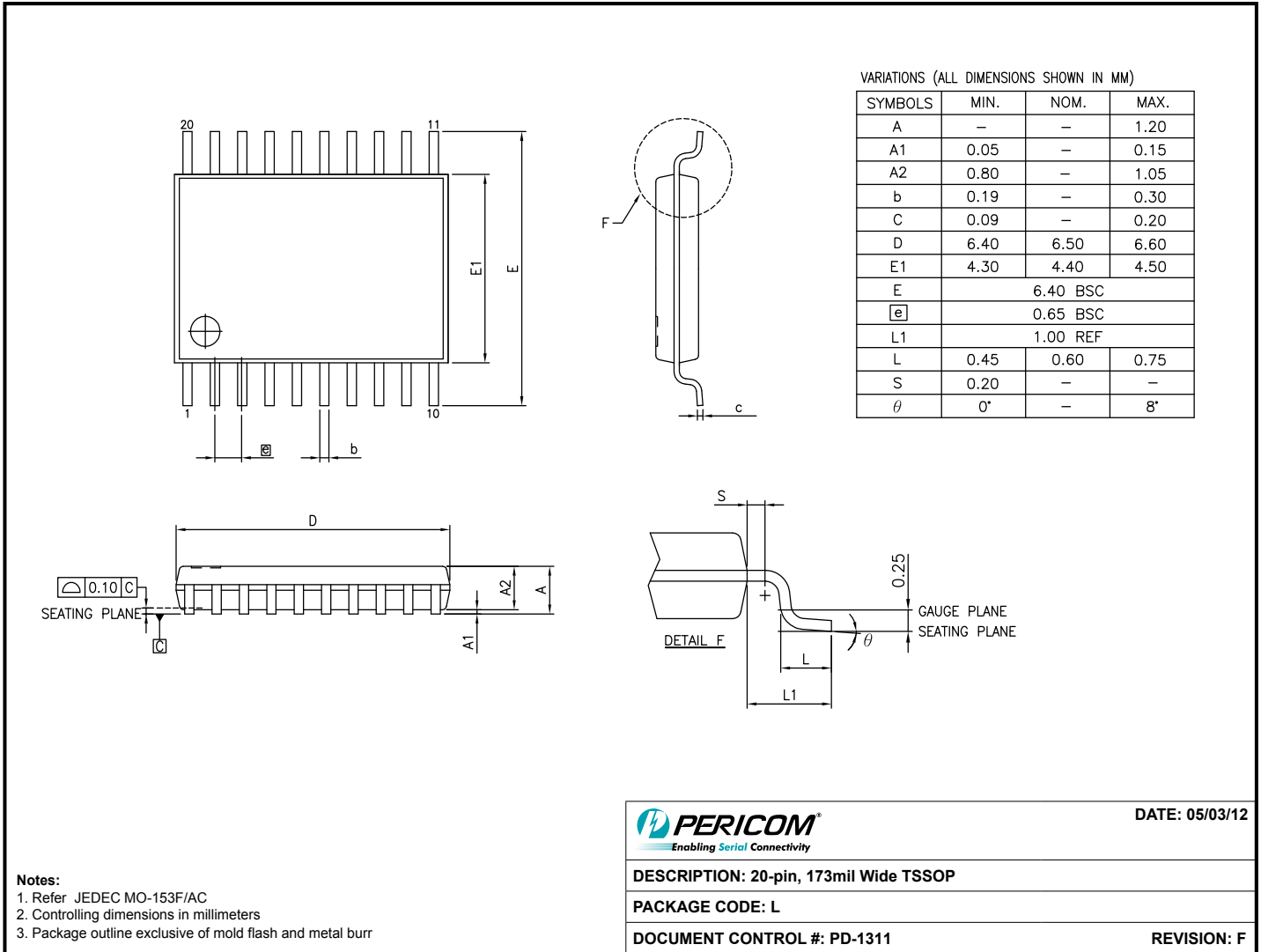
**AC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 5\%$ )

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$f_{max}$	Output Frequency				500	MHz
$t_{jit}$	Buffer Additive Jitter RMS	156.25MHz		0.05		ps
$V_{SWING}$	Peak-to-peak Output Voltage Swing	156.25MHz	0.6		1.1	V
$t_{Pd}$	Propagation Delay <sup>(1) (4)</sup>				1.5	ns
$T_{sk(o)}$	Output-to-output Skew <sup>(2) (4)</sup>				30	ps
$T_{sk(pp)}$	Part-to-part Skew <sup>(3) (4)</sup>				200	
$t_r/t_f$	Output Rise/Fall time <sup>(4)</sup>	20% - 80%	100		400	
odc	Output duty cycle <sup>(4)</sup>		48		52	%
Osc	Crystal Tolerance				1000	ppm

**Notes:**

1. Measured from the  $V_{DD}/2$  of the input to the differential output crossing point
2. Defined as skew between outputs at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
3. Defined as skew between outputs on different parts operating at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
4. All parameters are measured with CMOS input of 266MHz unless stated otherwise

**Packaging Mechanical: 20-Pin TSSOP (L)**



**Ordering Information**

Ordering Code	Package Code	Package Description
PI6C48535-11BLIE	L	Pb-free & Green 20-pin 173-mil wide TSSOP

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)

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