

## High Performance 1:5 LVPECL Fanout Buffer

### Features

- 5 LVPECL outputs
- Up to 1.5GHz output frequency
- Ultra low additive phase jitter: < 0.03 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Two selectable inputs
- Low delay from input to output (Tpd typ. 1.5ns)
- 2.5V/3.3V power supply
- Industrial temperature support
- TSSOP-20 package

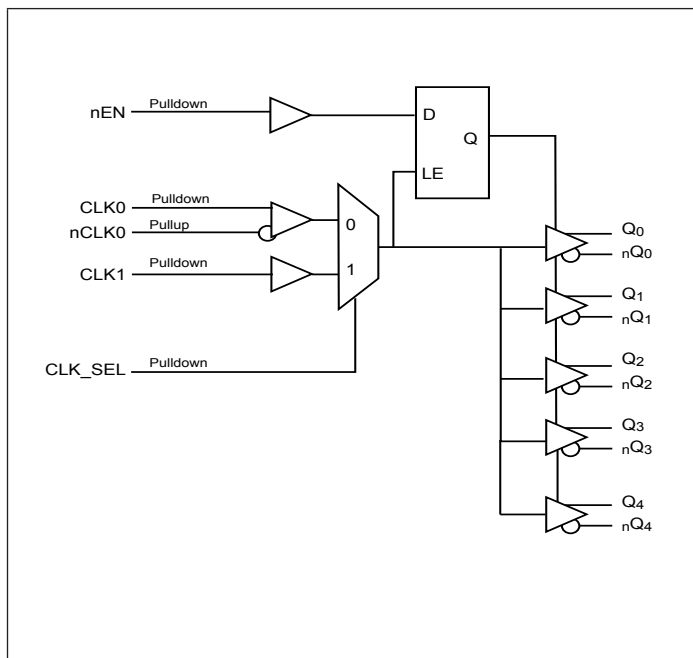
### Description

The PI6C4911505-04 is a high performance fanout buffer device which supports up to 1.5GHz frequency. The device has 2 selectable clock inputs that can accept most differential and single ended clock sources. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

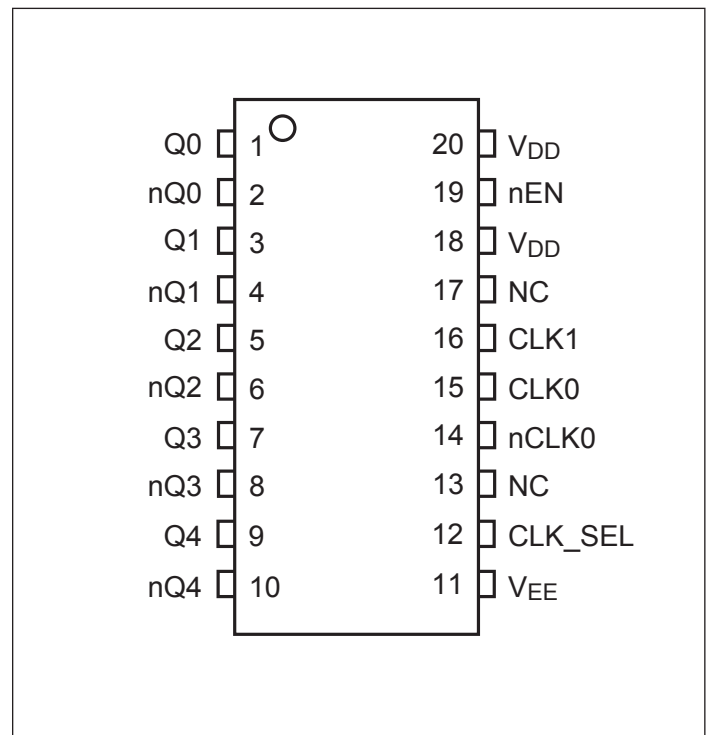
### Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

### Block Diagram



### Pin Configuration (20-Pin TSSOP)



### Pinout Table

Pin #	Pin Name	Type	Description
1, 2	Q0 nQ0	Output	LVPECL output clock
3, 4	Q1 nQ1	Output	LVPECL output clock
5, 6	Q2 nQ2	Output	LVPECL output clock
7, 8	Q3 nQ3	Output	LVPECL output clock
9, 10	Q4 nQ4	Output	LVPECL output clock
11	V <sub>EE</sub>	Power	Negative power supply
12	CLK_SEL	Input	Clock input source selection pin
13, 17	NC	-	No connect
14, 15	CLK0 nCLK0	Input	Differential clock input
16	CLK1	Input	CMOS clock input
18, 20	V <sub>DD</sub>	Power	Power supply
19	nEN	Input	Synchronizing clock enable. When LOW, clock outputs enabled. When HIGH, Q outputs are forced low, nQ outputs forced high.

**Function Table**

Table 1: Input select function

CLK_SEL	Function
0	CLK0, nCLK0
1	CLK1

Table 2: Enable function

nEN	Outputs	
	Q0:Q4	nQ0:nQ4
1	Disabled; LOW	Disabled; HIGH
0	Enabled	Enabled

**Maximum Ratings** (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....	-55 to +150°C
Supply Voltage to Ground Potential ( $V_{DD}$ ).....	-0.5 to +4.6V
Inputs (Referenced to GND) .....	-0.5 to $V_{DD}+0.5V$
Clock Output (Referenced to GND).....	-0.5 to $V_{DD}+0.5V$
Soldering Temperature (Max of 10 seconds) .....	+260°C
Latch up .....	200mA

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Power Supply Characteristics and Operating Conditions**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$V_{DD}$	Core Supply Voltage		3.0	3.3	3.6	V
			2.375	2.5	2.625	
$I_{DD}$	Power Supply Current	All outputs unloaded			150	mA
$T_A$	Ambient Operating Temperature		-40		85	°C

**DC Electrical Specifications - Differential Inputs**

Symbol	Parameter		Min.	Typ.	Max.	Units
$I_{IH}$	Input High current: CLK0, CLK1	Input = $V_{DD}$			150	uA
	Input High current: nCLK0	Input = $V_{DD}$			5	uA
$I_{IL}$	Input Low current: CLK0, CLK1	Input = GND	-5			uA
	Input Low current: nCLK0	Input = GND	-150			uA
$C_{IN}$	Input capacitance			4		PF
$V_{IH}$	Input high voltage				$V_{DD}+0.3$	V
$V_{IL}$	Input low voltage		-0.3			V
$V_{ID}$	Input Differential Amplitude PK-PK		0.15		1.3	V
$V_{CM}$	Common mode input voltage		$V_{EE}+0.5$		$V_{DD}-0.85$	V

**DC Electrical Specifications - LVCMOS Inputs**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I <sub>IH</sub>	Input High current	Input = V <sub>DD</sub>			150	uA
I <sub>IL</sub>	Input Low current	Input = GND	-150			uA
V <sub>IH</sub>	Input high voltage	V <sub>DD</sub> =3.3V	2.0		V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input low voltage	V <sub>DD</sub> =3.3V	-0.3		0.8	V
V <sub>IH</sub>	Input high voltage	V <sub>DD</sub> =2.5V	1.7		V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input low voltage	V <sub>DD</sub> =2.5V	-0.3		0.7	V

**DC Electrical Specifications- LVPECL Outputs**

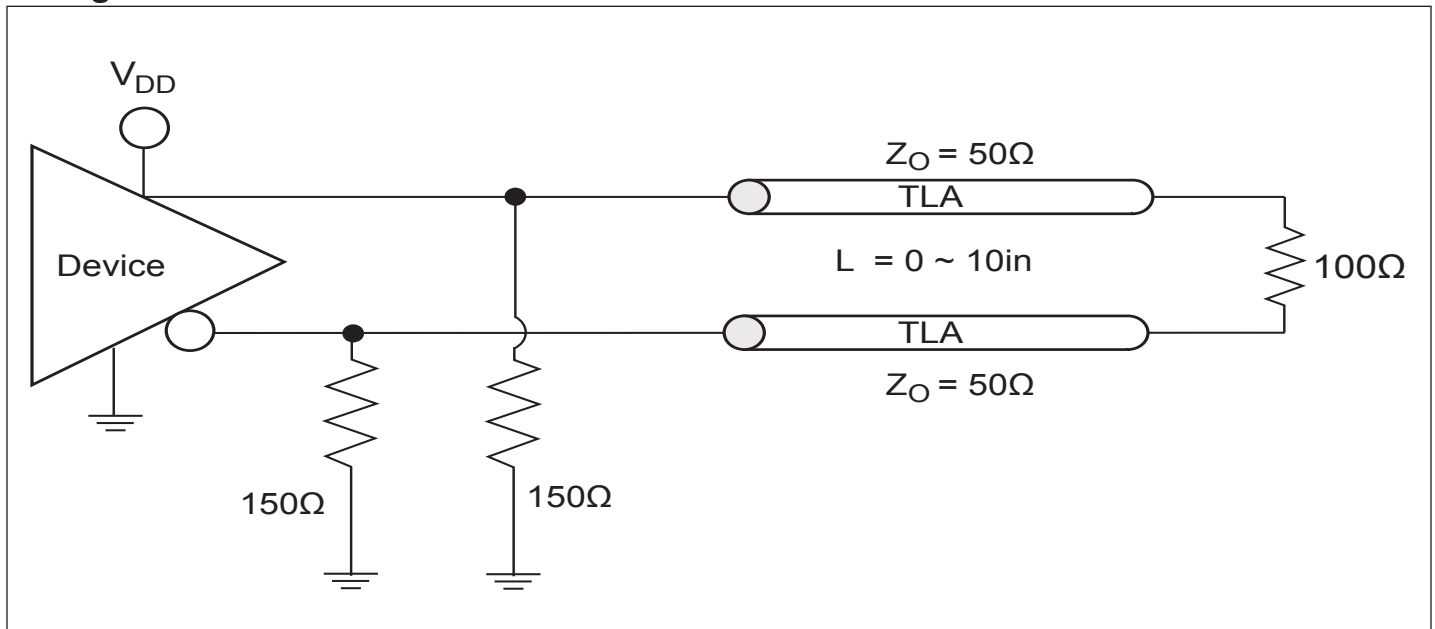
Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V <sub>OH</sub>	Output High voltage	V <sub>DD</sub> =3.3V	2.1		2.6	V
		V <sub>DD</sub> =2.5V	1.3		1.6	
V <sub>OL</sub>	Output Low voltage	V <sub>DD</sub> =3.3V	1.3		1.8	V
		V <sub>DD</sub> =2.5V	0.5		0.8	
V <sub>SWING</sub>	Peak to Peak Output Voltage Swing		0.6		1.1	V

### AC Electrical Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Clock output frequency	CLK0/ nCLK0 input, LVPECL			1500	MHz
		CLK1 input			300	
T <sub>r</sub>	Output rise time	From 20% to 80%		150		ps
T <sub>f</sub>	Output fall time	From 80% to 20%		150		ps
T <sub>ODC</sub>	Output duty cycle	Frequency < 650MHz, LVPECL input	48		52	%
V <sub>PP</sub>	Output swing Single-ended	LVPECL outputs	400			mV
T <sub>j</sub>	Buffer additive jitter RMS			0.03		ps
T <sub>SK</sub>	Output Skew				35	ps
T <sub>PD</sub>	Propagation Delay			1500	2100	ps
T <sub>P2P Skew</sub>	Part to Part Skew <sup>1</sup>				150	ps

1. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions.

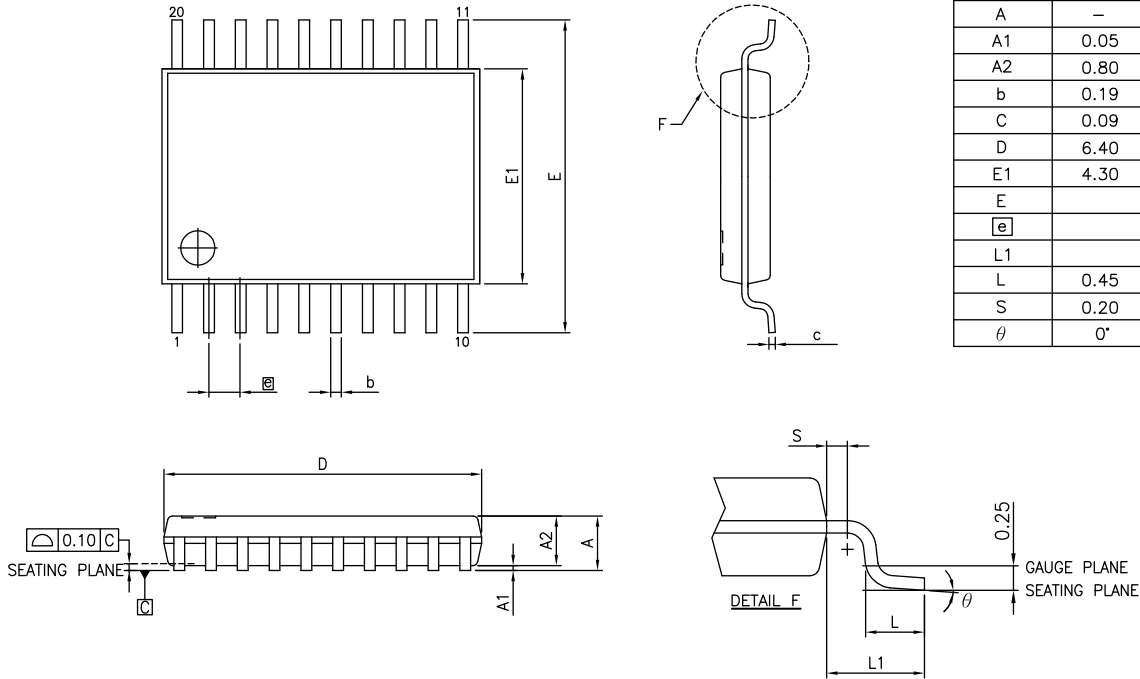
### Configuration Test Load Board Termination for LVPECL



### Packaging Mechanical: 20-Pin TSSOP (L)

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	–	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
$\theta$	0°	–	8°



- Notes:**
- 1. Refer JEDEC MO-153F/AC
  - 2. Controlling dimensions in millimeters
  - 3. Package outline exclusive of mold flash and metal burr

<b>PERICOM</b> Enabling Serial Connectivity	<b>DATE: 05/03/12</b>
<b>DESCRIPTION: 20-pin, 173mil Wide TSSOP</b>	
<b>PACKAGE CODE: L</b>	
<b>DOCUMENT CONTROL #: PD-1311</b>	<b>REVISION: F</b>

### Ordering Information<sup>(1-3)</sup>

Ordering Code	Package Code	Package Description
PI6C4911505-04LIE	L	20-pin, TSSOP, Pb-Free and Green

**Notes:**

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel

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[ADCLK905BCPZ-R7](#) [ADCLK907BCPZ-R2](#) [ADCLK907BCPZ-WP](#) [ADCLK914BCPZ-R2](#) [ADCLK914BCPZ-R7](#) [ADCLK925BCPZ-R2](#)  
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