

High Performance 1:8 Multi-Voltage CMOS Buffer

Features

- 8 single-ended outputs Fanout Buffer
- Up to 200MHz output frequency
- Ultra low output additive jitter = 0.01ps (typ.)
- Selectable reference inputs support Xtal (10~50MHz), single-ended and differential
- Low output skew ~ 50ps (typ.)
- 2.5V / 3.3V operation
- User configurable output VDDO in different banks:
 - Mixed 3.3V core, 2.5V, 1.8V or 1.5V output operating supply
 - Mixed 2.5V core, 1.8V, 1.5V or 1.2V output operating supply
- Industrial temperature range: -40°C to +85°C
- Packaging (Pb-free & Green available):
 - 32-pin TQFN (ZH)

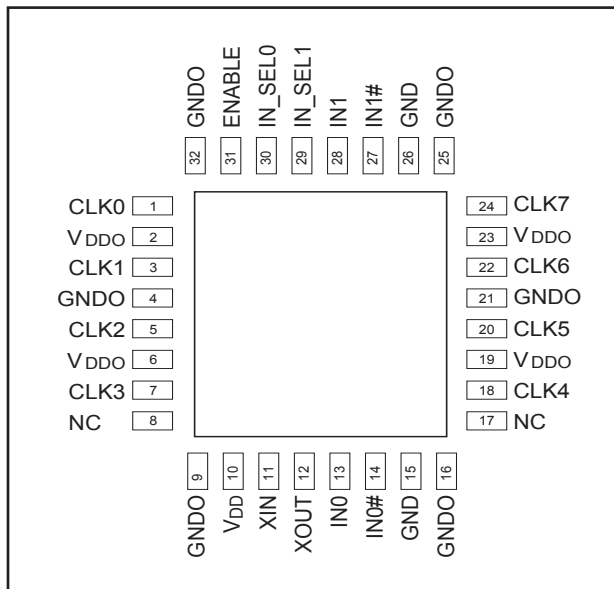
Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

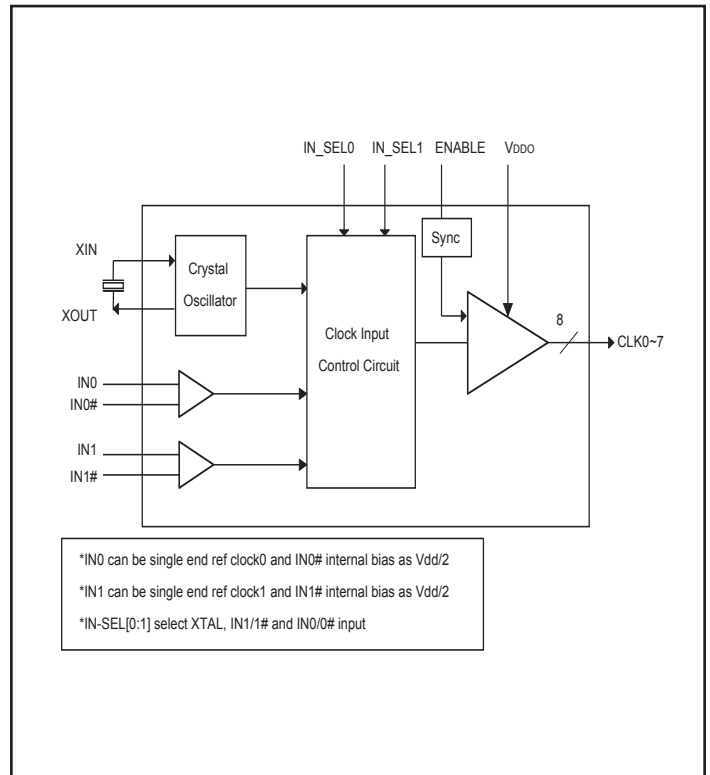
Description

The PI6C49X0208 is a high performance multi-voltage 8-outputs CMOS Fanout Buffer with internal Crystal Oscillator. The XTAL range is from 10MHz to 50MHz. The device has a wide range of operating voltages of 2.5V and 3.3V. The device also provides user selectable output VDD option, which provides excellent flexibilities to users. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

Pin Configuration



Block Diagram



Pin Description

Pin#	Pin Name	Type		Description
1, 3, 5, 7, 18, 20, 22, 24	CLK0~7	Output		Clock Outputs
2, 6, 19, 23	V _{DDO}	Power		Output Power Supplier
4, 9, 16, 21, 25, 32	GNDO	Power		Core Ground
8, 17	NC	-		No Connect
15, 26	GND	Power		Output Ground
10	V _{DD}	Power		Core Power Supplier
11	XIN	Input		Crystal interface
12	XOUT	Output		Crystal interface
13	IN0	Input	Pull-down	Diff or Single End
14	IN0#	Input	Pull-up/ Pull-down	When IN0 is single end IN0# internal bias as V _{dd} /2
27	IN1#	Input	Pull-up/ Pull-down	When IN1 is single end IN1# internal bias as V _{dd} /2
28	IN1	Input	Pull-down	REF1 Diff or Single End
30, 29	IN_SEL[0:1]	Input	Pull-down	IN-SEL[0:1] select XTAL, IN1/1# and IN0/IN0# input
31	ENABLE	Input		Synchronous active high Output Enable, LVCMOS/TTL

Input Mode Selection Logic

IN_SEL0	IN_SEL1	Selected Input
1	1	XTAL
0	1	XTAL
1	0	IN1/1# Diff or Single End
0	0	IN0/0# Diff or Single End

Input/Output Operation State

Input State	Output State
IN[0:1], IN[0:1]# open	Logic Low
IN[0:1], IN[0:1]# both to ground	Logic Low
IN[0:1]=High, IN[0:1]# =Low	Logic High
IN[0:1]=Low, IN[0:1]# =High	Logic Low

Output Mode Selection

ENABLE	Output CLK0~7
GND	High-impedance
V _{DD}	Enabled

Power Supply DC Characteristics ($V_{DD}/V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	ENABLE = '0'			32	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			1	mA

Power Supply DC Characteristics ($V_{DD}/V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	ENABLE = '0'			15	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			0.7	mA

Power Supply DC Characteristics ($V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	ENABLE = '0'			29	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			0.6	mA

Power Supply DC Characteristics ($V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ C$ to $85^\circ C$)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current	ENABLE = '0'			29	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			0.4	mA

Power Supply DC Characteristics ($V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.5V \pm 0.15V$, $T_A = -40^\circ C$ to $85^\circ C$)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.35	1.5	1.65	V
I_{DD}	Power Supply Current	ENABLE = '0'			29	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			0.3	mA

Power Supply DC Characteristics ($V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ C$ to $85^\circ C$)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current	ENABLE = '0'			13	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			0.4	mA

Power Supply DC Characteristics ($V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.5V \pm 0.15V$, $T_A = -40^\circ C$ to $85^\circ C$)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.35	1.5	1.65	V
I_{DD}	Power Supply Current	ENABLE = '0'			13	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			0.3	mA

Power Supply DC Characteristics ($V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.2V \pm 0.06V$, $T_A = -40^\circ C$ to $85^\circ C$)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.14	1.2	1.26	V
I_{DD}	Power Supply Current	ENABLE = '0'			13	mA
I_{DDO}	Output Supply Current	ENABLE = '0'			0.3	mA

Single-Ended input DC Characteristics ($T_A = -40^\circ C$ to $85^\circ C$)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
V_{IH}	Input High Voltage	$V_{DD} = 3.3V \pm 5\%$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V \pm 5\%$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	$V_{DD} = 3.3V \pm 5\%$	-0.3		0.8	V
		$V_{DD} = 2.5V \pm 5\%$	-0.3		0.7	V
V_{OH}	Output High Voltage ($I_{OH} = -8mA$)	$V_{DDO} = 3.3V \pm 5\%$ ⁽¹⁾	2.6			V
		$V_{DDO} = 2.5V \pm 5\%$	2			V
		$V_{DDO} = 2.5V \pm 5\%$ ⁽¹⁾	1.8			V
		$V_{DDO} = 1.8V \pm 0.2V$ ⁽¹⁾	1.5			V
	$V_{DDO} = 1.5V \pm 0.15V$ ⁽¹⁾	1.0			V	
	Output High Voltage ($I_{OH} = -1mA$)	$V_{DDO} = 1.2V \pm 0.06V$	0.7			V
V_{OL}	Output Low Voltage ($I_{OL} = 8mA$)	$V_{DDO} = 3.3V \pm 5\%$ ⁽¹⁾	2.6			V
		$V_{DDO} = 2.5V \pm 5\%$			0.5	V
		$V_{DDO} = 1.8V \pm 0.2V$ ⁽¹⁾			0.4	V
	$V_{DDO} = 1.5V \pm 0.15V$ ⁽¹⁾			0.35	V	
	Output Low Voltage ($I_{OH} = 1mA$)	$V_{DDO} = 1.2V \pm 0.06V$			0.2	V

Notes:

1. Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement section, "Load Test Circuit" diagrams.

Differential input DC Characteristics ($T_A = -40^{\circ}\text{C}$ to 85°C)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
I_{IH}	Input High Current	IN[0:1], IN[0:1]#	$V_{DD} = V_{IN} = 3.465\text{V}$ or 2.625V		100	μA
I_{IL}	Input Low Current	IN[0:1]	$V_{DD} = 3.465\text{V}$ or 2.625V $V_{IN} = 0\text{V}$	-1		μA
		IN[0:1]#	$V_{DD} = 3.465\text{V}$ or 2.625V $V_{IN} = 0\text{V}$	-50		μA
V_{PP}	Peak-to-Peak Input Voltage ⁽¹⁾	$V_{DD} = 3.3\text{V}$	0.25		1.3	V
		$V_{DD} = 2.5\text{V}$	0.25		1.3	
V_{CMR}	Common Mode Input Voltage (1,2)	$V_{DD} = 3.3\text{V}$	0.5		$V_{DD} - 1.35\text{V}$	V
		$V_{DD} = 2.5\text{V}$	0.5		$V_{DD} - 0.85\text{V}$	

Notes:

- V_{IL} should not be less than -0.3V .
- Common mode voltage is defined as $1/2(V_{IH} - V_{IL})$.

3.3V Absolute Maximum Ratings (Above which the useful life may be impaired. For user guidelines only, not tested.)

Storage Temperature.....	-65°C to +150°C
V _{DD} , V _{DDO} Voltage.....	-0.5V to +3.6V
Output Voltage	-0.5V to V _{DD} +0.5V
Input Voltage	-0.5V to V _{DD} +0.5V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC Characteristics (Over Operating Range: V_{DD}/V_{DDO} = 3.3V ± 5%, T_A = -40° to 85°C)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ	Max.	Units
f _{MAX}	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source ⁽²⁾	DC		200	
odc	Output Duty Cycle	125MHz	45		55	%
t _{sk(o)}	Output Skew ⁽³⁾				80	ps
t _{jit(Ø)}	RMS Phase Jitter (Random)	25MHz crystal @ (Integration Range: 100Hz-1MHz)		0.05		ps
t _{jit(additive)}	Additive RMS Phase Jitter (Random)	125MHz reference input @ (Integration Range: 12kHz-20MHz)		0.01		ps
t _R /t _F	Output Rise/Fall Time	20% to 80%	200		800	ps
t _{EN}	Output Enable Time ⁽⁴⁾				5	cycles
t _{DIS}	Output Disable Time ⁽⁴⁾				5	cycles
MUX _{isolation}	MUX Isolation	155.52MHz		64		dB

Notes:

1. Unless noted otherwise, all parameters are tested with xtal @ f ≤ F_{xtal_max}; outputs are terminated @ 50Ω to V_{DDO}/2, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0#/IN1# set as V_{DD}/2
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 5 cycles. Min. setup time = 3ns.

2.5V Absolute Maximum Ratings (Above which the useful life may be impaired. For user guidelines only, not tested.)

Storage Temperature.....	-65°C to +150°C
V _{DD} , V _{DDO} Voltage.....	-0.5V to +3.6V
Output Voltage	-0.5V to V _{DD} +0.5V
Input Voltage	-0.5V to V _{DD} +0.5V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC Characteristics (Over Operating Range: V_{DD}/V_{DDO} = 2.5V ± 5%, T_A = -40° to 85°C)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ	Max.	Units
f _{MAX}	Output Frequency	Using External Crystal		10	50	MHz
		Using External Clock Source ⁽²⁾		DC	200	
odc	Output Duty Cycle	125MHz	45		55	%
t _{sk(o)}	Output Skew ⁽³⁾				80	ps
t _{jit(Ø)}	RMS Phase Jitter (Random)	25MHz @ (Integration Range: 100Hz-1MHz)		0.06		ps
t _{jit(additive)}	Additive RMS Phase Jitter (Random)	125MHz @ (Integration Range: 12kHz-20MHz)		0.01		ps
t _R /t _F	Output Rise/Fall Time	20% to 80%	200		800	ps
t _{EN}	Output Enable Time ⁽⁴⁾				5	cycles
t _{DIS}	Output Disable Time ⁽⁴⁾				5	cycles
MUX _{isolation}	MUX Isolation	155.52MHz		63		dB

Notes:

1. Unless noted otherwise, all parameters are tested with xtal @ f ≤ F_{xtal_max}; outputs are terminated @ 50Ω to V_{DDO}/2, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0#/IN1# set as V_{DD}/2
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 5 cycles. Min. setup time = 3ns.

AC Characteristics (Over Operating Range: $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ$ to $85^\circ C$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ	Max.	Units
f _{MAX}	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source ⁽²⁾	DC		200	
odc	Output Duty Cycle	125MHz	45		55	%
t _{sk(o)}	Output Skew ⁽³⁾				80	ps
t _{jit(Ø)}	RMS Phase Jitter (Random)	25MHz @ (Integration Range: 100Hz-1MHz)		0.05		ps
t _{jit(additive)}	Additive RMS Phase Jitter (Random)	125MHz @ (Integration Range: 12kHz-20MHz)		0.01		ps
t _R /t _F	Output Rise/Fall Time	20% to 80%	200		800	ps
t _{EN}	Output Enable Time ⁽⁴⁾				5	cycles
t _{DIS}	Output Disable Time ⁽⁴⁾				5	cycles
MUX _{isolation}	MUX Isolation	155.52MHz		62		dB

Notes:

1. Unless noted otherwise, all parameters are tested with xtal @ $f \leq F_{xtal_max}$; outputs are terminated @ 50Ω to $V_{DDO}/2$, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 5 cycles. Min. setup time = 3ns.

AC Characteristics (Over Operating Range: $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ$ to $85^\circ C$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ	Max.	Units
f _{MAX}	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source ⁽²⁾	DC		200	
odc	Output Duty Cycle	125MHz	45		55	%
t _{sk(o)}	Output Skew ⁽³⁾				80	ps
t _{jit(Ø)}	RMS Phase Jitter (Random)	25MHz @ (Integration Range: 100Hz-1MHz)		0.06		ps
t _{jit(additive)}	Additive RMS Phase Jitter (Random)	125MHz @ (Integration Range: 12kHz-20MHz)		0.01		ps
t _R /t _F	Output Rise/Fall Time	20% to 80%	200		900	ps
t _{EN}	Output Enable Time ⁽⁴⁾				5	cycles
t _{DIS}	Output Disable Time ⁽⁴⁾				5	cycles
MUX _{isolation}	MUX Isolation	155.52MHz		58		dB

Notes:

1. Unless noted otherwise, all parameters are tested with xtal @ $f \leq F_{xtal_max}$; outputs are terminated @ 50Ω to $V_{DDO}/2$, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 5 cycles. Min. setup time = 3ns.

AC Characteristics (Over Operating Range: $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.5V \pm 0.15V$, $T_A = -40^\circ$ to $85^\circ C$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ	Max.	Units
f _{MAX}	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source ⁽²⁾	DC		200	
odc	Output Duty Cycle	125MHz	45		55	%
t _{sk(o)}	Output Skew ⁽³⁾				80	ps
t _{jit(Ø)}	RMS Phase Jitter (Random)	25MHz @ (Integration Range: 100Hz-1MHz)		0.07		ps
t _{jit(additive)}	Additive RMS Phase Jitter (Random)	125MHz @ (Integration Range: 12kHz-20MHz)		0.01		ps
t _{R/tF}	Output Rise/Fall Time	20% to 80%	200		900	ps
t _{EN}	Output Enable Time ⁽⁴⁾				5	cycles
t _{DIS}	Output Disable Time ⁽⁴⁾				5	cycles
MUX _{isolation}	MUX Isolation	155.52MHz		53		dB

Notes:

1. Unless noted otherwise, all parameters are tested with xtal @ $f \leq F_{xtal_max}$; outputs are terminated @ 50Ω to $V_{DDO}/2$, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 5 cycles. Min. setup time = 3ns.

AC Characteristics (Over Operating Range: $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ$ to $85^\circ C$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ	Max.	Units
f _{MAX}	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source ⁽²⁾	DC		200	
odc	Output Duty Cycle	125MHz	45		55	%
t _{sk(o)}	Output Skew ⁽³⁾				80	ps
t _{jit(Ø)}	RMS Phase Jitter (Random)	25MHz @ (Integration Range: 100Hz-1MHz)		0.06		ps
t _{jit(additive)}	Additive RMS Phase Jitter (Random)	125MHz @ (Integration Range: 12kHz-20MHz)		0.01		ps
t _R /t _F	Output Rise/Fall Time	20% to 80%	200		900	ps
t _{EN}	Output Enable Time ⁽⁴⁾				5	cycles
t _{DIS}	Output Disable Time ⁽⁴⁾				5	cycles
MUX _{isolation}	MUX Isolation	155.52MHz		59		dB

Notes:

1. Unless noted otherwise, all parameters are tested with xtal @ $f \leq F_{xtal_max}$; outputs are terminated @ 50Ω to $V_{DDO}/2$, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 5 cycles. Min. setup time = 3ns.

AC Characteristics (Over Operating Range: $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.5V \pm 0.15V$, $T_A = -40^\circ$ to $85^\circ C$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ	Max.	Units
f _{MAX}	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source ⁽²⁾	DC		200	
odc	Output Duty Cycle	125MHz	45		55	%
t _{sk(o)}	Output Skew ⁽³⁾				80	ps
t _{jit(Ø)}	RMS Phase Jitter (Random)	25MHz @ (Integration Range: 100Hz-1MHz)		0.08		ps
t _{jit(additive)}	Additive RMS Phase Jitter (Random)	125MHz @ (Integration Range: 12kHz-20MHz)		0.01		ps
t _R /t _F	Output Rise/Fall Time	20% to 80%	200		900	ps
t _{EN}	Output Enable Time ⁽⁴⁾				5	cycles
t _{DIS}	Output Disable Time ⁽⁴⁾				5	cycles
MUX _{isolation}	MUX Isolation	155.52MHz		55		dB

Notes:

1. Unless noted otherwise, all parameters are tested with xtal @ $f \leq F_{xtal_max}$; outputs are terminated @ 50Ω to $V_{DDO}/2$, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 5 cycles. Min. setup time = 3ns.

AC Characteristics (Over Operating Range: $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.2V \pm 0.06V$, $T_A = -40^\circ$ to $85^\circ C$)

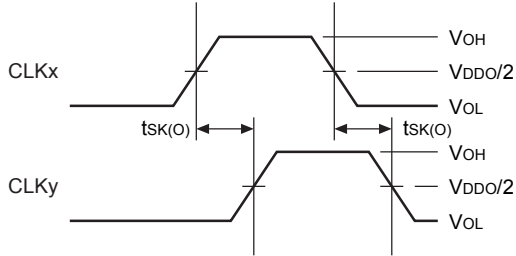
Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ	Max.	Units
f _{MAX}	Output Frequency	Using External Crystal	10		50	MHz
		Using External Clock Source ⁽²⁾	DC		125	
odc	Output Duty Cycle	125MHz, 5pF load	40		60	%
t _{sk(o)}	Output Skew ⁽³⁾				60	ps
t _{jit(Ø)}	RMS Phase Jitter (Random)	25MHz @ (Integration Range: 100Hz-1MHz)		0.13		ps
t _{jit(additive)}	Additive RMS Phase Jitter (Random)	125MHz @ (Integration Range: 12kHz-20MHz)		0.01		ps
t _R /t _F	Output Rise/Fall Time	20% to 80%		1000	1900	ps
t _{EN}	Output Enable Time ⁽⁴⁾				6	cycles
t _{DIS}	Output Disable Time ⁽⁴⁾				6	cycles
MUX _{isolation}	MUX Isolation	150MHz		72		dB

Notes:

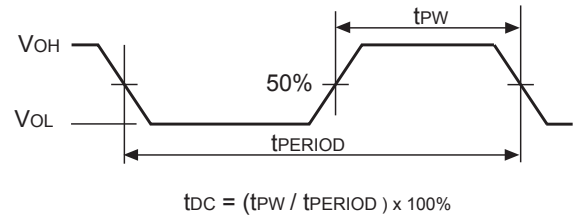
1. Unless noted otherwise, all parameters are tested with xtal @ $f \leq F_{xtal_max}$; outputs are terminated @ 50Ω to $V_{DDO}/2$, see waveforms.
2. Diff external clock source is driving IN0/IN0# and IN1/IN1# input. IN0/IN1 can be single end ref clock when IN0# /IN1# set as $V_{DD}/2$
3. Identical conditions: loading, transitions, supply voltage, temperature, package type and speed grade.
4. These parameters are guaranteed, but not tested. Max delay is 6 cycles. Min. setup time = 3ns.

Waveforms

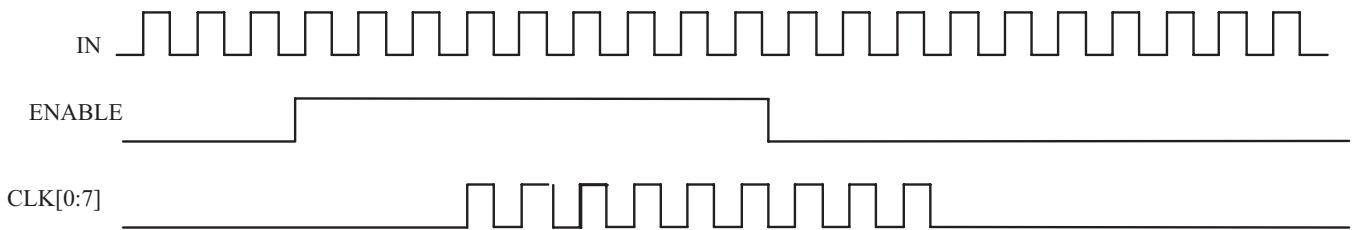
Output to Output Skew – tsk(O)



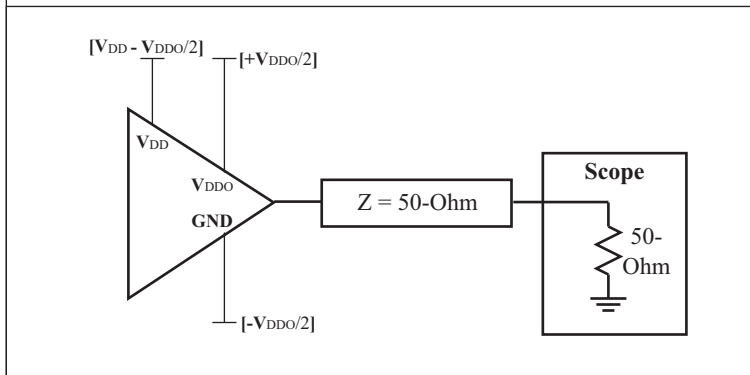
Duty Cycle – tDC



ENABLE Timing Diagram



AC Test Circuit Load



Crystal Characteristic (link to "<http://www.pericom.com/products/timing/crystals/index.php>" for more detailed and different size crystal specifications)

Parameters	Description	Min	Typ	Max.	Units
OSCMODE	Mode of Oscillation	Fundamental			
FREQ	Frequency	10	25	50	MHz
ESR ⁽¹⁾	Equivalent Series Resistance	30		50	Ohm
CLOAD	Load Capacitance		18		pF
CSHUNT	Shunt Capacitance			7	pF
DRIVE level				1	mW

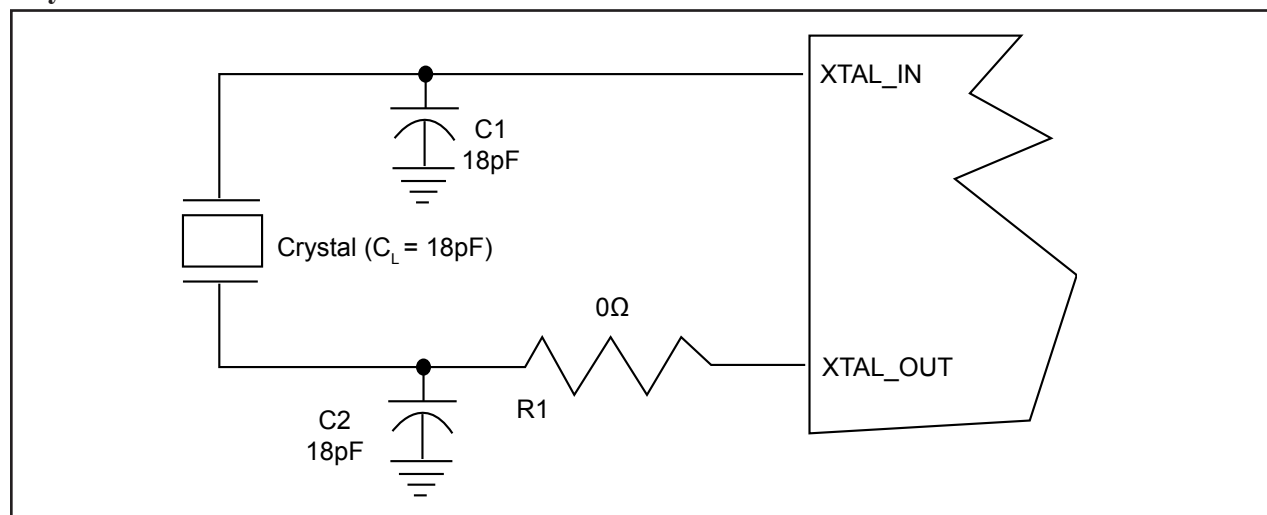
Note: 1. ESR value is dependent upon frequency of oscillation

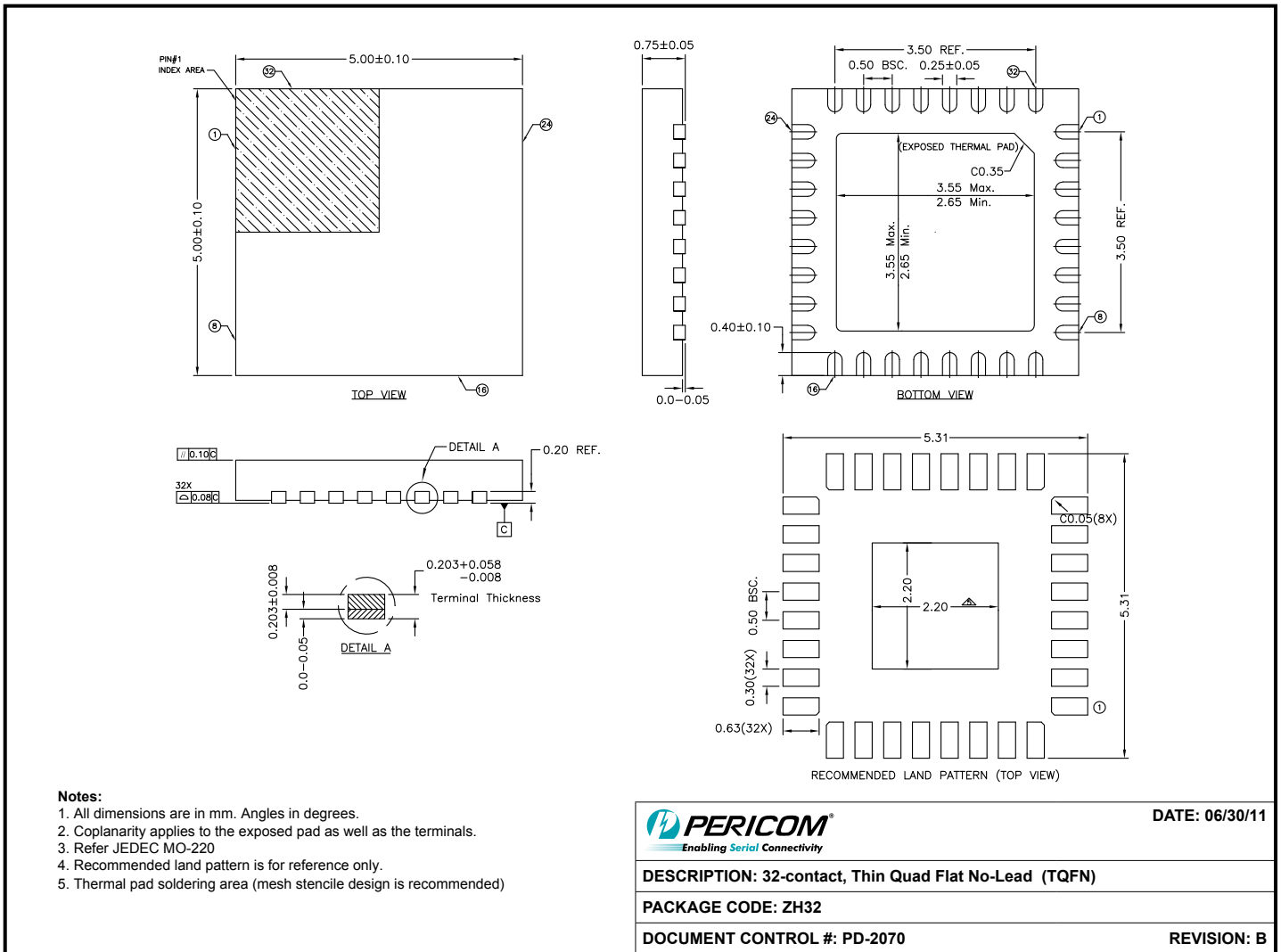
Application Notes

Crystal circuit connection

The following diagram shows PI6C49X0208 crystal circuit connection with a parallel crystal. For the $C_L=18\text{pF}$ crystal, it is suggested to use $C1=18\text{pF}$, $C2=18\text{pF}$. $C1$ and $C2$ can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts. $R1$ is not recommended.

Crystal Oscillator Circuit





Note: 11-0147

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Ordering Information(1,2,3)

Ordering Code	Package Code	Package Description
PI6C49X0208ZHIE	ZH	Pb-Free and Green 32-pin TQFN

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. X suffix = Tape/Reel

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[ADCLK905BCPZ-R7](#) [ADCLK907BCPZ-R2](#) [ADCLK907BCPZ-WP](#) [ADCLK914BCPZ-R2](#) [ADCLK914BCPZ-R7](#) [ADCLK925BCPZ-R2](#)
[ADCLK925BCPZ-R7](#)