2-Output PCIe Gen 4 Clock Generator for Automotive Applications

Features

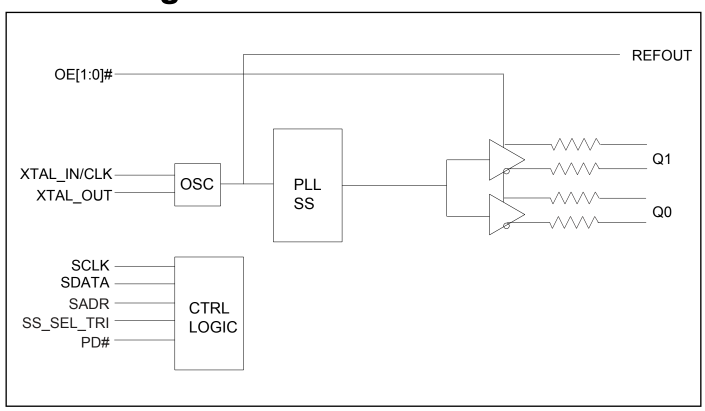
- 1.8V supply voltage
- Crystal/CMOS input: 25 MHz
- 2 differential low power HCSL outputs with on-chip termination
- Individual output enable
- Reference CMOS output
- Programmable Slew rate and output amplitude for each output
- Differential outputs blocked until PLL is locked
- Selectable 0%, -0.25% or -0.5% spread on differential outputs
- Strapping pins or SMBus for configuration;
- 3.3V tolerant SMBus interface support
- Very low jitter outputs
  - Differential cycle-to-cycle jitter <50ps
  - Differential output-to-output skew <50ps
  - PCIe Gen1/Gen2/Gen3/Gen4 compliant
  - CMOS REFOUT phase jitter is < 1.5ps RMS
- AEC-Q 100 qualified, Automotive Grade 2 support
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green): 24-lead 4×4mm TQFN

Description

The PI6CG182Q is an 2-output very low power PCIe Gen1/Gen2/Gen3/ Gen4 clock generator. It uses 25MHz crystal or CMOS reference as an input to generate the 100MHz low power differential HCSL outputs with on-chip terminations. The on-chip termination can save 8 external resistors and make layout easier. An additional buffered reference output is provided to serve as a low noise reference for other circuitry.

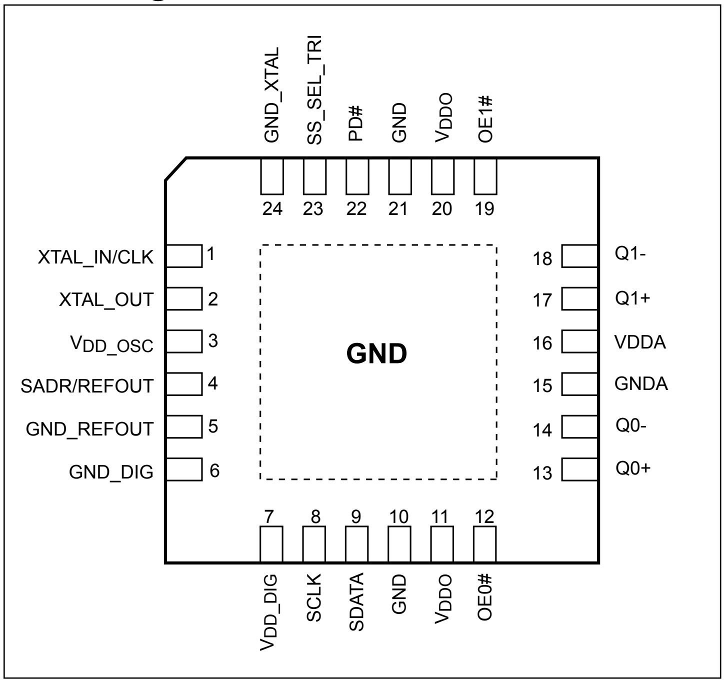
It uses Diodes' proprietary PLL design to achieve very low jitter that meets PCIe Gen1/Gen2/Gen3/Gen4 requirements. It also provides various options such as different slew rate and amplitude through strapping pins or SMBUS so that users can configure the device easily to get the optimized performance for their individual boards. The device also supports selectable spread-spectrum options to reduce EMI for Automotive applications.

Block Diagram



Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin #	Pin Name	Type		Description
1	XTAL_IN/CLK	Input		Crystal input or CMOS reference input
2	XTAL_OUT	Output		Crystal output
3	V_{DD}_OSC	Power		Power supply for oscillator circuitry, nominal 1.8V
4	SADR/REFOUT	Input/ Output	CMOS	Latch to select SMBus Address or 1.8V LVCMOS REFOUT. This pin has an internal pull-down.
5	GND_REFOUT	Power		Ground for REFOUT
6	GND_DIG	Power		Ground for digital circuitry
7	V_{DD}_DIG	Power		Power supply for digital circuitry, nominal 1.8V
8	SCLK	Input	CMOS	SMBUS clock input, 3.3V tolerant
9	SDATA	Input/ Output	CMOS	SMBUS Data line, 3.3V tolerant
10, 21	GND	Power		Ground
11, 20	V_{DDO}	Power		Power supply for differential outputs
12	OE0#	Input	CMOS	Active low input for enabling Q0 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
13	Q0+	Output	HCSL	Differential true clock output
14	Q0-	Output	HCSL	Differential complementary clock output
15	GNDA	Power		Ground for analog circuitry
16	V_{DDA}	Power		Power supply for analog circuitry
17	Q1+	Output	HCSL	Differential true clock output

Pin Description Cont.

Pin #	Pin Name	Type		Description
18	Q1-	Output	HCSL	Differential complementary clock output
19	OE1#	Input	CMOS	Active low input for enabling Q1 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
22	PD#	Input	CMOS	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
23	SS_SEL_TRI	Input	Tri-level	Latched select input to select spread spectrum amount at initial power up 1 = -0.5% spread, M = -0.25%, 0 = Spread Off
24	GND_XTAL	Power		Ground for oscillator circuit

SMBus Address Selection Table

	SADR	Address	+Read/Write Bit
State of SADR on first application of PD#	0	1101000	X
	1	1101010	X

Power Management Table

PD#	SMBus OE bit	OEn#	Qn+	Qn-	REFOUT
0	X	X	Low	Low	HiZ
1	1	0	Running	Running	Running
1	1	1	Low	Low	Low
1	0	X	Low	Low	Low

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential, V_{DDxx}	−0.5V to +2.5V
Input Voltage	−0.5V to V_{DD}+0.5V, not exceed 2.5V
SMBus, Input High Voltage	3.6V
ESD Protection (HBM)	2000 V
ESD Protection (CDM) PD# pin #22 only	250 V
ESD Protection (CDM) all other pins	500 V
Max Junction Temperature	+125°C

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DDO}, V_{DDA}, V_{DD}_OSC, V_{DD}_DIG	Power Supply Voltage		1.7	1.8	1.9	V
I_{DDA}	Analog Power Supply Current	All outputs active @100MHz		7	8	mA
I_{DD}	Power Supply Current	All V_{DD}, except V_{DDA} All outputs active @100MHz		15	18	mA
I_{DD_WL}	Power Supply Wake-on-LAN(1) Current	All V_{DD}, Q outputs off, REF output running		1.5	2	mA
I_{DD_PD}	Power Supply Power Down(2) Current	All outputs off		0.6	1	mA
T_A	Ambient Temperature	Automotive Grade 2	−40		105	°C

Note:

1. Wake-on-LAN mode: PD# = '0' Byte 3, bit 5 = '1'
2. Power down mode: PD# = '0' Byte 3, bit 5 = '0'

Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
R_{pu}	Internal pull up resistance			120		KΩ
R_{dn}	Internal pull down resistance			120		KΩ
C_{XTAL}	Internal capacitance on X_IN and X_OUT pins			5		pF
L_{PIN}	Pin inductance				7	nH

Crystal Characteristic

Parameters	Description	Min.	Typ	Max.	Units
OSCmode	Mode of Oscillation		Fundamental		
FREQ	Frequency		25		MHz
ESR[1]	Equivalent Series Resistance			50	Ω
Cload	Load Capacitance		8		pF
Cshunt	Shunt Capacitance			7	pF
	Drive Level			300	uW

Note:

1. ESR value is dependent upon frequency of oscillation

SMBus Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DDSMB}	Nominal bus voltage		1.7		3.6	V
V_{IHSMB}	SMBus Input High Voltage	SMBus, V_{DDSMB} = 3.3V	2.1		3.6	V
		SMBus, V_{DDSMB} < 3.3V	0.65 V_{DDSMB}			
V_{ILSMB}	SMBus Input Low Voltage	SMBus, V_{DDSMB} = 3.3V			0.6	V
		SMBus, V_{DDSMB} < 3.3V			0.6	
$I_{SMBSINK}$	SMBus sink current	SMBus, at V_{OLSMB}	4			mA
V_{OLSMB}	SMBus Output Low Voltage	SMBus, at $I_{SMBSINK}$			0.4	V
f_{MAXSMB}	SMBus operating frequency	Maximum frequency			400	kHz
t_{RMSB}	SMBus rise time	(Max V_{IL} - 0.15) to (Min V_{IH} + 0.15)			1000	ns
t_{FMSB}	SMBus fall time	(Min V_{IH} + 0.15) to (Max V_{IL} - 0.15)			300	ns

Spread Spectrum Characteristic

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
f_{MOD}	SS Modulation Frequency	Triangular modulation	30	31.6	33	kHz

LVCMOS DC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Single-ended inputs, except SMBus	0.75 V_{DD}		V_{DD} +0.3	V
V_{IM}	Input Mid Voltage	SS_SEL_TRI	$0.4V_{DD}$	$0.5V_{DD}$	$0.6V_{DD}$	V
V_{IL}	Input Low Voltage	Single-ended inputs, except SMBus	-0.3		0.25 V_{DD}	V
I_{IH}	Input High Current	Single-ended inputs, $V_{IN} = V_{DD}$			20	µA
I_{IL}	Input Low Current	Single-ended inputs, $V_{IN} = 0V$	-20			µA
I_{IH}	Input High Current	Single-ended inputs with pull up / pull down resistor, $V_{IN} = V_{DD}$			220	µA
I_{IL}	Input Low Current	Single-ended inputs with pull up / pull down resistor, $V_{IN} = 0V$	-220			µA
V_{OH}	Output High Voltage	REFOUT, except SMBus; I_{OH} = -2mA	V_{DD} -0.45			V
V_{OL}	Output Low Voltage	REFOUT, except SMBus; I_{OH} = 2mA			0.45	V
R_{OUT}	CMOS Output impedance			20		Ω
C_{IN}	Input Capacitance		1.5		5	pF

LVCMOS AC Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
f_{INPUT}	Input Frequency	XTAL_IN/CLK	23	25	27	MHz
t_{RIN}	Input rise time	Single-ended inputs			5	ns
t_{FIN}	Input fall time	Single-ended inputs			5	ns
t_{STAB}	Clock stabilization	From Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.6	1.8	ms
t_{OELAT}	Output enable latency	Q start after OE# assertion Q stop after OE# deassertion	1		3	clocks
t_{PDLAT}	PD# de-assertion	Differential outputs enable after PD# de-assertion			300	us
t_{PERIOD}	REFOUT clock period	REFOUT, assume input is at 25MHz		40		ns
f_{ACC}	REFOUT frequency accuracy(1)	REFOUT, long term accuracy to input		0		ppm
t_{SLEW}	REFOUT slew rate(1)	Byte 3 = 1F, 20% to 80% of V_{DDREF}		1	2.5	V/ns
		Byte 3 = 5F, 20% to 80% of V_{DDREF}		1.6	2.5	V/ns
		Byte 3 = 9F, 20% to 80% of V_{DDREF}		2.0	2.5	V/ns
		Byte 3 = DF, 20% to 80% of V_{DDREF}		2.1	2.5	V/ns
t_{DC}	REFOUT Duty Cycle(1)	$V_T = V_{DD}$ /2 V, driven by a Xtal	45	50	55	%

LVCMOS AC Characteristics Cont.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
t_{DCDIS}	REFOUT Duty Cycle Distortion	$V_T = V_{DD}$ /2 V, driven by an external source	0	2	4	%
t_{JITCC}	REFOUT cycle-cycle jitter	$V_T = V_{DD}$ /2 V, driven by a Xtal		20	250	ps
t_{JITPH}	REFOUT phase jitter	12kHz to 5MHz, RMS, driven by a Xtal		0.68	1.5	ps
t_{JITN}	Noise floor	1kHz offset, driven by a Xtal		-130	-105	dBc
		10kHz offset to Nyquist, driven by a Xtal		-140	-120	dBc

Note:

1. Guaranteed by design and characterization, not 100% tested in production

HCSL Output Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output Voltage High(1)	Statistical measurement on single-ended signal using oscilloscope math function	660	784		mV
V_{OL}	Output Voltage Low(1)		-150		150	mV
V_{OMAX}	Output Voltage Maximum(1)	Measurement on single ended signal using absolute value		816	1150	mV
V_{OMIN}	Output Voltage Minimum(1)		-300	-15		mV
V_{OSWING}	Output Swing Voltage(1,2,3)	Scope averaging off	300	1551		mV
V_{OC}	Output Cross Voltage(1,2,4)		250	400	550	mV
DV_{OC}	V_{OC} Magnitude Change(1,2,5)			14	140	mV

Note:

1. At default SMBUS amplitude settings
2. Guaranteed by design and characterization, not 100% tested in production
3. Measured from differential waveform
4. This one is defined as voltage where Q+ = Q- measured on a component test board and only applied to the differential rising edge
5. The total variation of all Vcross measurements in any particular system. This is a subset of Vcross_min/max allowed.

HCSL Output AC Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
f_{OUT}	Output Frequency			100		MHz
t_{RF}	Slew rate(1,2,3)	Scope averaging on fast setting	2.9	3.1	5.7	V/ns
		Scope averaging on slow setting	1.1	2.0	3.0	V/ns
Dt_{RF}	Slew rate matching(1,2,4)	Scope averaging on		3		%
t_{DC}	Duty Cycle(1,2)	Measured differentially, PLL Mode	45	50	55	%
t_{SKEW}	Output Skew(1,2)	Averaging on, V_T = 50%		34	50	ps
tj_{c-c}	Cycle to cycle jitter(1,2)			14	55	ps
$t_{STARTUP}$	Start up time				10	ms
t_{LOCK}	PLL lock time				20	ms

HCSL Output AC Characteristics Cont.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
tj_{PHASE}	Integrated phase jitter (RMS) (1,5,6)	PCIe Gen 1	20	25	86	ps
		PCIe Gen 2 Low Band, 10kHz < f < 1.5MHz	0.8	0.9	3.0	ps
		PCIe Gen 2 High Band, 1.5MHz < f < Nyquist (50MHz)	1.5	1.6	3.1	ps
		PCIe Gen 3 Common Clock Architecture (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	0.4	0.5	1.0	ps
		PCIe Gen 4 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	0.25	0.3	0.5	ps

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. Measured from differential waveform
3. Slew rate is measured through the Vswing voltage range centered around differential 0V, within +/-150mV window
4. It is measured using a +/-75mV window centered on the average cross point
5. See http://www.pcisig.com for complete specs
6. Sample size of at least 100k cycles. This can be extrapolated to 108ps pk-pk @ 1M cycles for a BER of 10^{-12}

Differential Output Clock Periods - Spread Spectrum Disabled [1, 2]

Center Freq. MHz	Measurement Window							Units
	1 clock	1 us	0.1 s	0.1 s	0.1 s	1 us	1 clock	
	-c2c jitter AbsPer Min	- SSC Short-term Avg. Min	-ppm Long-term Avg. min	0 ppm Period Nominal	+ppm Long-term Avg. max	+ SSC Short-term Avg. Max	-c2c jitter AbsPer Max	
100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns

Differential Output Clock Periods - Spread Spectrum Enabled [1, 2]

Center Freq. MHz	Measurement Window							Units
	1 clock	1 us	0.1 s	0.1 s	0.1 s	1 us	1 clock	
	-c2c jitter AbsPer Min	- SSC Short-term Avg. Min	-ppm Long-term Avg. min	0 ppm Period Nominal	+ppm Long-term Avg. max	+ SSC Short-term Avg. Max	-c2c jitter AbsPer Max	
99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. All long term accuracy and clock period specifications are guaranteed assuming REF is trimmed to 25.00MHz

SMBus Serial Data Interface

PI6CG182Q is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	SADR	0	1/0

Note: SMBus address is latched on SADR pin

How to Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit		8 bits	1 bit	1 bit
Start bit	Add.	W(0)	Ack	Beginning Byte location = N	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack	....	Data Byte (N+X-1)	Ack	Stop bit

How to Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte location = N	Ack	Repeat Start bit	Address	R(1)	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack

	8 bits	1 bit	1 bit
....	Data Byte (N+X-1)	NAck	Stop bit

Byte 0: Output Enable Register[1]

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			1		
6	Reserved			1		
5	Reserved			1		
4	Reserved			1		
3	Reserved			1		
2	Q1_OE	Q1 output enable	RW	1	Low/Low	Enabled
1	Q0_OE	Q0 output enable	RW	1	Low/Low	Enabled
0	Reserved			1		

Note:

1. A low on these bits will override the OE# pins and force the differential outputs to Low/Low states

Byte 1: SS Readback and Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	SSENRB1	SS Enable Readback Bit1	R	Latch	'00' for SS_SEL_TRI = '0', '01' for SS_SEL_TRI = 'M', '11' for SS_SEL_TRI = '1'	
6	SSENRB0	SS Enable Readback Bit0	R	Latch		
5	SSEN_SWCTR	Enable SW control of SS	RW	0	Values in B1[7:6] control SS amount	Values in B1[4:3] control SS amount
4	SSENSW1	SS enable SW control Bit1	RW[1]	0	'00' = SS off, '01' = -0.25% SS, '10' = Reserved, '11' = -0.5% SS	
3	SSENSW0	SS enable SW control Bit0	RW[1]	0		
2	Reserved			1		
1	Amplitude1	Control output amplitude	RW	1	'00' = 0.6V, '01' = 0.7V, '10' = 0.8V, '11' = 0.9V	
0	Amplitude0		RW	0		

Note:

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

Byte 2: Differential Output Slew Rate Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			1		
6	Reserved			1		
5	Reserved			1		
4	Reserved			1		
3	Reserved			1		
2	SLEWRATECTR_Q1	Control slew rate of Q1	RW	1	Slow setting	Fast setting
1	SLEWRATECTR_Q0	Control slew rate of Q0	RW	1	Slow setting	Fast setting
0	Reserved			1		

Byte 3: REF Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	REFSLEWRATE	Slew rate control for REF	RW	0	'00' = 0.9V/ns '01' = 1.3V/ns,	
6			RW	1	'10' = 1.6V/ns, '11' = 1.8V/ns	
5	REF_PDSTATE	Wake-on-Lan enable for REF	RW	0	REF = 'Low'	REF = running
4	REF_OE	Output enable for REF	RW	1	REF = "Low'	REF = running
3	Reserved			1		
2	Reserved			1		
1	Reserved			1		
0	Reserved			1		

Byte 4: Reserved

Bit	Control Function	Description	Type	Power Up Condition	0	1
7:0	Reserved			1		

Byte 5: Revision and Vendor ID Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	RID3	Revision ID	R	0	rev = 0000	
6	RID2		R	0		
5	RID1		R	0		
4	RID0		R	0		
3	PVID3	Vendor ID	R	0	Diodes = 0011	
2	PVID3		R	0		
1	PVID3		R	1		
0	PVID3		R	1		

Byte 6: Device Type/Device ID Register

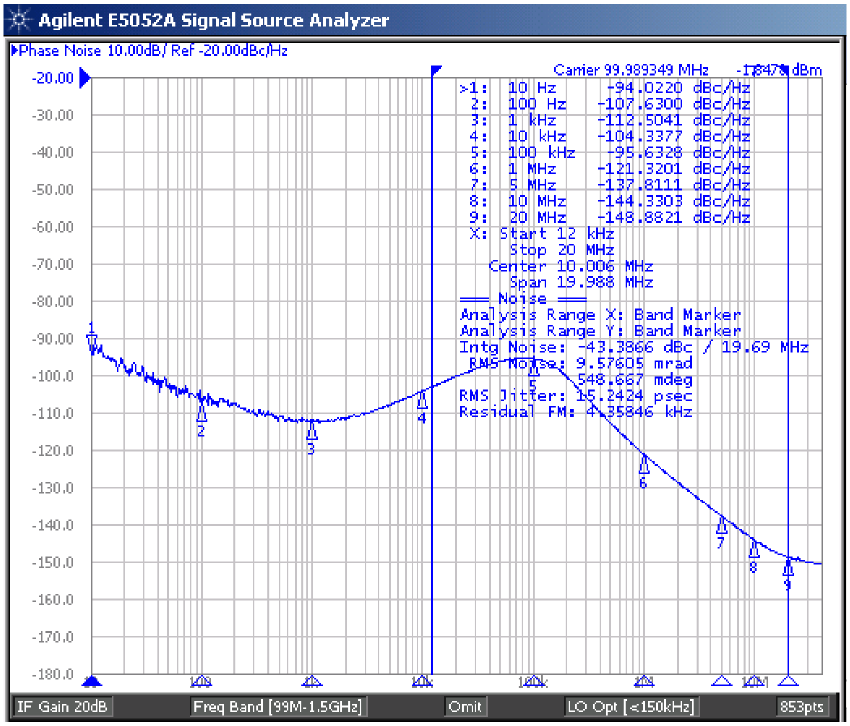
Bit	Control Function	Description	Type	Power Up Condition	0	1
7	DTYPE1	Device type	R	0	'00' = CG, '01' = ZDB,	
6	DTYPE0		R	0	'10' = Reserve, '11' = ZDB	
5	DID5	Device ID	R	0	000010 binary, 02Hex	
4	DID4		R	0		
3	DID3		R	0		
2	DID2		R	0		
1	DID1		R	1		
0	DID0		R	0		

Byte 7: Byte Count Register

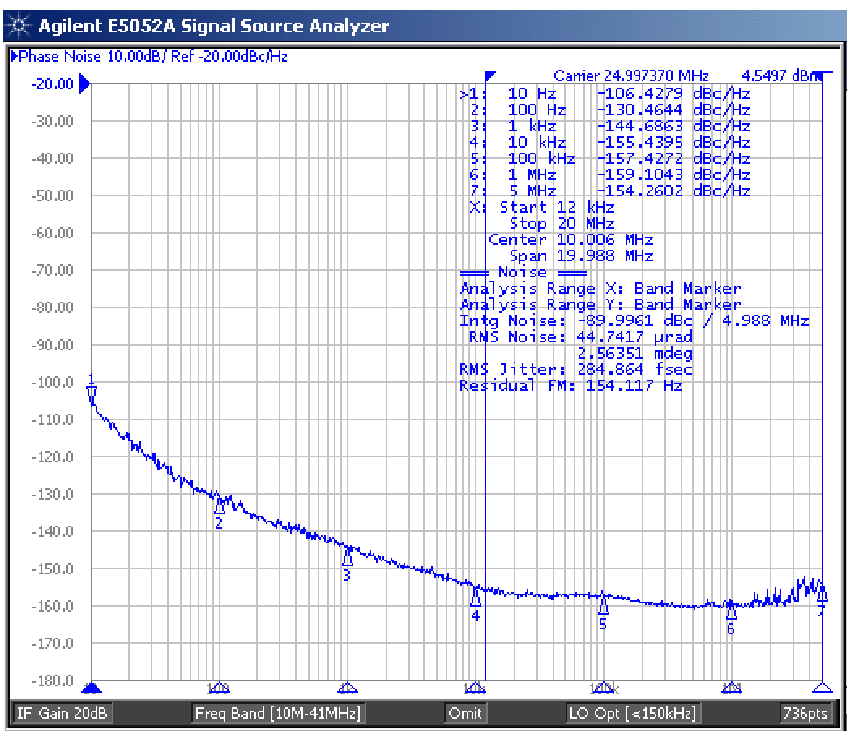
Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			0		
5	Reserved			0		
4	BC4	Byte count programming	RW	0	Writing to this register will configure how many bytes will be read back, default is 8 bytes	
3	BC3		RW	1		
2	BC2		RW	0		
1	BC1		RW	0		
0	BC0		RW	0		

Plots

100MHz HCSL Clock



25MHz CMOS Clock



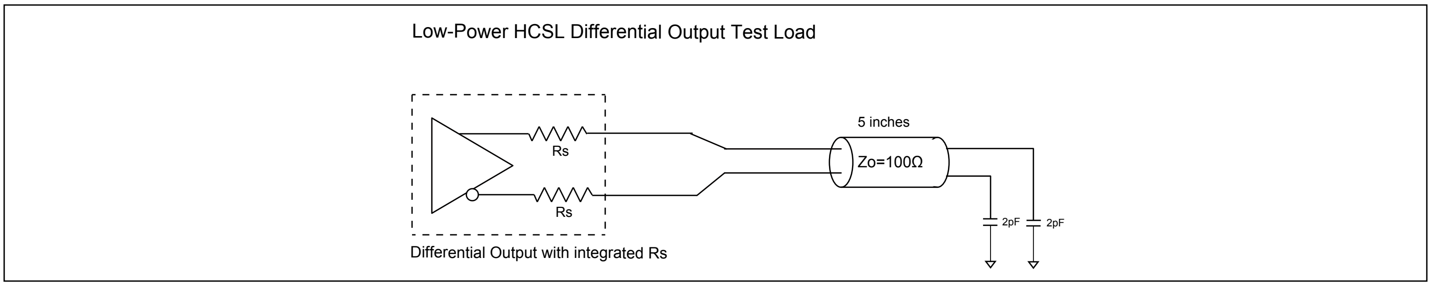


Figure 1. Low Power HCSL Test Circuit

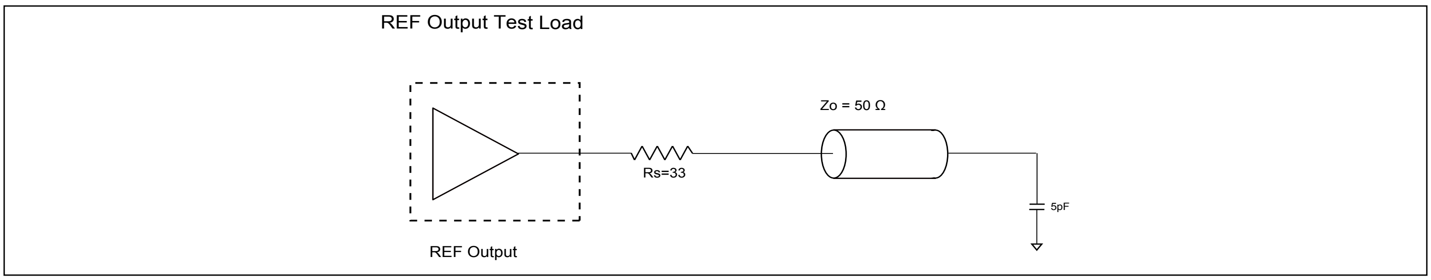


Figure 2. CMOS REF Test Circuit

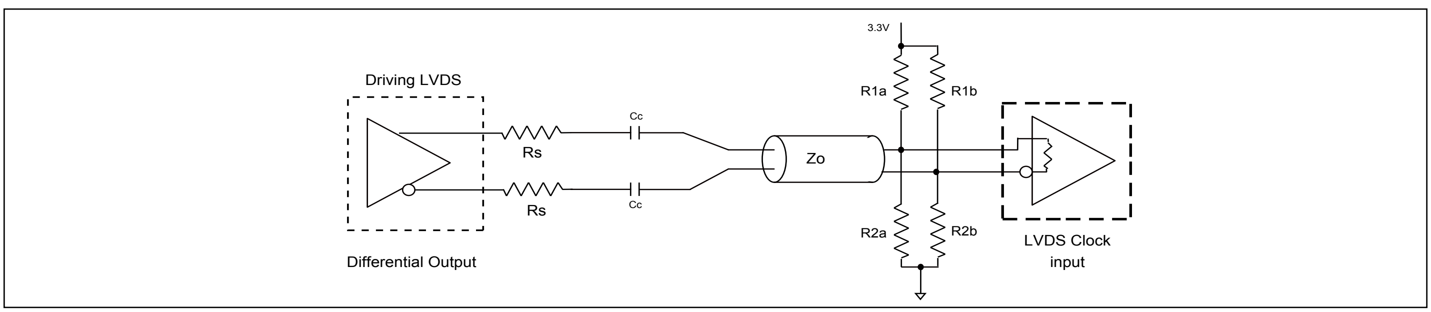


Figure 3. Differential Output driving LVDS

Alternate Differential Output Terminations

Component	Receiver with termination	Receiver without termination	Unit
R_{1a}, R_{1b}	10,000	140	Ω
R_{2a}, R_{2b}	5,600	75	Ω
C_C	0.1	0.1	µF
V_{CM}	1.2	1.2	V

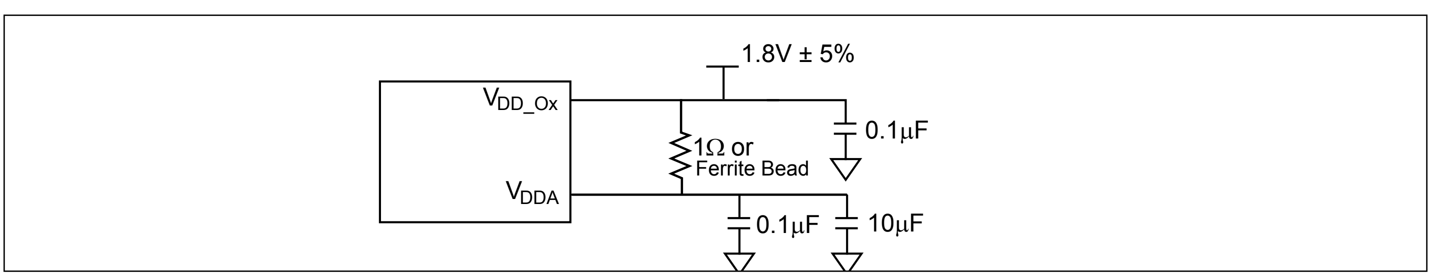
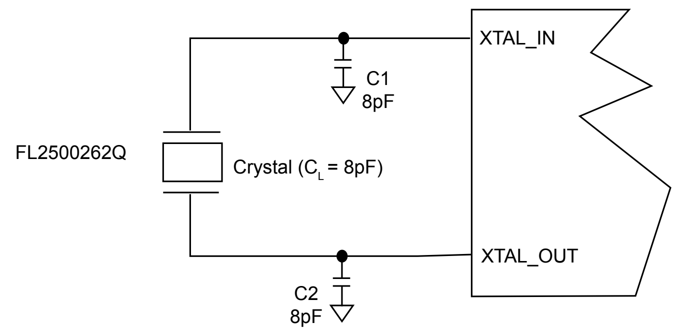


Figure 4. Power Supply Filter

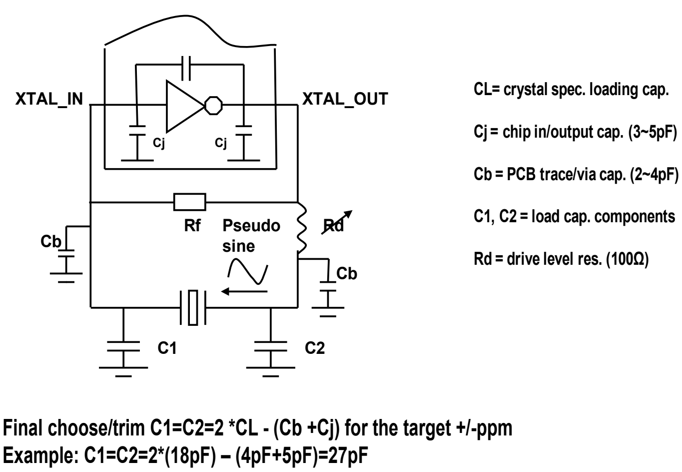
Crystal Circuit Connection

The following diagram shows PI6CG182Q crystal circuit connection with a parallel crystal. For the CL=8pF crystal, it is suggested to use C1=8pF, C2=8pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts based on the following formular in the Crystal Capacitor Calculation diagram.

Crystal Oscillator Circuit



Crystal Capacitor Calculation



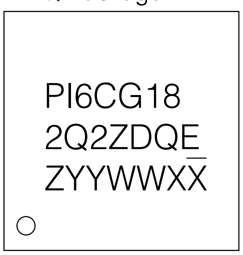
Recommended Crystal Specification

Diodes Recommends:

a) FL2500262Q, SMD 3.2x2.5(4P), 25MHz, CL=8pF, +/-50ppm, https://www.diodes.com/assets/Datasheets/FL.pdf
b) FW2500054Q, SMD 2.0x1.6(4P), 25MHz, CL=8pF, +/-50ppm, https://www.diodes.com/assets/Datasheets/FW.pdf

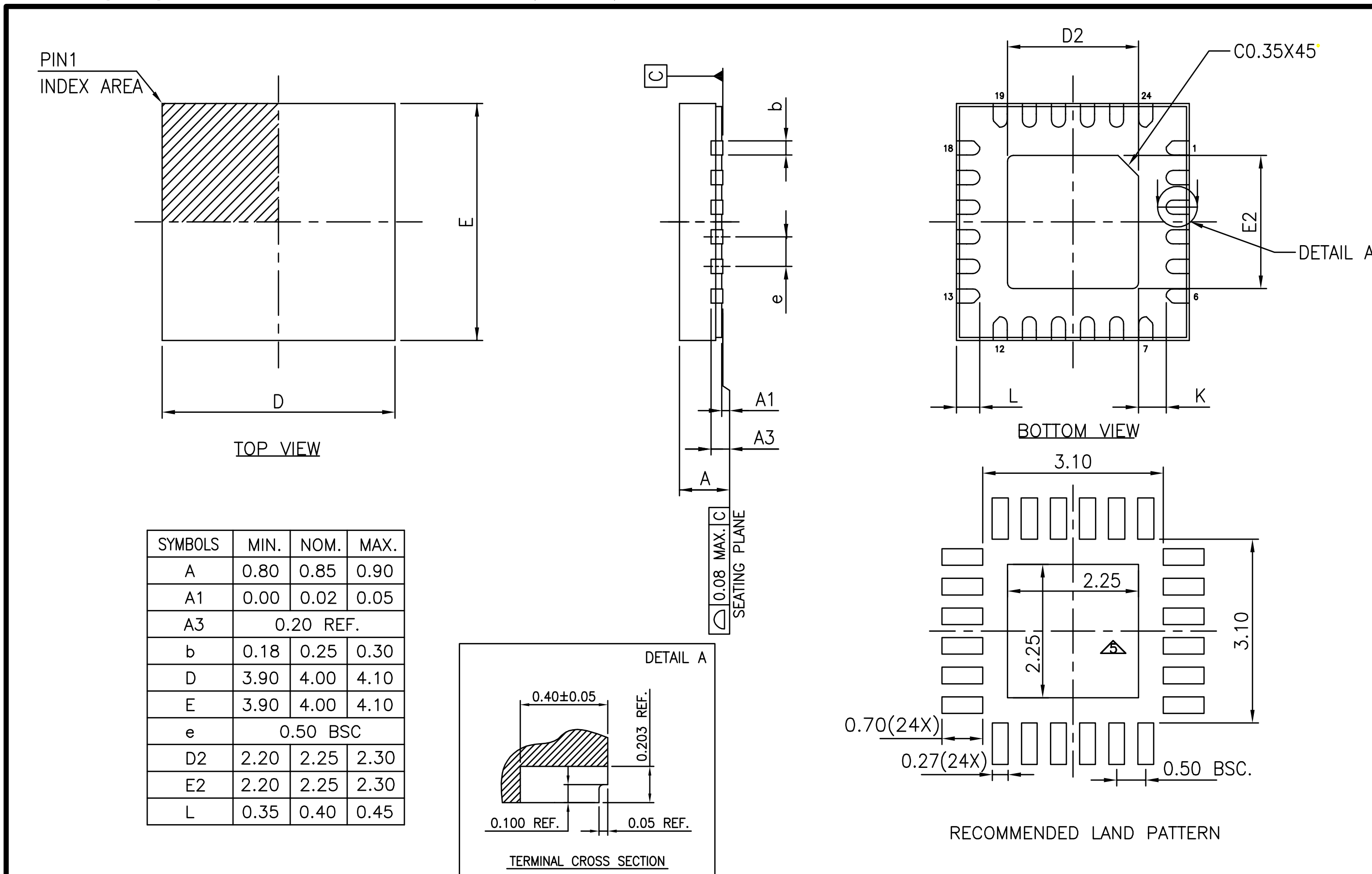
Part Marking

ZDQ Package



Z: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Packaging Mechanical: 24-TQFN (ZDQ)



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.18	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.50 BSC		
D2	2.20	2.25	2.30
E2	2.20	2.25	2.30
L	0.35	0.40	0.45

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO−220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA

DATE: 11/23/17

DESCRIPTION: 24-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZDQ (ZDQ24)

DOCUMENT CONTROL #: PD-2236 **REVISION: --**

17-0144

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information(1-3)

Ordering Code	Package Code	Package Description	Operating Temperature
PI6CG182Q2ZDQEX	ZDQ	24-contact, Very Thin Quad Flat No-Lead (TQFN)	-40 to 105 °C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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