A product Line of
Diodes Incorporated

PERICOM®

PI6LC58S1101

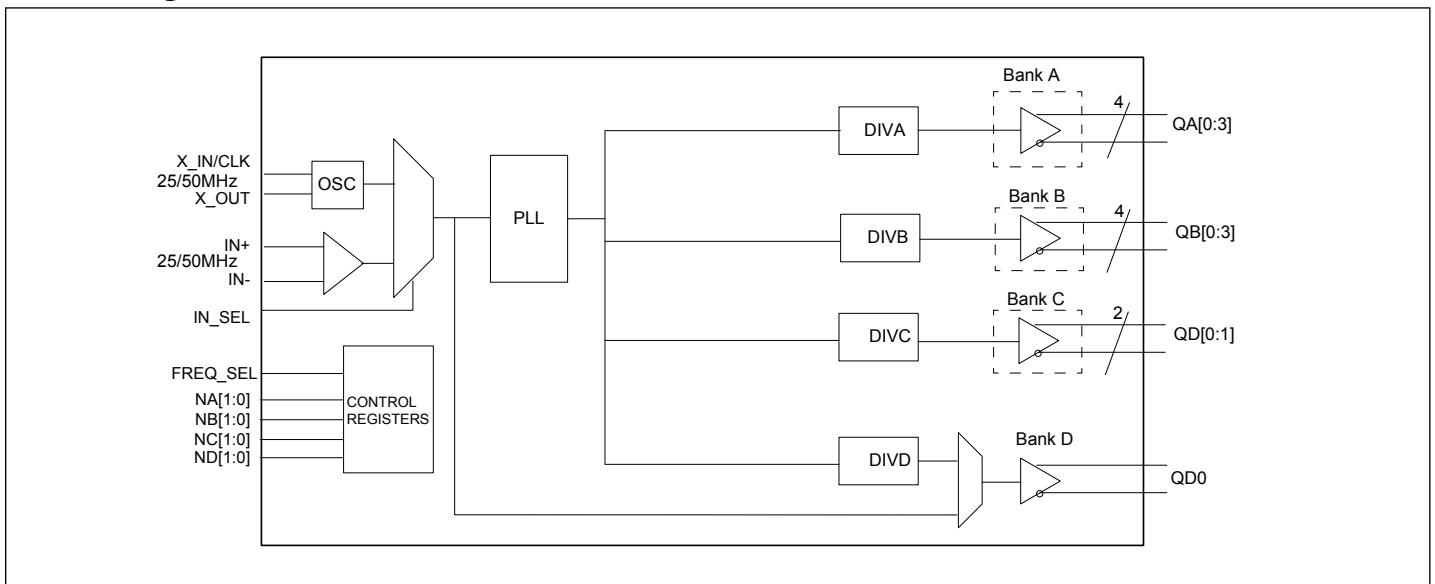## 11 Outputs HiFlex™ Ethernet Network Clock Generator

Features

➔ 3.3V Supply Voltage
➔ Crystal/CMOS Input: 25MHz/50MHz
➔ Differential Input: 25MHz/50MHz
➔ Selectable Output Frequencies
➔ Four Output Banks with Selectable Output Signaling: LVPECL or LVDS
➔ Very low RMS Phase jitter: 0.08ps (typ.), 156.25MHz (10kHz to 20MHz)
➔ Excellent phase noise: -145dBc/Hz, 156.25MHz at 100kHz offset
➔ Power Supply Noise Rejection: -55dBc
➔ Industrial Temperature Support: -40°C to 85°C
➔ Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
➔ Halogen and Antimony Free. "Green" Device (Note 3)
➔ For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
https://www.diodes.com/quality/product-definitions/
➔ Packaging (Pb-free & Green): 64-lead 9mm × 9mm TQFN

Description

The PI6LC58S1101 is very low jitter clock generator target for applications that demand extremely low phase noise, such as 10GbE, 40GbE, 100GbE, and 400GbE. It uses Diodes' proprietary LC VCO-based PLL design to achieve an optimum combination of those popular networking clock frequencies and low phase noise performance along with high power supply noise rejection.

The PI6LC58S1101 has four output banks which can be configured independently for different frequencies and different output signaling types based on control pins. The pin control method provides an easy way to configure the device at the hardware level.
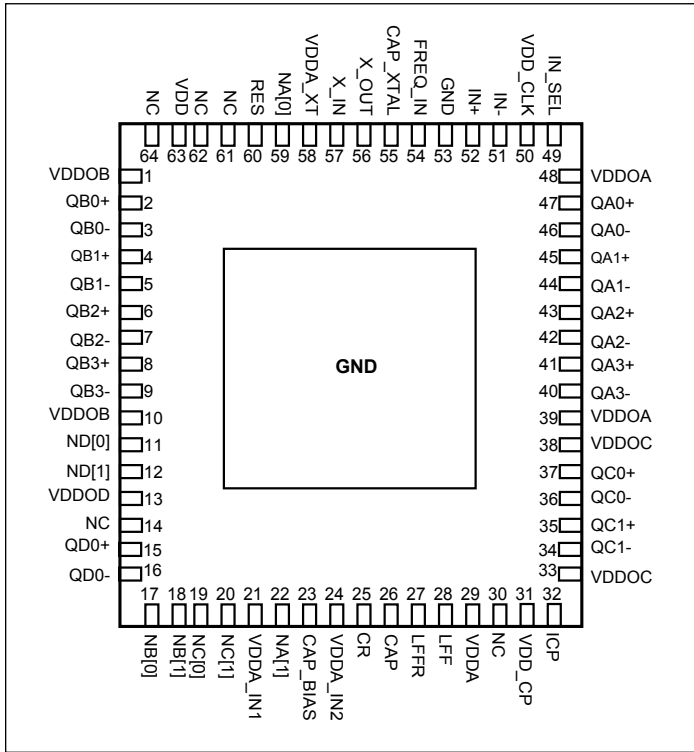
Block Diagram

Pin Configuration

Pin Description

Pin #	Pin Name	Type		Description
1	VDDOB	Power	—	Power supply voltage for output Bank B
2	QB0+	Output	—	Bank B, Differential clock output, LVPECL or LVDS
3	QB0-	Output	—	Bank B, Differential clock output, LVPECL or LVDS
4	QB1+	Output	—	Bank B, Differential clock output, LVPECL or LVDS
5	QB1-	Output	—	Bank B, Differential clock output, LVPECL or LVDS
6	QB2+	Output	—	Bank B, Differential clock output, LVPECL or LVDS
7	QB2-	Output	—	Bank B, Differential clock output, LVPECL or LVDS
8	QB3+	Output	—	Bank B, Differential clock output, LVPECL or LVDS
9	QB3-	Output	—	Bank B, Differential clock output, LVPECL or LVDS
10	VDDOB	Power	—	Power supply voltage for output Bank B
11	ND[0]	Input	Pullup/ Pulldown	Control input for output Bank D. 3-level signals
12	ND[1]	Input	Pullup/ Pulldown	Control input for output Bank D. 3-level signals
13	VDDOD	Power	—	Power supply voltage for output Bank D
14	NC	—	—	No Connect.
15	QD0+	Output	—	Bank D, Differential clock output, LVPECL or LVDS
16	QD0-	Output	—	Bank D, Differential clock output, LVPECL or LVDS

Pin Description Cont.

Pin #	Pin Name	Type		Description
17	NB[0]	Input	Pullup/ Pulldown	Control input for output Bank B. 3-level signals
18	NB[1]	Input	Pullup/ Pulldown	Control input for output Bank B. 3-level signals
19	NC[0]	Input	Pullup/ Pulldown	Control input for output Bank C. 3-level signals
20	NC[1]	Input	Pullup/ Pulldown	Control input for output Bank C. 3-level signals
21	VDDA_IN1	Power	—	Analog Power supply voltage for PLL
22	NA[1]	Input	Pullup/ Pulldown	Control input for output Bank A. 3-level signals
23	CAP_BIAS	Analog	—	Internal VCO bias decoupling capacitor. Use a 4.7μF capacitor between the CAP_BIAS and GND
24	VDDA_IN2	Power	—	Analog Power supply voltage for PLL
25	CR	Analog	—	1uF decoupling capacitor between CR amd VDDA
26	CAP	Analog	—	4.7uF Decoupling capacitor
27	LFFR	Analog	—	Ground return path for PLL loop filter
28	LFF	Output	—	Loop filter/ charge pump output for PLL. Connect to external loop filter
29	VDDA	Power	—	Analog Power supply voltage for PLL
30	NC	—	—	No Connect
31	VDD_CP	Power	—	Analog power supply for charge pump
32	ICP	Analog	—	Charge pump current input, connect to LFF pin 28
33	VDDOC	Power	—	Power supply voltage for output Bank C
34	QC1-	Output	—	Bank C, Differential clock output, LVPECL or LVDS
35	QC1+	Output	—	Bank C, Differential clock output, LVPECL or LVDS
36	QC0-	Output	—	Bank C, Differential clock output, LVPECL or LVDS
37	QC0+	Output	—	Bank C, Differential clock output, LVPECL or LVDS
38	VDDOC	Power	—	Power supply voltage for output Bank C
39	VDDOA	Power	—	Power supply voltage for output Bank A
40	QA3-	Output	—	Bank A, Differential clock output, LVPECL or LVDS
41	QA3+	Output	—	Bank A, Differential clock output, LVPECL or LVDS
42	QA2-	Output	—	Bank A, Differential clock output, LVPECL or LVDS
43	QA2+	Output	—	Bank A, Differential clock output, LVPECL or LVDS
44	QA1-	Output	—	Bank A, Differential clock output, LVPECL or LVDS
45	QA1+	Output	—	Bank A, Differential clock output, LVPECL or LVDS
46	QA0-	Output	—	Bank A, Differential clock output, LVPECL or LVDS
47	QA0+	Output	—	Bank A, Differential clock output, LVPECL or LVDS
48	VDDOA	Power	—	Power supply voltage for output Bank A

Pin Description Cont.

Pin #	Pin Name	Type		Description
49	IN_SEL	Input	Pulldown	Selects input reference source. LVCMOS interface levels. 0 = Crystal input on pins X_IN, X_Out (default) 1 = Reference clock input on pins IN+, IN-
50	VDD_CLK	Power	—	Power supply voltage for input IN+, IN-
51	IN-	Input	Pullup/ Pulldown	Differential clock input Internal resistor bias to VDD_CLK/2
52	IN+	Input	Pulldown	Differential clock input
53	GND	Power	—	Connect to Ground
54	FREQ_IN	—	Pullup/ Pulldown	Input frequency select. 3-level signals
55	CAP_XTAL	Analog	—	Crystal oscillator circuit decoupling capacitor. Use a 4.7µF capacitor between the CAP_XTAL and the GND terminals.
56	X_OUT	Output	—	Crystal out
57	X_IN	Input	—	Crystal in, the input also supports being driven by a single-ended crystal oscillator or reference clock
58	VDDA_XT	Analog	—	Analog power supply voltage for the crystal oscillator
59	NA[0]	Input	Pullup/ Pulldown	Control input for output Bank A. 3-level signals
60	RES	—	—	2.8kΩ (1%) resistor to Ground
61	NC	—	—	No Connect
62	NC	—	—	No Connect
63	VDD	Power	—	Power supply
64	NC	—	—	No Connect
Epad	Ground	Power	—	Connect to Ground

Input MUX Selection

IN_SEL	Input Source
0	Crystal Input (X_IN, X_OUT)
1	Differential Input (IN+, IN-)

Input Frequency Selection

FREQ_IN	Input Source
High	Reserved
Middle	25MHz
Low	50MHz

Bank A Differential Output Control

NA[1]	NA[0]	Output Types	Output Frequency (MHz)
Low	Low	LVPECL	156.25
Low	Middle	LVPECL	125
Low	High	LVPECL	100
Middle	Low	LVPECL	25
Middle	Middle	Power Down, both outputs of the differential output pair will drive a logic-high level	
Middle	High	LVDS	156.25
High	Low	LVDS	125
High	Middle	LVPECL	312.5
High	High	Reserved	

Bank B Differential Output Control

NB[1]	NB[0]	Output Types	Output Frequency (MHz)
Low	Low	LVPECL	156.25
Low	Middle	LVPECL	125
Low	High	LVPECL	100
Middle	Low	LVPECL	25
Middle	Middle	Power Down, both outputs of the differential output pair will drive a logic-high level	
Middle	High	LVDS	156.25
High	Low	LVDS	125
High	Middle	LVPECL	312.5
High	High	LVPECL	50

Bank C Differential Output Control

NC[1]	NC[0]	Output Types	Output Frequency (MHz)
Low	Low	LVPECL	312.5
Low	Middle	LVPECL	156.25
Low	High	LVPECL	125
Middle	Low	LVPECL	25
Middle	Middle	Power Down, both outputs of the differential output pair will drive a logic-high level	
Middle	High	LVDS	125
High	Low	LVDS	100
High	Middle	LVPECL	50
High	High	LVDS	156.25

Bank D Differential Output Control

ND[1]	ND[0]	Output Types	Output Frequency (MHz)
Low	Low	LVDS	156.25
Low	Middle	LVDS	125
Low	High	LVDS	100
Middle	Low	LVPECL	156.25
Middle	Middle	Power Down, both outputs of the differential output pair will drive a logic-high level	
Middle	High	LVPECL	100
High	Low	LVPECL	25
High	Middle	LVPECL	125
High	High	LVPECL	fin

PLL Loop Bandwidth and Loop Filter

The PI6LC58S1101 PLL requires an external loop filter. The components of the filter are connected in between the ICP (pin32) and LFFR (pin27). PLL loop bandwidth generally depends on the loop components, charge pump current, PFD frequency, and VCO gain. For the best results, we recommend the following values for the components: C1=200pF, C2=0.1uF, and R2=150Ω.
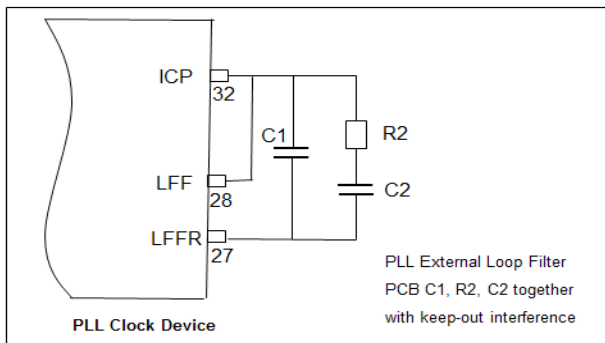
Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.. –65°C to +150°C
Supply Voltage to Ground Potential, V_{DD}, V_{DDA} V_{DDOx} –0.5V to +3.8V
Input Voltage .... –0.5V to V_{DD} Max, not exceed 3.8V
SMBus, Input High Voltage 3.6V
ESD Protection (HBM) .... 2000 V
Junction Temperature .... 125°C max

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Core Power Supply Voltage	—	3.135	3.3	3.465	V
V_{DDOX}	Output Power Supply Voltage	—	3.135	3.3	3.465	V
V_{DDA}	Analog Power Supply Voltage	—	3.135	3.3	3.465	V
I_{DD}	Power Supply Current	—	—	—	85	mA
I_{DDO}	Power Supply Current for Outputs	All outputs loaded, Diff. Outputs are LVPECL	—	—	850	mA
		All outputs loaded, Diff. Outputs are LVDS	—	—	650	mA
I_{DDA}	Analog Power Supply Current	—	—	—	180	mA
T_A	Ambient Temperature	—	–40	—	85	°C

Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
R_{pu}	Internal Pullup Resistance	—	—	51	—	KΩ
R_{dn}	Internal Pulldown Resistance	—	—	51	—	KΩ
R_{dn}	Internal Pulldown Resistance	IN_SEL	—	100	—	KΩ
C_{XTAL}	Internal capacitance on X_IN and X_OUT pins	—	—	12	—	pF

LVCMOS DC Electrical Characteristics for 2- Level Pins

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	V_{DD} = 3.3V ±5%	0.7x V_{DD}	—	V_{DD} +0.3	V
V_{IL}	Input Low Voltage	V_{DD} = 3.3V ±5%	-0.3	—	0.3x V_{DD}	V
I_{IH}	Input High Current	V_{IN} = $V_{DD\,max.}$	—	—	150	μA
I_{IL}	Input Low Current	V_{IN} = 0V	-150	—	—	μA
T_{DC}	Input Duty Cycle	—	40	—	60	%
C_{IN}	Input Capacitance	—	—	3.5	—	pF

LVCMOS DC Electrical Characteristics for 3- Level Pins

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	V_{DD} = 3.3V ±5%	$0.7 \times V_{DD}$	—	3.465	V
V_{IM}	Input Middle Voltage	V_{DD} = 3.3V ±5%	$0.4 \times V_{DD}$	—	$0.6 \times V_{DD}$	V
V_{IL}	Input Low Voltage	V_{DD} = 3.3V ±5%	-0.3	—	$0.3 \times V_{DD}$	V
I_{IH}	Input High Current	$V_{IN} = V_{DD \, max.}$	—	—	150	µA
I_{IH}	Input Middle Current	$V_{IN} = V_{DD}$ /2	—	±1	—	µA
I_{IL}	Input Low Current	V_{IN} = 0V	-150	—	—	µA

Differential Input DC Characteristics

Symbol	Parameters	Conditions	Min..	Typ.	Max.	Units
V_{IH}	Input High Voltage	—	—	—	V_{DD} - 0.7	V
V_{IL}	Input Low Voltage	—	V_{DD} - 2.0	—	—	V
V_{CM}	Input Bias Voltage	—	1.1	—	V_{DD} - 0.3	V
V_{IN-PP}	Input Differential Swing	Differential peak to peak	0.2	—	1.4	V

Crystal Characteristic

Parameters	Description	Min.	Typ	Max.	Units
OSCmode	Mode of Oscillation	Fundamental			
FREQ	Frequency	—	25	50	MHz
ESR[1]	Equivalent Series Resistance	—	—	50	Ω
Cload	Load Capacitance, 50MHz crystal	—	8	12	pF
	Load Capacitance, 25MHz crystal	—	12	22	pF
Cshunt	Shunt Capacitance	—	—	7	pF
	Drive Level	—	—	250	uW

Note: 1. ESR value is dependent upon frequency of oscillation

LVPECL Output DC Characteristics[1]

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{OPP}	Output Peak-Peak Voltage	Single-ended	—	0.78	—	V
V_{OH}	Output High Voltage	Outputs terminated with 50Ω to V_{DD_OX} - 2V	V_{DDOX} - 1.4	—	V_{DDOX} - 0.7	V
V_{OL}	Output Low Voltage		V_{DDOX} - 2.0	—	V_{DDOX} - 1.3	V

LVDS Output DC Characteristics

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{OPP}	Output Peak-peak Voltage	Single-ended	0.247	—	0.530	V
DV_{OPP}	V_{OPP} Magnitude Change	—	—	—	50	mV
V_{OS}	Output Offset Voltage	—	1.9	—	2.7	V
DV_{OS}	V_{OS} Magnitude Change	—	—	—	50	mV

AC Output Characteristics (see test circuit)[1]

T_A=-40°C to 85°C; V_{DD}=3.3V±5%, V_{DD_O}=3.3V±5%

Symbol	Parameters	Condition		Min.	Typ.	Max.	Units
f_{OUT}	Output Frequency	LVPECL		—	—	156.25	MHz
		LVDS		—	—	156.25	MHz
$t_{R\,/\,tF}$	Rise and Fall Time; 20% ~ 80%	LVPECL, LVDS		—	100	200	ps
t_{DC}	Duty Cycle	LVPECL, LVDS		45	—	55	%
tj_{PHASE}	Integrated-Phase Jitter (RMS)	10kHz-20MHz @ 156.25MHz, 25MHz Xtal input, with ELF		—	0.08	0.12	ps
tj_{c-c}	Cycle-to-Cycle Jitter	—		—	28	30	ps
tj_{Pk-Pk}	Peak-to-Peak jitter	—		—	30	35	ps
f_N	Single-Side Band Phase Noise	156.25MHz, 25MHz Xtal input	Offset 1kHz	—	-130	—	dBc/Hz
			Offset 10kHz	—	-140	—	
			Offset 100kHz	—	-145	—	
			Offset 1MHz	—	-150	—	
			Offset 10MHz	—	-160	—	
PSNR	Power Supply Noise Rejection	V_{DD}, 50mVpp, 10k-15MHz		—	-65	—	dBc
		V_{DDA}, 50mVpp, 10k-15MHz		—	-65	—	
		V_{DD_Ox}, 50mVpp, 10k-15MHz		—	-55	—	
$t_{STARTUP}$	Start Time[1]	—		—	—	175	ms
t_{LOCK}	PLL Lock Time	—		—	—	20	ms

Note:

1. Startup time is dependent on the capacitor value of CR (pin 25).

LVPECL/LVDS Buffer
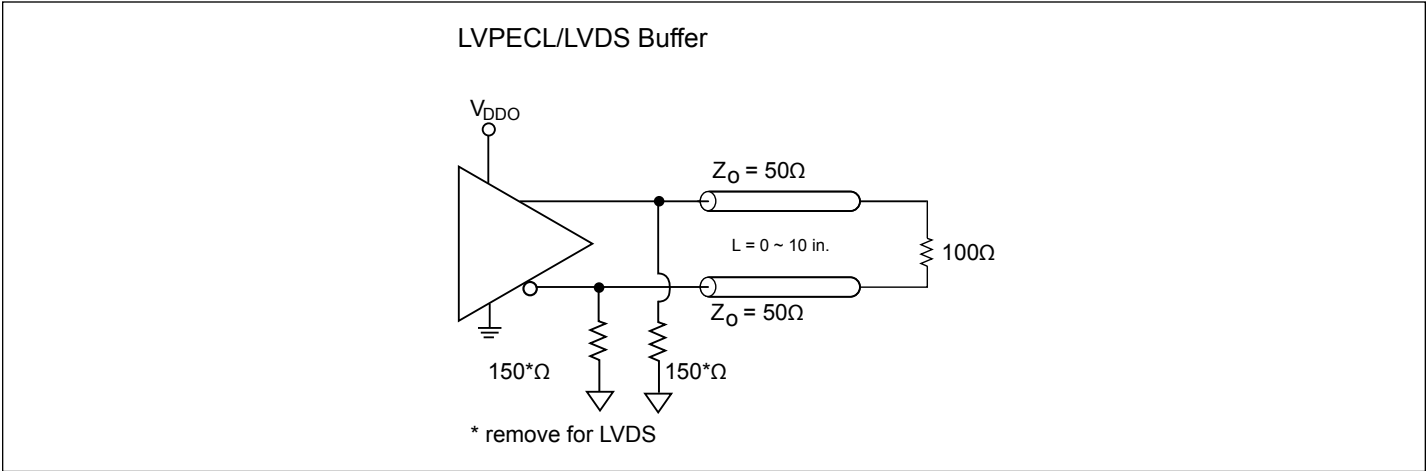
Figure 1. LVPECL and LVDS Test Circuit

Application Information

Recommendations for Unused Input and Output Pins

Crystal Inputs:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. A 1kΩ resistor can be tied from XTAL_IN to ground for additional protection.

Reference Inputs: IN+/IN-

They can be left floating if not used. Connect them 1k to GND can provide additional protection.

LVCMOS Control Pins:

All control pins have internal pulldowns; A 1kΩ resistor tied from each control pin to ground can provide additional protection.

Outputs:

All unused are suggested to leave open in NC without any trace. This can save the IC supply power and with mini. EMI radiation.

Crystal Circuit Connection

The following diagram shows PI6LC58S1101 crystal circuit connection with a parallel crystal. For the CL=12pF crystal, it is suggested to use C1=12pF, C2=12pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.
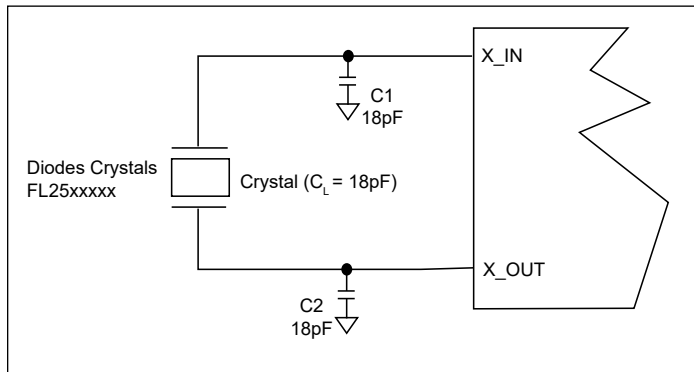
Figure 2. Crystal Oscillator Circuit

Recommended Crystal Specification

Diodes recommends:

a) FL2500158, SMD 3.2x2.5(4P), 25MHz, CL=12pF, +/-20ppm, -40 to 85C. http://www.pericom.com/pdf/datasheets/se/FL.pdf
b) FL2500221, SMD 3.2x2.5(4P), 25MHz, CL=12pF, +/-25ppm, -40 to 85C. http://www.pericom.com/pdf/datasheets/se/FL.pdf

Placement & Routing

VDD Pin

0.1μF bypass capacitors should be used for each VDD pin, a 1uF capacitor in parallel can be used for better decoupling. The decoupling capacitor on component side has better decoupling filter result. So place the 0.1uF capacitor as close to the device as possible as shown in Figure 3.
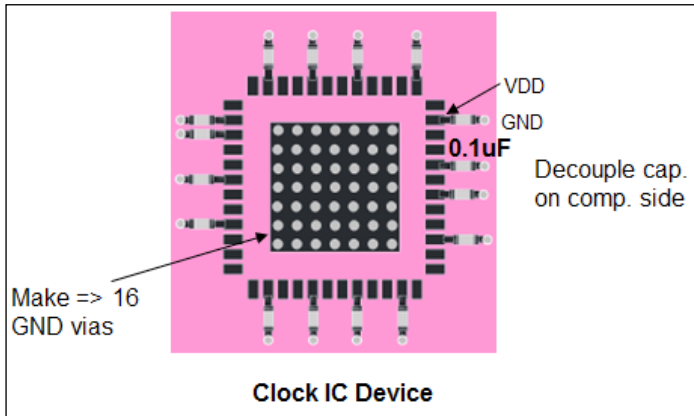
Figure 3. Layout guidance for VDD decoupling

Thermal Pad Vias

Thermal pad provides a heat dissipation path for device to GND plane. The vias count density design is from 1mm to 1.25mm. For example, a 6x6mm thermal pad land pattern can have $(6/1.25)^2=25$ vias. The via diameter guide can be found from a PCB assemble manufacture, for example, 0.3 to 0.33mm for 1oz. copper. Please check with the manufacturer for details.

Crystal Input

Design external load cap.: C1=C2=2 *CL –cap(Xin)/2- C_stray to be equal to crystal datasheet CL equivalent. This device Xin pin cap=12pF. Typical PCB C_stray = 5pF.

For crystal frequency =25MHz or higher, C1=C2=2*(CL-6) is a good formula to start with, but always check datasheet for crystal recommendation. The C1 and C2 value can be fine tune by (6ppm/1pF) for more accurate ppm during board bring up.

A good PCB layout can eliminate the most C_stray and OSC IC Xin pin is the most sensitive pin as crystal amplifier input, so make narrow trace routing loop between Xin/Xout pins to crystal with load capacitors (C1/C2) GND close crystal pins on top PCB layer. The 2nd layer GND plane must be continuously underneath the crystal layout with a keep-out (>200mil) of any board trace and vias around to prevent any board noises crosstalk as shown in Figure 4.
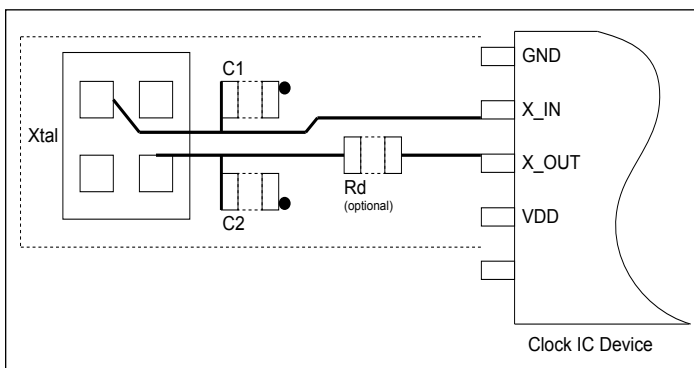
Figure 4. Crystal load capacitor

X_IN/CMOS Input

X_IN pin can be treated as CMOS input pin for CMOS input if its inut V_swing is full rail VDD of clock IC. The X_OUT pin leaves open. For lower V_swing, i.e. less than VDD input, AC coupling to X_IN is recommended.
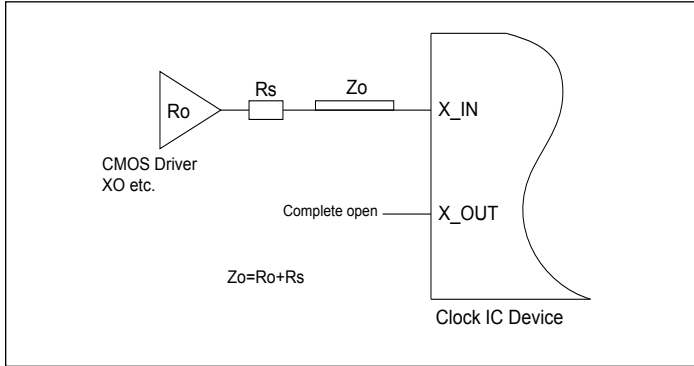
Figure 5. 25/50MHz CMOS XO Drive X_IN

Differential Clock Input

LVPECL and LVDS XO drive this IC need equivalent 100ohm differential termination with a 100ohm R cross IN+/IN- pins. If use AC coupling drive, AC must be in front of that 100ohm cross. LVDS XO does not need TX side 150ohm pull-down as shown in Figure 6.
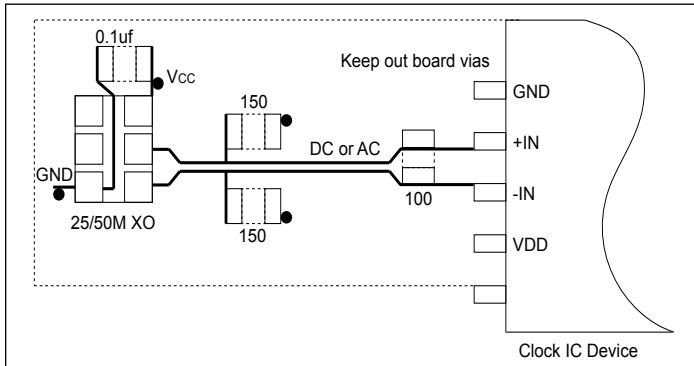
Figure 6. Differential XO Drive IN+/IN-

Output Clock Routing Design

Clock timing is the most important component in PCB design, so its trace routing must be planned and routed with the highest priority by manual routing. For example, control minimum total trace vias count is less tna 3~4; use independent layer with good reference plane and keep enough space from other signal trace (>20mil. at least) etc. The termination can be referenced to Figure 7.

Power Supply Decoupling Consideration

There are several power supply pins including VDDA, VDDA_IN1, VDDA_IN2, VDDA_XT, VDD, VDD_CLK, VDD_CP. VDDOA, VDDOB, and VDDOC . Power supply pins need to follow the decoupling suggestions in figure 7. This device has other critical pins which connect capacitors either to GND or between them. Pin 24 and 27 are connected with 4.7uF to GND, and pin 26 and 30 needs a 1uF cross them after pin 30 a 22uF to GND.
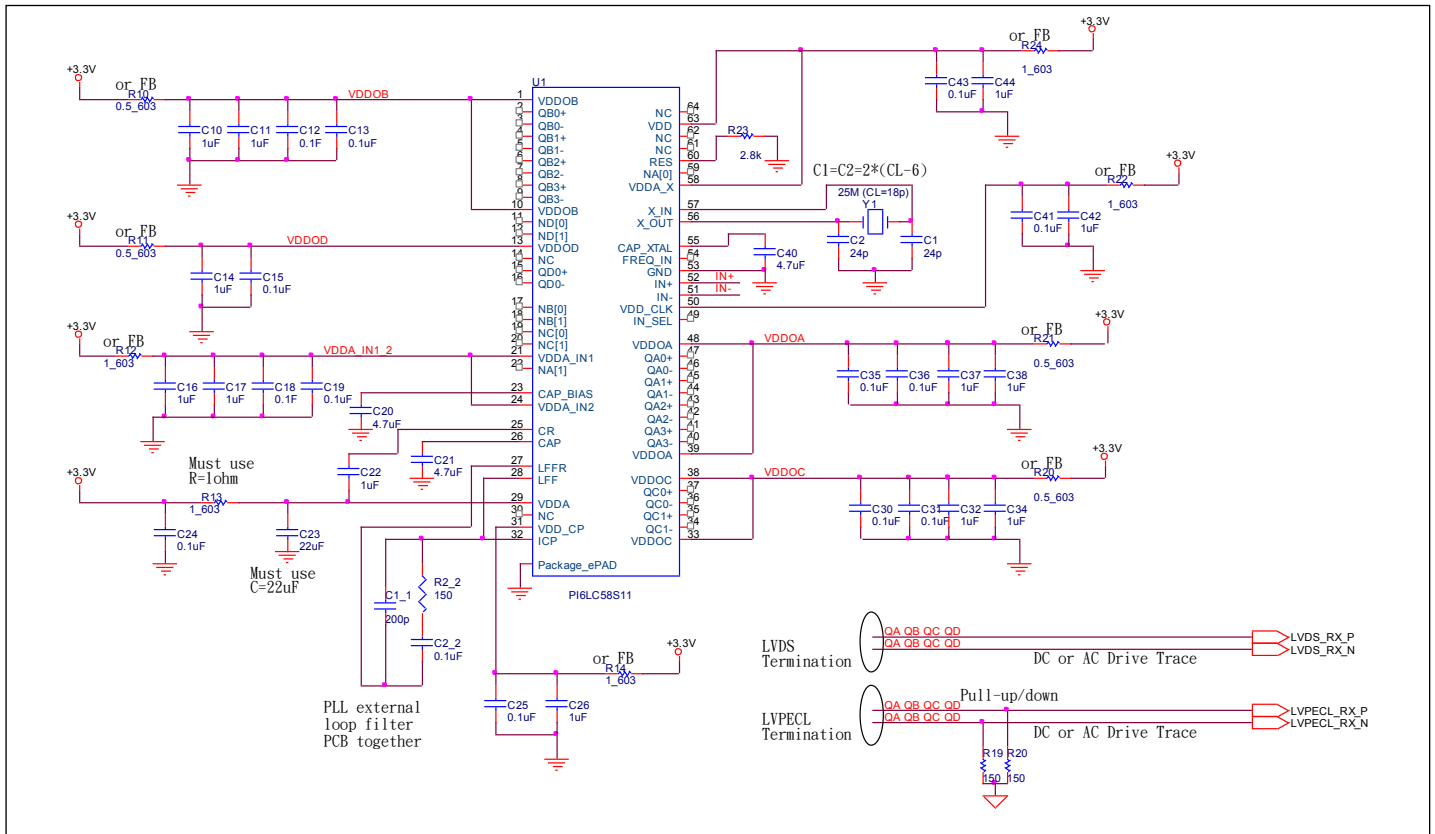
Figure 7. Power supply and other critical pins decoupling reference

Phase Noise Plots
156.25MHz LVPECL Clock
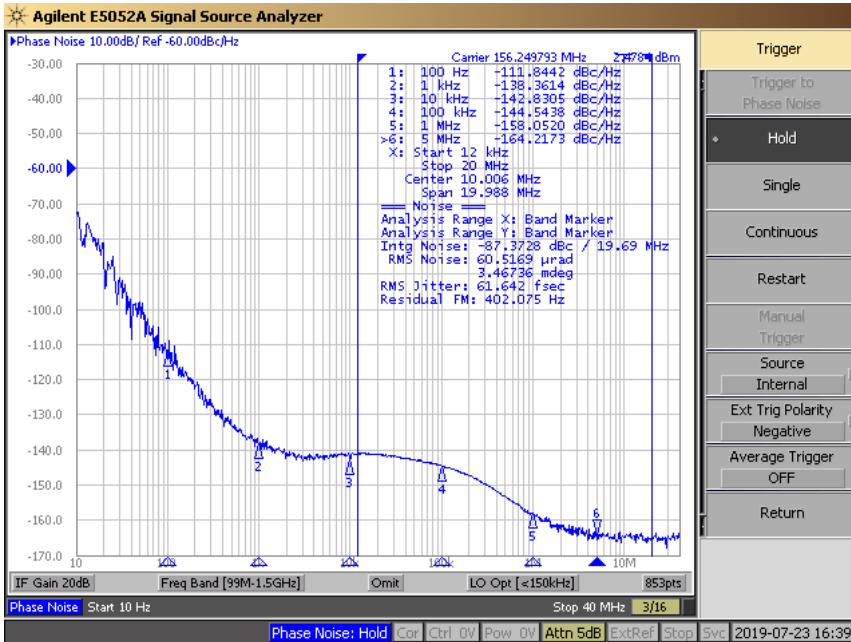
Part Marking

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

Packaging Mechanical: 64-TQFN (ZD)

SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.18	0.25	0.30
D	8.90	9.00	9.10
E	8.90	9.00	9.10
e	0.50 BSC.		
K	1.10 REF.		
D2	5.95	6.00	6.05
E2	5.95	6.00	6.05
L	0.35	0.40	0.45

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

DATE: 05/18/18

DESCRIPTION: 64-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZD (ZD64)

DOCUMENT CONTROL #: PD-2036   **REVISION: D**

For latest package information:

See https://www.diodes.com/assets/MediaList-Attachments/Diodes-Package-Information.pdf

Ordering Information

Ordering Code	Package Code	Package Description	Operating Temperature
PI6LC58S1101ZDIEX	ZD	64-Contact, Very Thin Quad Flat No-Lead (TQFN)	Industrial

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel

IMPORTANT NOTICE

LIFE SUPPORT

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