Dual Bidirectional I2C-bus and SMBus Voltage-Level Translator

Features

- 2-bit bidirectional translator for SDA and SCL lines in mixed-mode I2C-bus applications
- Standard-mode, Fast-mode, and Fast-mode Plus I2C-bus and SMBus compatible
- Less than 1.5 ns maximum propagation delay to accommodate Standard mode and Fast mode I2C-bus devices and multiple masters
- Allows voltage level translation between:
  - 0.9V VREF1 and 1.8 V, 2.5 V, 3.3 V or 5 V VREF2
  - 1.2 V VREF1 and 1.8 V, 2.5 V, 3.3 V or 5 V VREF2
  - 1.5 V VREF1 and 2.5 V, 3.3 V or 5 V VREF2
  - 1.8 V VREF1 and 3.3 V or 5 V VREF2
  - 2.5 V VREF1 and 5 V VREF2
  - 3.3 V VREF1 and 5 V VREF2
- Provides bidirectional voltage translation with no direction pin
- Low 3.5 ohm ON-state connection between input and output ports provides less signal distortion
- Open-drain I2C-bus I/O ports (SCL1, SDA1, SCL2 and SDA2)
- 5 V tolerant I2C-bus I/O ports to support mixed-mode signal operation
- High-impedance SCL1, SDA1, SCL2 and SDA2 pins for EN = LOW
- Lock-up free operation for isolation when EN = LOW
- Flow through pin out for ease of printed-circuit board trace routing
- ESD protection exceeds 4KV HBM per JESD22-A114
- Package: TDFN2x3-8L, MSOP-8L,SOIC-8L

Description

The PI6ULS5V9306 is a dual bidirectional I^2C-bus and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.0 V to 3.3 V (VREF1) and 1.8 V to 5.5 V(VREF2).

The PI6ULS5V9306 allows bidirectional voltage translations between 1.0 V and 5 V without the use of a direction pin. The low ON-state resistance (Ron) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports.

The PI6ULS5V9306 is not a bus buffer that provides both level translation and physically isolates to either side of the bus when both sides are connected. The PI6ULS5V9306 only isolates both sides when the device is disabled and provides voltage level translation when active.

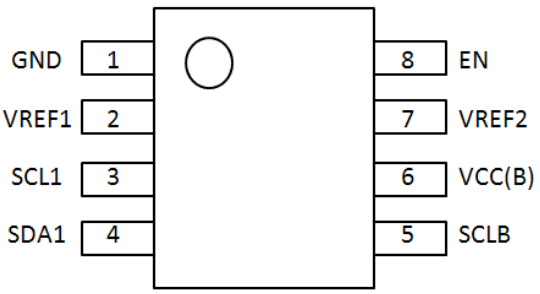
The PI6ULS5V9306 can also be used to run two buses, one at 400 kHz operating frequency and the other at 100 kHz operating frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated when the 400 kHz operation of the other bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the translator.

As with the standard I^2C-bus system, pull-up resistors are required to provide the logic HIGH levels on the translator's bus. The PI6ULS5V9306 has a standard open-collector configuration of the I^2C-bus. The size of these pull-up resistors depends on the system, but each side of the translator must have a pull-up resistor. The device is designed to work with Standard-mode, Fast-mode and Fast mode Plus I^2C-bus devices in addition to SMBus devices.

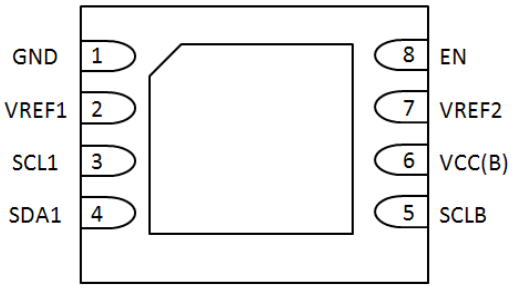
When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low resistance connection exists between the SDA1 and SDA2 ports. When the higher voltage is on the SDA2 port, and the SDA2 port is HIGH , the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull-up supply voltage (VDPU) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

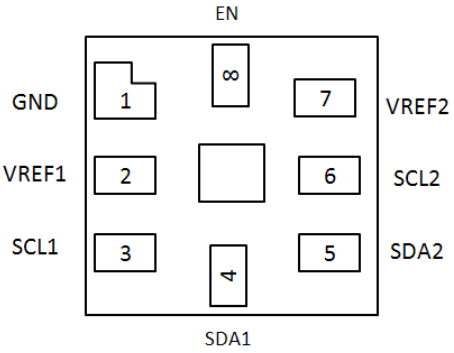
Pin Configuration



MSOP-8L/SOIC-8L(Top View)



TDFN2x3-8L(Top View)

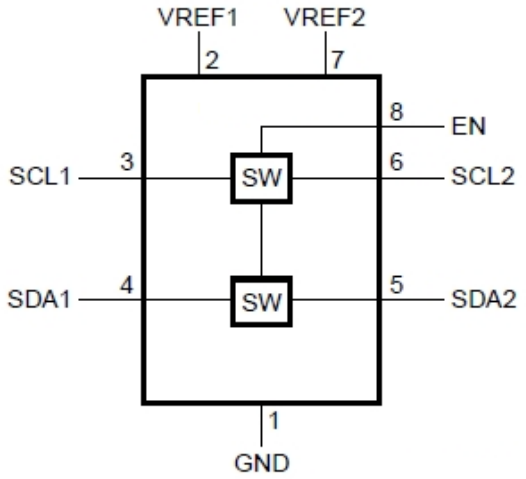


UQFN1.6x1.6-8L(Top View)

Pin Description

Pin No	Name	Description
1	GND	ground (0 V)
2	VREF1	low-voltage side reference supply voltage for SCL1 and SDA1
3	SCL1	serial clock, low-voltage side; connect to VREF1 through a pull-up resistor
4	SDA1	serial data, low-voltage side; connect to VREF1 through a pull-up resistor
5	SDA2	serial data, high-voltage side; connect to VREF2 through a pull-up resistor
6	SCL2	serial clock, high-voltage side; connect to VREF2 through a pull-up resistor
7	VREF2	high-voltage side reference supply voltage for SCL2 and SDA2
8	EN	switch enable input; connect to VREF2 and pull-up through a high resistor

Block Diagram



EN	Function
H	SCL1 = SCL2; SDA1 = SDA2
L	disabled

Figure.1Block Diagram

Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Reference Voltage(2) ..... -0.5V to +6.0V
Reference bias voltage ..... -0.5V to+6.0V
DC Input Voltage ..... -0.5V to +6.0V
Control Input Votage(EN) ..... -0.5V to+6.0V
channel current (DC) 128mA
Input clamping Current ..... -50mA
ESD: HBM Mode 4000V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

V_{CC} = 2.7 V to 5.5 V; GND = 0 V; T_A = -40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{I/O}$	Voltage on an input/output pin	SCL1, SDA1, SCL2, SDA2	0	-	5	V
V_{REF1}	Reference voltage (1)	VREF1	0	-	5	V
V_{REF2}	Reference bias voltage (2)	VREF2	0	-	5	V
$V_{I(EN)}$	Input voltage on pin EN	-	0	-	5	V
$I_{(pass)}$	Pass switch current	-	-	-	64	mA
T_A	Ambient temperature	-	-40	-	85	°C

DC Electrical Characteristics

T_A = -40 °C to +85 °C; unless otherwise specified

Parameter	Description	Test Conditions[1]		Min	Typ.[2]	Max	Unit
Input and output SDAB and SCLB							
V_{IK}	input clamping voltage	I_I = -18mA; $V_{I(EN)}$ = 0 V		-	-	-1.2	V
I_{IH}	HIGH-level input current	V_I = 5 V; $V_{I(EN)}$ = 0 V		-	-	5	µA
$C_{i(EN)}$	input capacitance on pin EN	V_I = 3 V or 0 V		-	11	-	pF
$C_{io(off)}$	off-state input/output capacitance (SCLn, SDAn)	V_O = 3 V or 0 V; $V_{I(EN)}$ = 0 V		-	4	-	pF
$C_{io(on)}$	on-state input/output capacitance (SCLn, SDAn)	V_O = 3 V or 0 V; $V_{I(EN)}$ = 3 V		-	10.5	-	pF
Ron	ON-state resistance[2] (SCLn, SDAn)	V_I = 0V; I_O = 64mA	$V_{I(EN)}$ = 4.5 V	-	3.5	5.5	Ω
			$V_{I(EN)}$ = 3 V	-	4.7	7.0	Ω
			$V_{I(EN)}$ = 2.3 V	-	6.3	9.5	Ω
			$V_{I(EN)}$ = 1.5 V	-	60	140	Ω
		V_I = 2.4V; I_O = 15mA	$V_{I(EN)}$ = 4.5 V	1	6	15	Ω
			$V_{I(EN)}$ = 3 V	20	60	140	Ω
		V_I = 1.7V; I_O = 15mA	$V_{I(EN)}$ = 2.3 V	20	60	140	Ω

Notes:

1) All typical values are at T_A = 25 °C.
2) Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

Dynamic Characteristics

T_A = -40 °C to +85 °C; unless otherwise specified. Values guaranteed by design.

Symbol	Parameter	Conditions	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		Unit
			Min	Max	Min	Max	Min	Max	
Dynamic characteristics (translating down)									
$V_{I(EN)}$ = 3.3 V; V_{IH} = 3.3 V; V_{IL} = 0 V; V_M = 1.15 V									
t_{PLH}	LOW-to-HIGH propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	0.8	0	0.6	0	0.3	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1.2	0	1	0	0.5	ns
$V_{I(EN)}$ = 2.5 V; V_{IH} = 2.5 V; V_{IL} = 0 V; V_M = 0.75 V									
t_{PLH}	LOW-to-HIGH propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1	0	0.7	0	0.4	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1.3	0	1	0	0.6	ns
Dynamic characteristics (translating up)									
$V_{I(EN)}$ = 3.3 V; V_{IH} = 2.3 V; V_{IL} = 0 V; V_T = 3.3 V; V_M = 1.15 V; R_L = 300 Ω									
t_{PLH}	LOW-to-HIGH propagation delay	ffrom (input) SCL1 orSDA1 to (output) SCL2 or SDA2	0	0.9	0	0.6	0	0.4	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1.4	0	1.1	0	0.7	ns
$V_{I(EN)}$ = 2.5 V; V_{IH} = 1.5 V; V_{IL} = 0 V; V_T = 2.5 V; V_M = 0.75 V; R_L = 300 Ω									
t_{PLH}	LOW-to-HIGH propagation delay	from (input) SCL1 orSDA1 to (output) SCL2 or SDA2	0	1	0	0.6	0	0.4	ns
t_{PHL}	HIGH-to-LOW propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1.3	0	1.3	0	0.8	ns

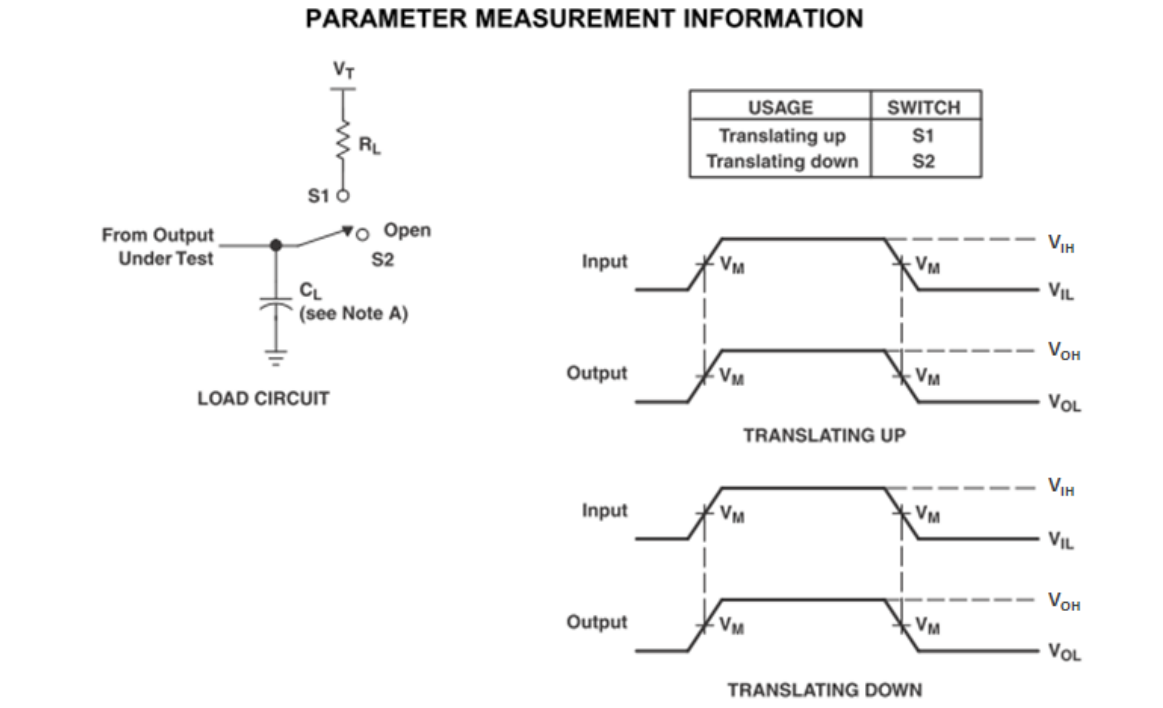


Figure.2 Load Circuit for Outputs

Functional Description

The PI6ULS5V9306 is a dual bidirectional I²C-bus and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.2 V to 3.3 V (VREF1) and 1.8 V to 5.5 V(VREF2).

The PI6ULS5V9306 allows bidirectional voltage translations between 1.2 V and 5 V without the use of a direction pin. The low ON-state resistance (Ron) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports.

The PI6ULS5V9306 is not a bus buffer that provides both level translation and physically isolates to either side of the bus when both sides are connected. The PI6ULS5V9306 only isolates both sides when the device is disabled and provides voltage level translation when active.

The PI6ULS5V9306 can also be used to run two buses, one at 400kHz operating frequency and the other at 100 kHz operating frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated when the 400 kHz operation of the other bus is required. If the master is running at 400kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the translator.

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the translator's bus. The PI6ULS5V9306 has a standard open-collector configuration of the I²C-bus. The size of these pull-up resistors depends on the system, but each side of the translator must have a pull-up resistor. The device is designed to work with Standard-mode, Fast-mode and Fast mode Plus I²C-bus devices in addition to SMBus devices.

When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low resistance connection exists between the SDA1 and SDA2 ports. When the higher voltage is on the SDA2 port, and the SDA2 port is HIGH, the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull-up supply voltage (VDPU) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or

propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

Application Information

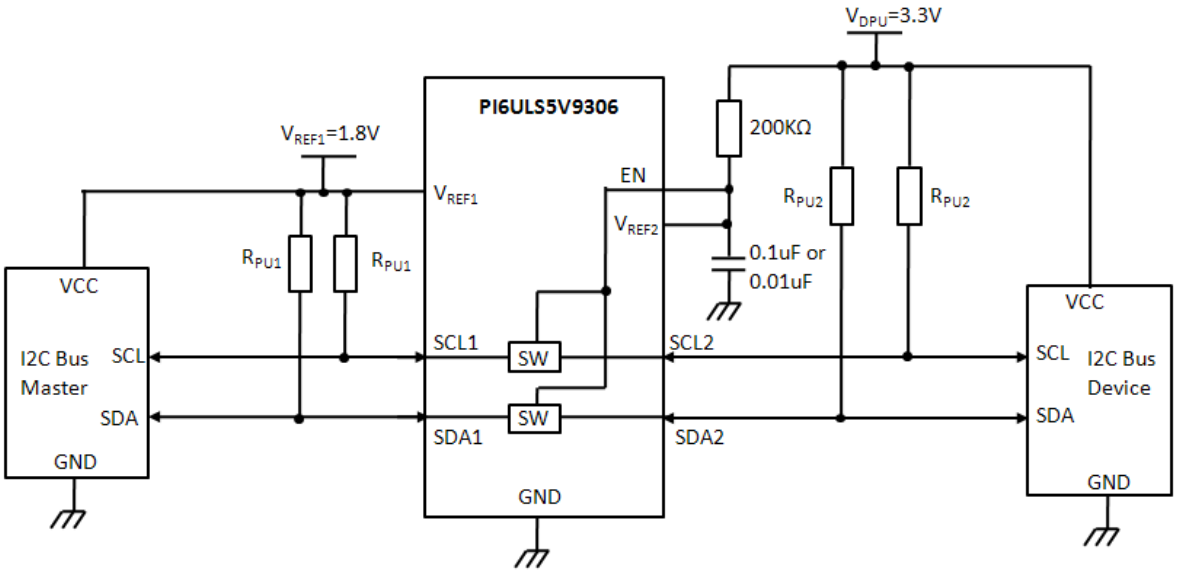


Figure.3 Typical Open Drain Application Circuit (Switch Always Enabled)

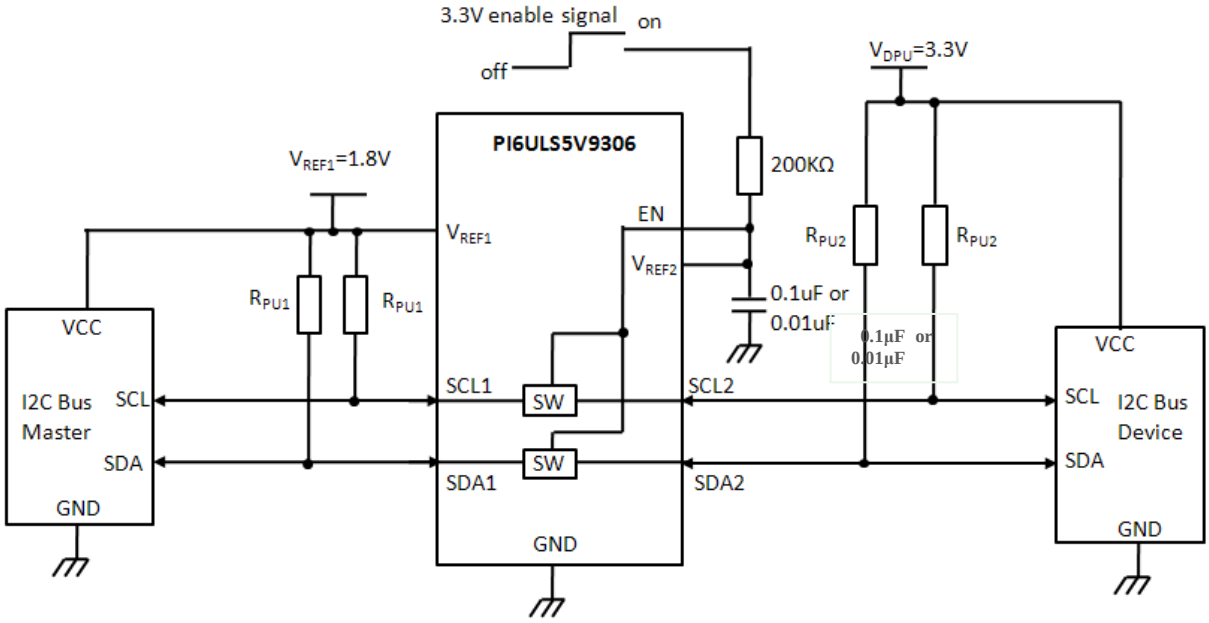


Figure.4 Typical Open Drain Application Circuit (Switch Enabled Control)

Open Drain Application

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREF2 and both pins pulled to high-side VDPU through a pull-up resistor (typically 200 kΩ). This allows VREF2 to regulate the EN input. A filter capacitor on VREF2 is recommended.

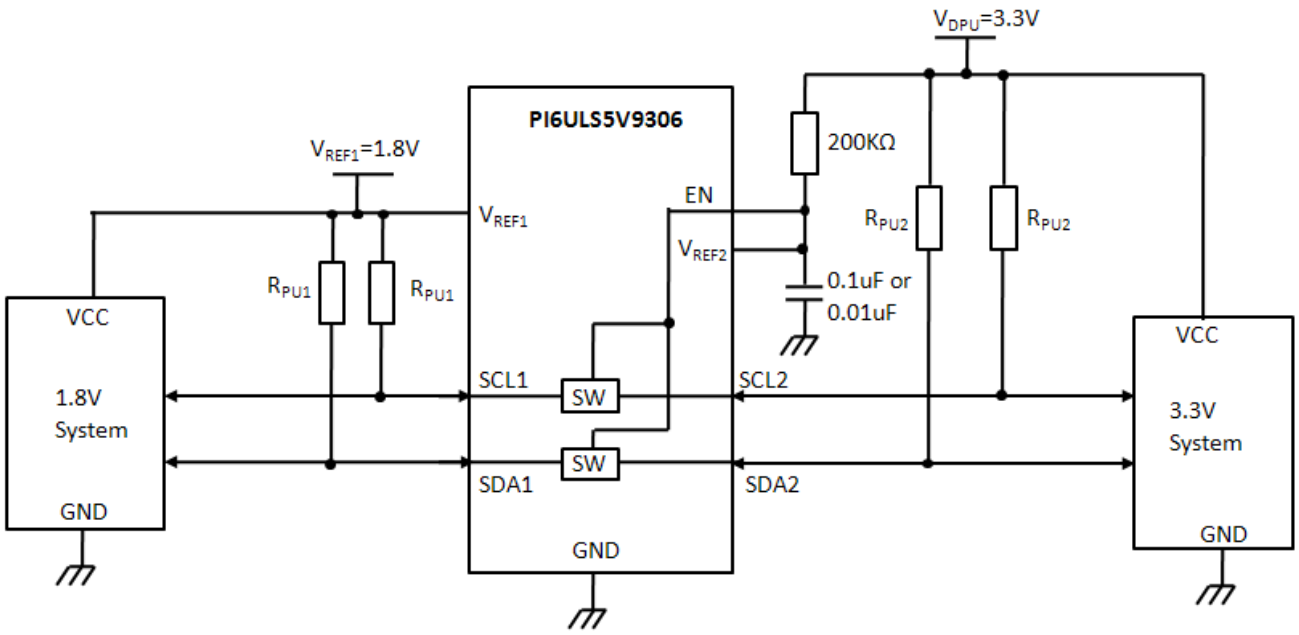


Figure.5 Typical push-pull Application Circuit (Switch Enabled Control)

Push Pull Application

If used in push-pull system, the pull-up resistors on REF side are also needed. The data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction.

Operating Voltage

Refer to Figure 2

		MIN	TYP(1)	MAX	UNIT
V_{DPU}	Ref2 side pull-up voltage on 200kΩ	V_{REF1} + 0.6	2.1	5	V
EN	Enable input voltage	V_{REF1} + 0.6	2.1	5	V
V_{REF1}	Reference voltage	0	1.5	4.4	V
I_{PASS}	Pass switch current		14		mA
I_{REF}	Reference-transistor current		5		µA
TA	Operating free-air temperature	–40		85	℃

The pass through current: I_pass

I_pass is determined by the pull-up and the low voltage added on the PI6LS5V9306

In figure 6, I_pass= $(V_{REF1}-V_{OL1\_9306})/R_{PU1}$

When V_IN is 0V, the PI6ULS5V9306 can support as large as 64mA pass through current in theory. But we recommend it's better to limit the I_pass in 15mA

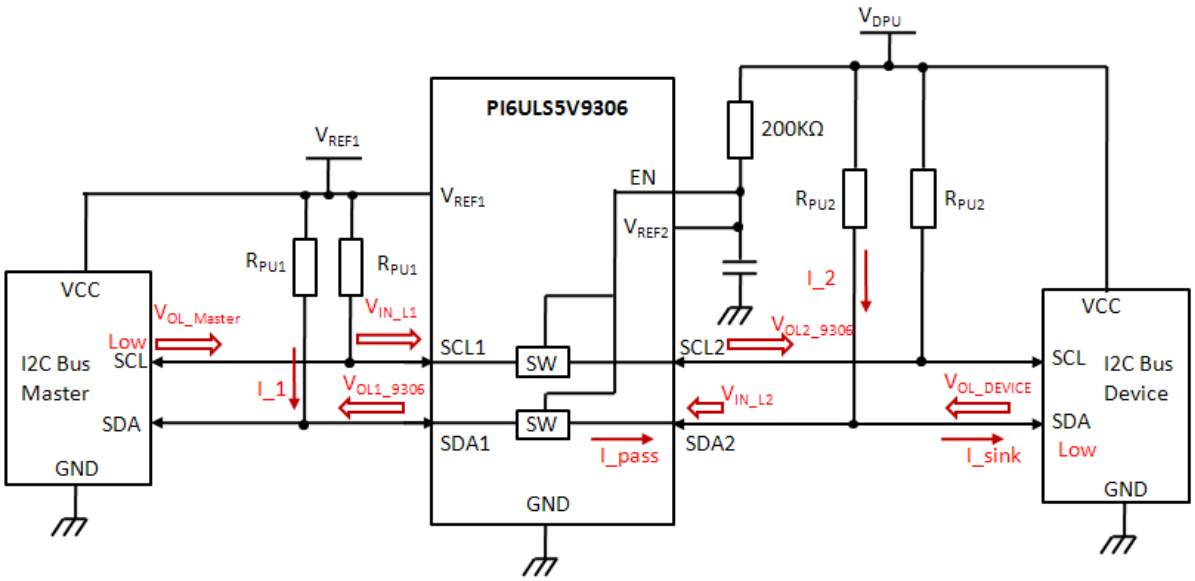


Figure 6. Typical Open Drain Application Circuit

(1) The sink current : I_sink

The device would sink the total current from both pull-up resistors.
For example, in figure bellow, when the SDA2 is pulled low by the I2C device, the sink current of the I2C device I_sink=Ipass+I_2=I_1+I_2. The same thing will happen when I2C master pull low the I2C bus.
The I_sink should be limited to not larger than the tolerance of the I2C devices.

(2) V_{IL},V_{OL} of the external drive and V_{OL} of PI6ULS5V9306

In normal application, the V_{IL} of external devices should always be larger than the V_{OL} of PI6ULS5V9306.
The value of PI6ULS5V9306's V_{OL} is determined by the pass through current and the low voltage added on the SDA, SCL pins.
The $V_{OL\_9306} = V_{IN\_L} + V_{UP}$ (V_{UP} is mainly determined by the I_pass, it always less than 0.35V.)

(3) Low VREF application

The PI6ULS5V9306 can support very low Vref1 application in theory, but we recommend not lower than 0.9V.Because when VREF1 is less than 1.8V, the V_{OL} of REF1 side is a concern in system.
For example, in figure 6, if VREF1=0.9V, VDPU=3.3V he V_{IL} of the REF1 side I2C master is normally 0.3*VREF1 =0.25V, but the V_{OL} of REF2 side can up to 0.1*VDPU=0.36V sometimes.
The system designer must make sure this situation doesn't happen. A limit for the V_{OL} of REF2 side devices is required then.

The bellow table shows the requirement for V_{OL} of VREF2 side devices when using PI6ULS5V9306
(Requirement for V_{OL_DEVICE} in figure 6)

The V_{OL} requirement of V_{REF2} side external devices (Temp=25℃, Assume the V_{IL} of V_{REF1} side devices is 0.3*V_{REF1})			
I_pass / V_{REF1}	≤3mA	10mA	15mA
0.9V	≤0.15V	≤0.1V	Not Recommended
1.2V	≤0.2V	≤0.15V	Not Recommended

1.5V	≤0.3V	≤0.25V	≤0.2V
1.8V	≤0.4V	≤0.35V	≤0.3V

Pull-up resistors and minimum values

Sizing the pull-up resistor on an open-drain bus is specific to the individual application and is dependent on the following driver characteristics:

- The driver sink current
- The V_{OL} of driver
- The V_{OL} of the PI6ULS5V9306
- The V_{IL} of the driver
- Frequency of operation

The following tables can be used to estimate the pull-up resistor value in different use cases so that the minimum resistance for the pull-up resistor can be found.

Tables in bellow contain suggested minimum values of pull-up resistors for the PI6ULS5V9306 with typical voltage translation levels and drive currents.

The calculated values assume that both drive currents are the same.

V_{OL} = V_{IL} = 0.1*VCC and accounts for a 5 % VCC tolerance of the supplies, 1 % resistor values. It should be noted that the resistor chosen in the final application should be equal to or larger than the values shown in the table to ensure that the pass voltage is less than 10 % of the VCC voltage, and the external driver should be able to sink the total current from both pull-up resistors.

Pull-up resistor minimum values, 3 mA driver sink current for PI6ULS5V9306

A Side	B side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.9V	R_{RPU1} = 859Ω R_{RPU2} = 859Ω	R_{RPU1} = 970Ω R_{RPU2} = 970Ω	R_{RPU1} = none R_{RPU2} = 896Ω Or both 1.23kΩ	R_{RPU1} = none R_{RPU2} = 1.19kΩ Or both 1.53kΩ	R_{RPU1} = none R_{RPU2} = 1.82kΩ Or both 2.16kΩ
1.2V		R_{RPU1} = 1.07kΩ R_{RPU2} = 1.07kΩ	R_{RPU1} = none R_{RPU2} = 886Ω Or both 1.33kΩ	R_{RPU1} = none R_{RPU2} = 1.18kΩ Or both 1.63kΩ	R_{RPU1} = none R_{RPU2} = 1.81kΩ Or both 2.26kΩ
1.5V			R_{RPU1} = none R_{RPU2} = 875Ω Or both 1.43kΩ	R_{RPU1} = none R_{RPU2} = 1.17kΩ Or both 1.73kΩ	R_{RPU1} = none R_{RPU2} = 1.8kΩ Or both 2.36kΩ
1.8V			R_{RPU1} = 1.53kΩ R_{RPU2} = 1.53kΩ	R_{RPU1} = none R_{RPU2} = 1.16kΩ Or both 1.82kΩ	R_{RPU1} = none R_{RPU2} = 1.79kΩ Or both 2.46kΩ
2.5V				R_{RPU1} = 2.06kΩ R_{RPU2} = 2.06kΩ	R_{RPU1} = none R_{RPU2} = 1.77kΩ Or both 2.69kΩ
3.3V					R_{RPU1} = none R_{RPU2} = 1.74kΩ Or both 2.96kΩ

Pull-up resistor minimum values, 10 mA driver sink current for PI6ULS5V9306

A Side	B side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.9V	R_{RPU1} = 258Ω R_{RPU2} = 258Ω	R_{RPU1} = 291Ω R_{RPU2} = 291Ω	R_{RPU1} = none R_{RPU2} = 269Ω Or both 369Ω	R_{RPU1} = none R_{RPU2} = 358Ω Or both 458Ω	R_{RPU1} = none R_{RPU2} = 546Ω Or both 646Ω
1.2V		R_{RPU1} = 321Ω R_{RPU2} = 321Ω	R_{RPU1} = none R_{RPU2} = 266Ω Or both 399Ω	R_{RPU1} = none R_{RPU2} = 355Ω Or both 488Ω	R_{RPU1} = none R_{RPU2} = 543Ω Or both 677Ω
1.5V			R_{RPU1} = none R_{RPU2} = 263Ω Or both 429Ω	R_{RPU1} = none R_{RPU2} = 352Ω Or both 518Ω	R_{RPU1} = none R_{RPU2} = 540Ω Or both 707Ω
1.8V			R_{RPU1} = 460Ω R_{RPU2} = 460Ω	R_{RPU1} = none R_{RPU2} = 348Ω Or both 548Ω	R_{RPU1} = none R_{RPU2} = 537Ω Or both 737Ω
2.5V				R_{RPU1} = 619Ω R_{RPU2} = 619Ω	R_{RPU1} = none R_{RPU2} = 521Ω Or both 808Ω
3.3V					R_{RPU1} = none R_{RPU2} = 522Ω Or both 889Ω

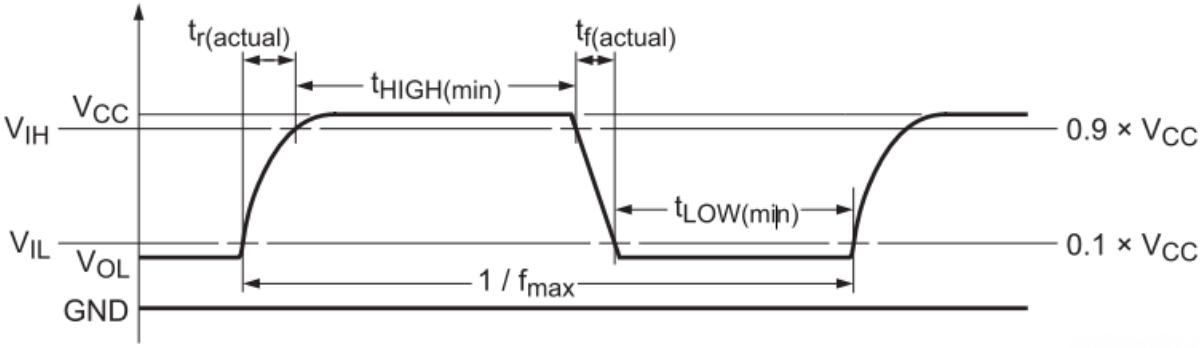
Pull-up resistor minimum values, 15 mA driver sink current for PI6ULS5V9306

A Side	B side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.9V	R_{RPU1} = 172Ω R_{RPU2} = 172Ω	R_{RPU1} = 194Ω R_{RPU2} = 194Ω	R_{RPU1} = none R_{RPU2} = 179Ω Or both 246Ω	R_{RPU1} = none R_{RPU2} = 238Ω Or both 305Ω	R_{RPU1} = none R_{RPU2} = 364Ω Or both 431Ω
1.2V		R_{RPU1} = 214Ω R_{RPU2} = 214Ω	R_{RPU1} = none R_{RPU2} = 177Ω Or both 266Ω	R_{RPU1} = none R_{RPU2} = 236Ω Or both 325Ω	R_{RPU1} = none R_{RPU2} = 362Ω Or both 451Ω
1.5V			R_{RPU1} = none R_{RPU2} = 175Ω Or both 286Ω	R_{RPU1} = none R_{RPU2} = 234Ω Or both 345Ω	R_{RPU1} = none R_{RPU2} = 360Ω Or both 471Ω
1.8V			R_{RPU1} = 306Ω R_{RPU2} = 306Ω	R_{RPU1} = none R_{RPU2} = 232Ω Or both 366Ω	R_{RPU1} = none R_{RPU2} =358Ω Or both 492Ω
2.5V				R_{RPU1} = 413Ω R_{RPU2} = 413Ω	R_{RPU1} = none R_{RPU2} = 354Ω Or both 539Ω
3.3V					R_{RPU1} = none R_{RPU2} = 348Ω Or both 593Ω

Max Frequency Application

The maximum frequency is limited by the minimum pulse width LOW and HIGH as well as rise time and fall time.

$$f(\max) = \frac{1}{\text{tLOW(min)} + \text{tHIGH(min)} + \text{tr(actual)} + \text{tf(actual)}}$$



The rise and fall times are dependent upon translation voltages, the drive strength, the total node capacitance (CL) and the pull-up resistors (RPU) that are present on the bus. The node capacitance is the addition of the PCB trace capacitance and the device capacitance that exists on the bus.

Because of the dependency of the external components, PCB layout and the different device operating states the calculation of rise and fall times is complex and has several inflection points along the curve.

The main component of the rise and fall times is the RC time constant of the bus line when the device is in its two primary operating states: when device is in the ON state and it is low-impedance, the other is when the device is OFF isolating the A-side from the B-side.

There are some basic guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the PI6ULS5V9306 close to the processor.
- The signal round trip time on trace should be shorter than the rise or fall time of signal to reduce reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher drive strength controlled by the pull-up resistor (up to 15 mA), the higher the frequency the device can use.

The system designer must design the pull-up resistor value based on external current drive strength and limit the node capacitance (minimize the wire, stub, connector and trace length) to get the desired operation frequency result.

Part Marking

W Package Cu

Z: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above fab code means Cu wire

Note: Bar above "I" means Fab3 og MGN

W Package Au

Z: Die Rev
AB: Date Code (Year & Workweek)
K: Assembly Site Code
G: Wafer Fab Site Code

U Package

Z: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above fab code means Cu wire

ZE Package

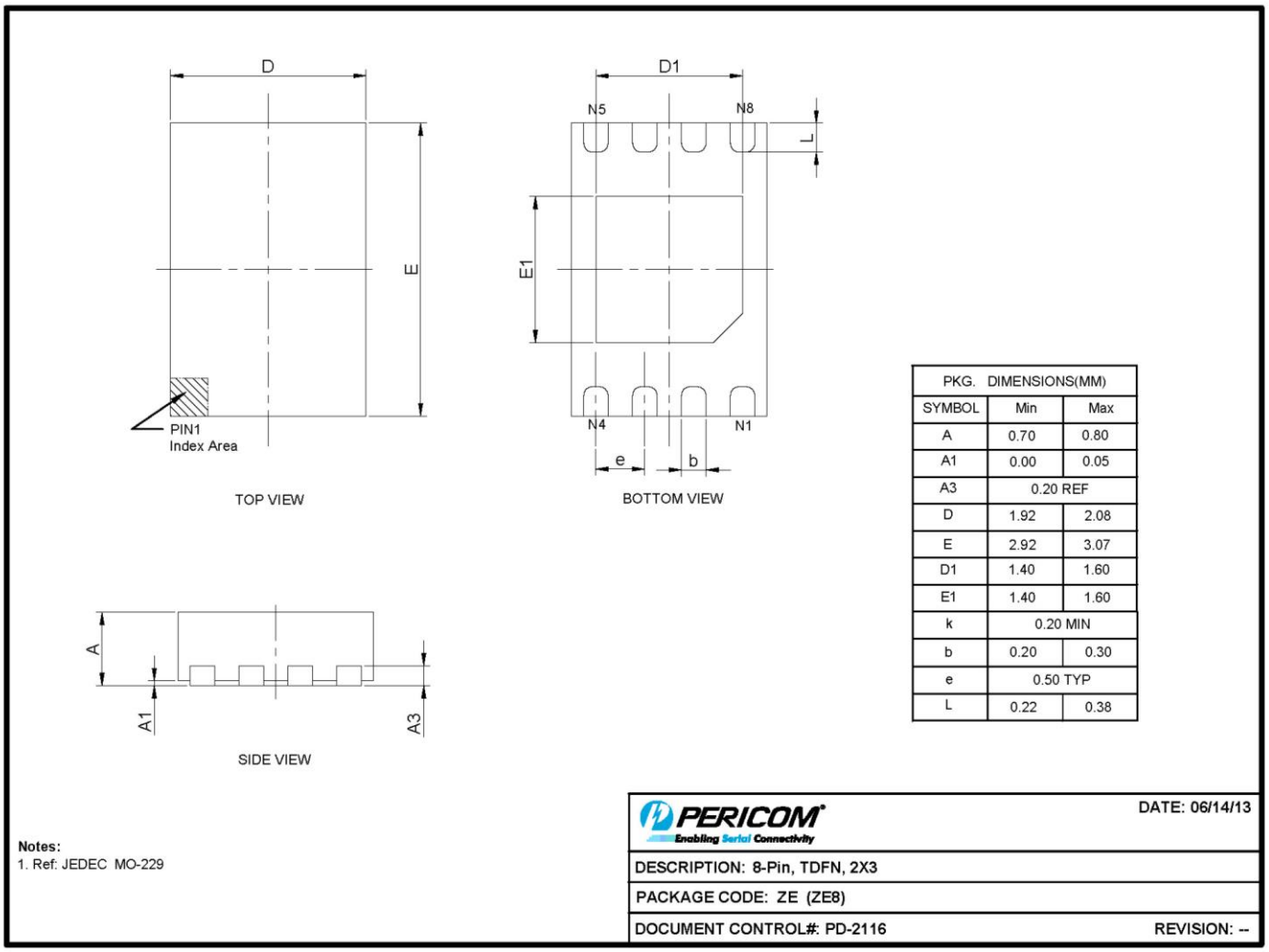
J: Assembly Site Code
G: Fab Site Code
XX: Date Code (Year & Workweek)
Bar above "A" means Fab3 of MGN

XT Package

Y: Year
W: Workweek

Packaging Mechanical

TDFN-8 (ZE)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
D	1.92	2.08
E	2.92	3.07
D1	1.40	1.60
E1	1.40	1.60
k	0.20 MIN	
b	0.20	0.30
e	0.50 TYP	
L	0.22	0.38

Notes:
1. Ref: JEDEC MO-229

PERICOM Enabling Serial Connectivity — DATE: 06/14/13

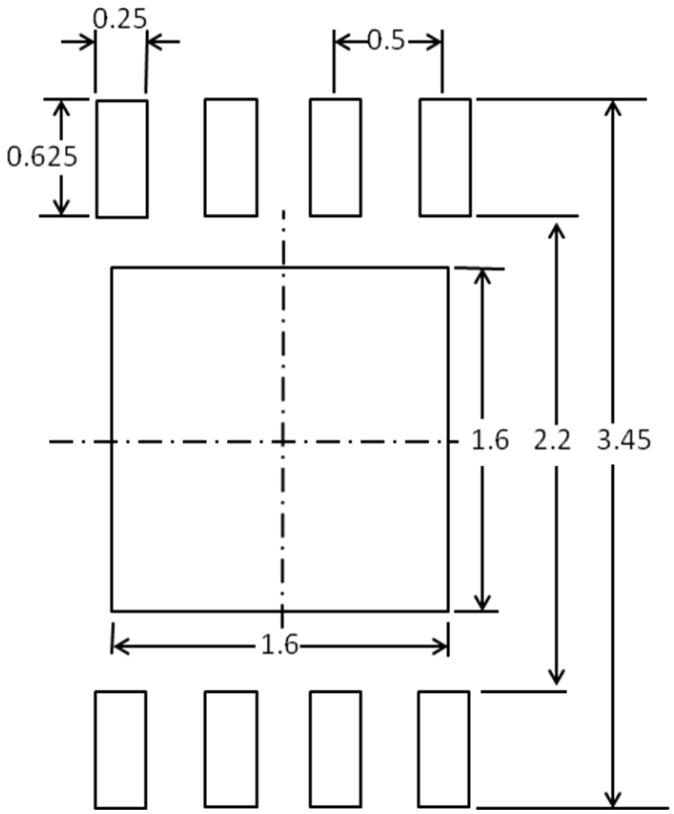
DESCRIPTION: 8-Pin, TDFN, 2X3

PACKAGE CODE: ZE (ZE8)

DOCUMENT CONTROL#: PD-2116 — REVISION: --

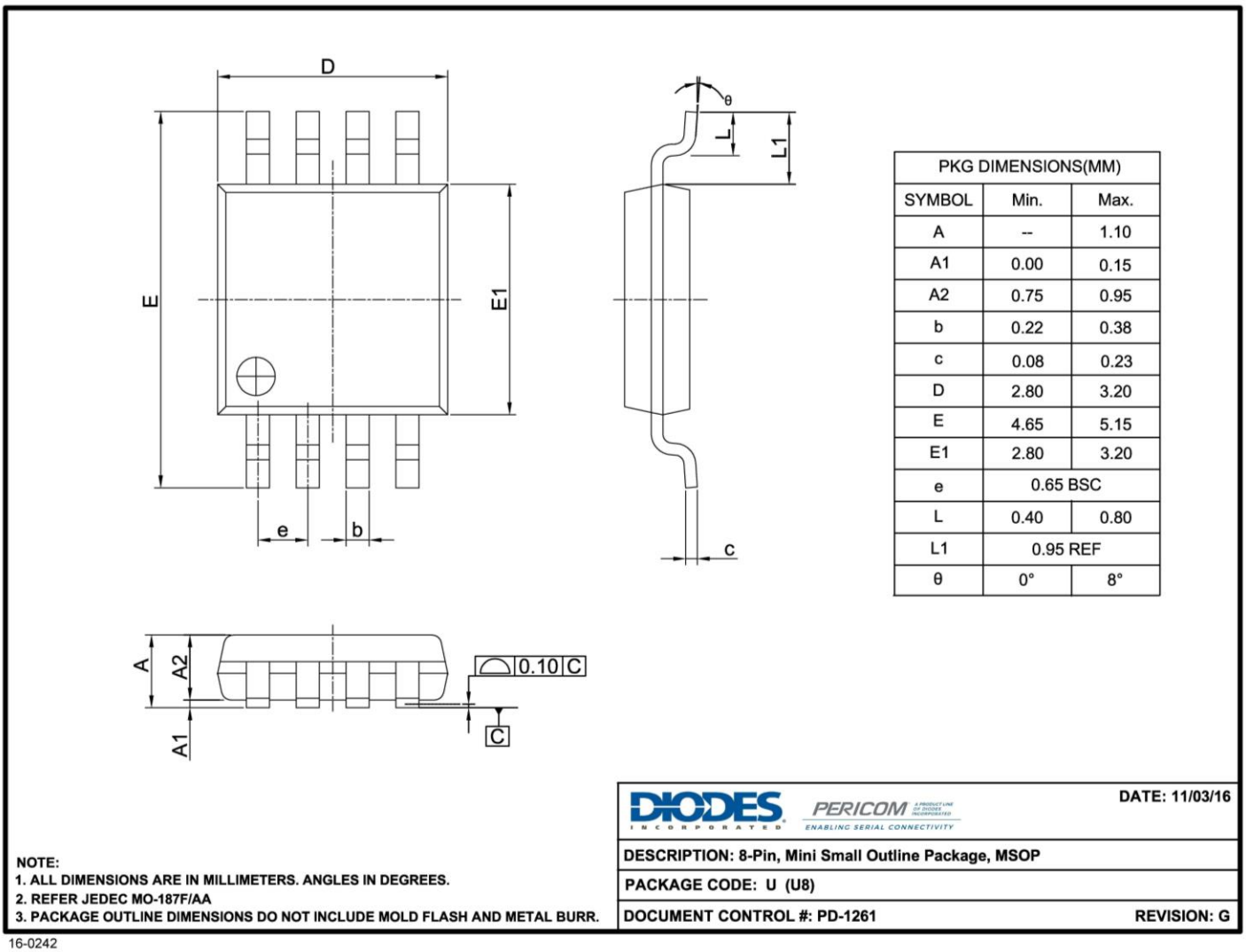
13-0155

Recommended Land pattern for TDFN2x3-8L



Note:
All linear dimensions are in millimeters

MSOP-8(U)



PKG DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	--	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.80	3.20
E	4.65	5.15
E1	2.80	3.20
e	0.65 BSC	
L	0.40	0.80
L1	0.95 REF	
θ	0°	8°

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. REFER JEDEC MO-187F/AA
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.

DATE: 11/03/16

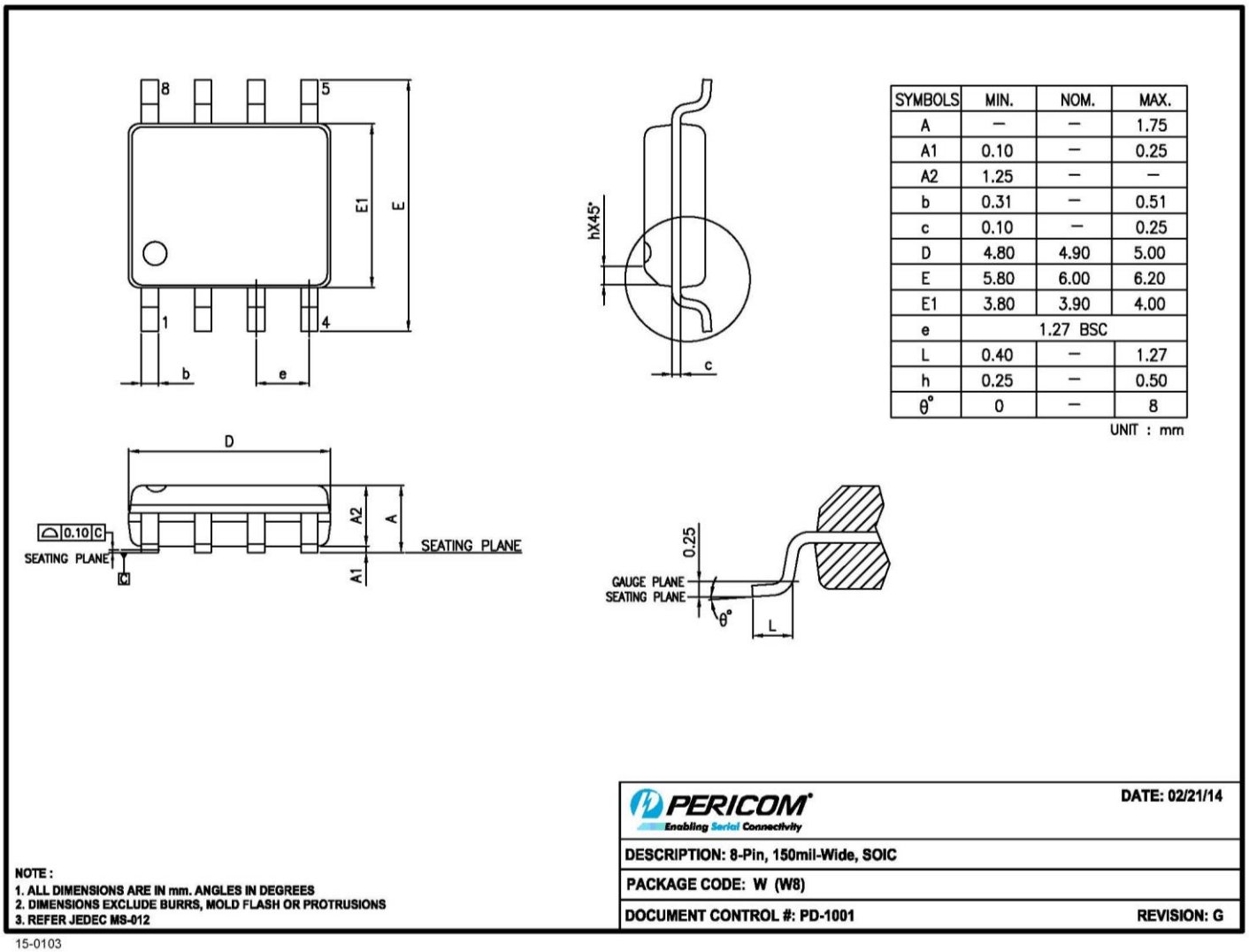
DESCRIPTION: 8-Pin, Mini Small Outline Package, MSOP

PACKAGE CODE: U (U8)

DOCUMENT CONTROL #: PD-1261 REVISION: G

16-0242

SOIC-8(W)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

UNIT : mm

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. DIMENSIONS EXCLUDE BURRS, MOLD FLASH OR PROTRUSIONS
3. REFER JEDEC MS-012

PERICOM Enabling Serial Connectivity

DATE: 02/21/14

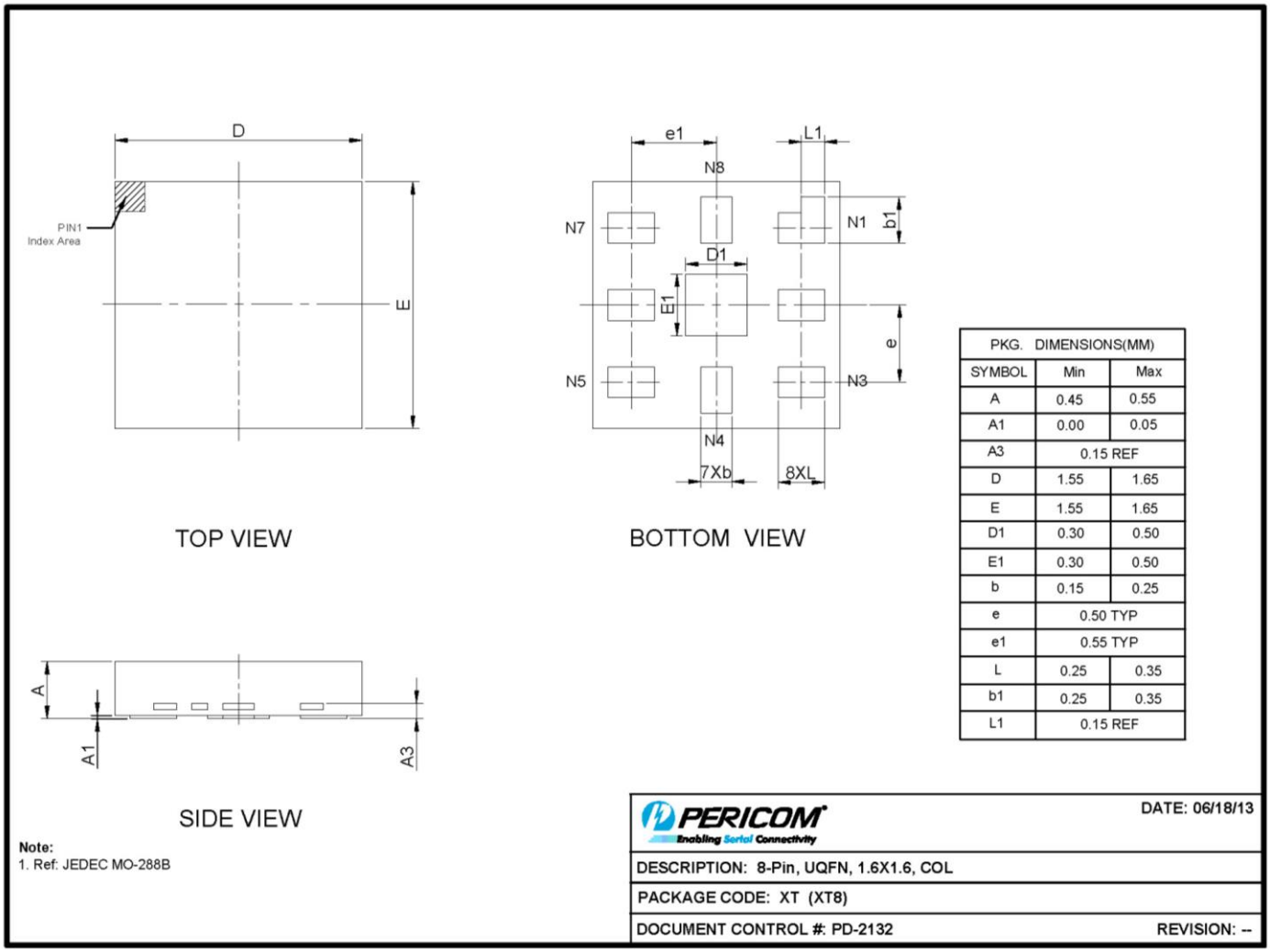
DESCRIPTION: 8-Pin, 150mil-Wide, SOIC

PACKAGE CODE: W (W8)

DOCUMENT CONTROL #: PD-1001 REVISION: G

15-0103

UQFN-8 (XT)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.45	0.55
A1	0.00	0.05
A3	0.15 REF	
D	1.55	1.65
E	1.55	1.65
D1	0.30	0.50
E1	0.30	0.50
b	0.15	0.25
e	0.50 TYP	
e1	0.55 TYP	
L	0.25	0.35
b1	0.25	0.35
L1	0.15 REF	

For latest package info.
please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part Number	Package Code	Package Description
PI6ULS5V9306ZEEX	ZE	8-Pin, 2X3 (TDFN)
PI6ULS5V9306UEX	U	8-Pin, Mini Small Outline Package (MSOP)
PI6ULS5V9306WEX	W	8-Pin,150 mil Wide (SOIC)
PI6ULS5V9306XTEX	XT	8-pin, 1.6x1.6, COL (UQFN)

Notes:

- EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
- See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or

2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Interface - Signal Buffers, Repeaters ***category:***

Click to view products by Diodes Incorporated ***manufacturer:***

Other Similar products are found below :

PI6ULS5V9509UEX PI3HDMI101-BZHEX PI3EQX12904AZHEX PI6ULS5V9306WEX PI3EQX1004EZTFEX PI6ULS5V9509WEX 48705-3001R2 48705-6501R2 DS280BR820ZBLT PCA9617ADPJ PI6ULS5V9515AWEX PI3HDMI101ZHE LTC4315CDE#PBF LTC4300-1CMS8#PBF DS110DF1610FB/NOPB LTC4301LCDD#PBF LTC4303IDD#PBF LTC4315IMS#TRPBF LTC4304IMS#PBF DS280DF810ABVT LTC4315IDE#PBF LTC4300-1IMS8#PBF LTC4313IMS8-3#TRPBF LTC4300-2IMS8#PBF LTC4300A-1CMS8#PBF PCA9515AD,118 LTC4307CMS8-1#TRPBF LTC4304CDD#PBF PI3EQX1002B1ZLEX LTC4301LIMS8 LTC4313IDD-3#TRPBF LTC4309IGN#PBF LTC4309CGN#PBF MAX9169EUE+ LTC4302IMS-2#PBF LTC4302CMS-1#PBF PI6ULS5V9306UEX LTC4300A-1CMS8#TRPBF P82B715TD,112 PCA9507DP,118 PCA9509DP,118 PCA9509GM,125 PCA9515ADP,118 PCA9517AD,118 PCA9517ADP,118 PCA9517DP,118 P82B715TD,118 PI6ULS5V9511AWEX PI1EQX512AXUAEX PI2EQX502TZHEX