Real-time Clock Module (3-wire Interface)

Features

- Uses external 32.768kHz quartz crystal
- Real-time clock (RTC) counts seconds, minutes hours, date of the month, month, day of the week, and year with leap-year compensation valid up to 2099
- 31-byte, RAM for data storage
- Time keeping voltage: 1.5V to 5.5V
- Uses less than 300nA at 2.0V
- Simple 3-wire interface
- Serial I/O for minimum pin count
- Burst mode for reading/writing successive addresses in clock/RAM
- TTL-compatible (VCC = 5V)
- Optional industrial temperature range: -40°C to +85°C
- Battery backup
- Trickle charger on chip for rechargeable energy source backup
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 8-Pin, SOIC (W)
  - 8-Pin, TDFN (ZE)

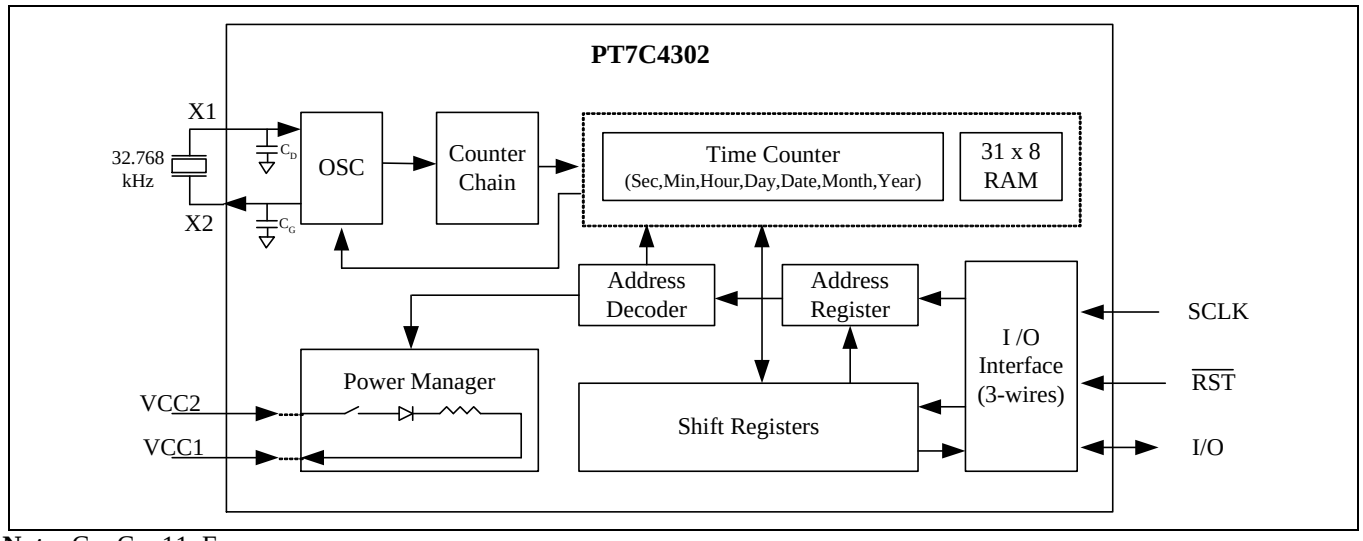
Description

The PT7C4302 serial real-time clock is a low-power clock/calendar with a programmable square-wave output and 31 bytes of RAM.

Address and data are transferred serially via a 3-wire bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock supports either the 24-hour or 12-hour format with AM/PM indicator.

Table 1 shows the basic functions of PT7C4302. More details are shown in section: overview of functions.

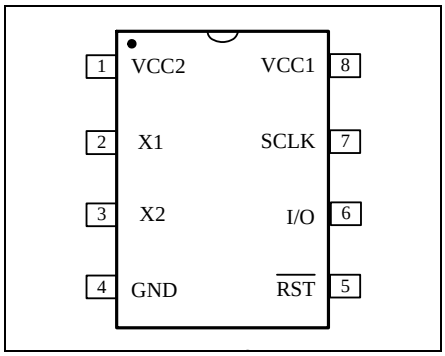
Function Block



Note: C_D=C_G=11pF

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin#	Pin	Type	Description
1	VCC 2	P	**Primary power.** When V_{CC2} is greater than V_{CC1} + 0.2V, V_{CC2} will power the IC. While V_{CC2}<V_{CC1}, V_{CC1} will power the IC.[*1]
2	X1	I	**Oscillator Circuit Input.** Together with X2, 32.768kHz crystal is connected between them.
3	X2	O	**Oscillator Circuit Output.** Together with X1, 32.768kHz crystal is connected between them.
4	GND	P	**Ground.**
5	$\overline{RST}$	I	**Reset.** The reset signal must be asserted high during a read or a write. This pin has a 40kΩ internal pull-down resistor.
6	I/O	I/O	**Serial Data Input/Output.** I/O is the input/output pin for the 3-wire serial interface. The pin has a 40kΩ internal pull-down resistor.
7	SCL K	I	**Serial Clock Input.** SCLK is used to synchronize data movement on the 3-wire serial interface. The pin has a 40kΩ internal pull-down resistor.
8	VCC 1	P	**Backup power.** When V_{CC2} is greater than V_{CC1} + 0.2V, V_{CC2} will power the IC. While V_{CC2}<V_{CC1}, V_{CC1} will power the IC. [*1]

Note[*1]: If V_{CC1} connects to battery, the battery voltage V_{CC1} has to be lower than V_{CC2} - 0.2Vwhen IC is read and written.

Maximum Ratings

Storage Temperature.....-65℃ to +150℃
Supply Voltage to Ground Potential (Vcc to GND) .....-0.3V to +6.5V
DC Input (All Other Inputs except Vcc & GND).....-0.3V to +6.5V
DC Output Voltage (SDA, /INTA, /INTB pins).....-0.3V to +6.5V
Power Dissipation ..... 320mW (Depend on package)
Junction Temperature.....125℃ max.

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Description	Min	Type	Max	Unit
V_{CC1}	Backup power voltage	1.5	-	5.5	V
V_{CC2}	Timing data and RAM data maintaining voltage	1.2	-	5.5	
	Timing data writing voltage	1.5	-	5.5	
	Timing data reading voltage	1.5	-	5.5	
	RAM data writing voltage	3.0	-	5.5	
	RAM data reading voltage	1.5	-	5.5	
V_{IH}	Input high level	2	-	V_{CC}+0.3	
V_{IL}	Input low level	-0.3	-	0.3	
T_A	Operating temperature	-40	-	85	℃

DC Electrical Characteristics

Unless otherwise specified, GND =0V, T_A = 25 ℃, Oscillation frequency = 32.768 kHz.

Symbol	Item	Pin	Conditions		Min	Typ	Max	Unit
V_{CC1}	Backup power voltage	VCC1	-		1.5	-	5.5	V
V_{CC2}	Timing and RAM data maintaining	VCC2	-		1.2	-	5.5	V
	Timing data writing voltage		-		1.5	-	5.5	
	Timing data reading voltage		-		1.5	-	5.5	
	RAM data writing voltage		-		3.0	-	5.5	
	RAM data reading voltage		-		1.5	-	5.5	
I_{CC1}	Current consumption	VCC1	OSC on, Note 2, 5	V_{CC1}: 2V	-	-	0.4	mA
				V_{CC1}: 5V	-	-	1.2	
			OSC on, Note 1, 5	V_{CC1}: 2V	-	0.5	-	µA
				V_{CC1}: 5V	-	1	-	
			OSC off, Note 4, 5, 7	V_{CC1}: 2V	-	100	-	nA
				V_{CC1}: 5V	-	100	-	
I_{CC2}	Current consumption	VCC2	OSC on, Note 2, 6	V_{CC1}: 2V	-	-	0.425	mA
				V_{CC1}: 5V	-	-	1.28	
			OSC on, Note 1, 6	V_{CC1}: 2V	-	-	25.3	µA
				V_{CC1}: 5V	-	-	81	
			OSC off, Note 4, 6	V_{CC1}: 2V	-	-	25	µA
				V_{CC1}: 5V	-	-	80	
V_{IL1}	Low-level input voltage	SCL, /RST	V_{CC1}: 5V		-	1.1	0.8	V
			V_{CC1}: 2V		-	0.6	0.4	
V_{IH1}	High-level input voltage	SCL, /RST	V_{CC1}: 5V		2.0	1.3	-	V
			V_{CC1}: 2V		1.4	0.9	-	

Symbol	Item	Pin	Conditions	Min	Typ	Max	Unit
V_{IL2}	Low-level input voltage	X1	V_{CC1}: 5V	-	1.9	0.8	V
			V_{CC1}: 2V	-	0.9	0.6	
V_{IH2}	High-level input voltage	X1	V_{CC1}: 5V	2.0	1.9	-	V
			V_{CC1}: 2V	1.4	0.9	-	
V_{OL}	Low-level output voltage	I/O	I_{OH} = 1.5mA, V_{CC} = 2V	-	0.08	0.4	V
			I_{OH} = 4.0mA, V_{CC} = 5V	-	0.11	0.4	
V_{OH}	High-level output voltage	I/O	I_{OH} = -0.4mA, V_{CC} = 2V	1.6	1.9	-	V
			I_{OH} = -1.0mA, V_{CC} = 5V	2.4	4.9	-	
I_{IL}	Input leakage current	/RST,SCLK	Note 3	-	-	500	μA
I_{OZ}	Output current when OFF	I/O	Note 3	-	-	500	μA
V_{TD}	Trickle Charge Diode Voltage Drop	-	-	-	0.7	-	V
R1	Trickle charge resistors	-	-	-	2	-	kΩ
R2		-	-	-	4	-	
R3		-	-	-	8	-	

Note:
1. I/O open, /RST set to a logic 0, and /EOSC bit = 0 (oscillator enabled).
2. I/O pin open, /RST high, SCLK=2MHz at V_{CC} = 5V; SCLK = 500kHz, V_{CC} = 2.0V, and /EOSC bit = 0 (oscillator enabled).
3. /RST, SCLK, and I/O all have 40kΩ pull-down resistors to ground.
4. /RST, I/O, and SCLK open. The /EOSC bit = 1 (oscillator disabled).
5. V_{CC2} = 0V.
6. V_{CC1} = 0V.
7. Typical values are at 25°C.

AC Electrical Characteristics

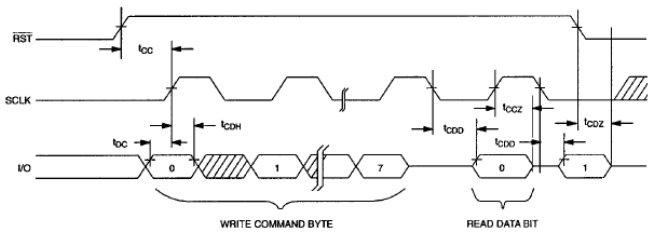


Figure 1: Timing diagram, Read data transfer

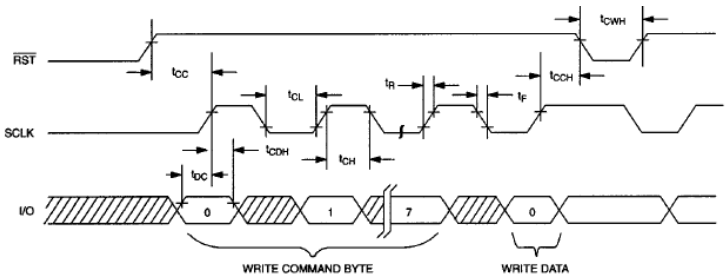


Figure 2: Timing diagram, Write data transfer

T_A = -40 ℃ to +85 ℃. Unless otherwise specified.

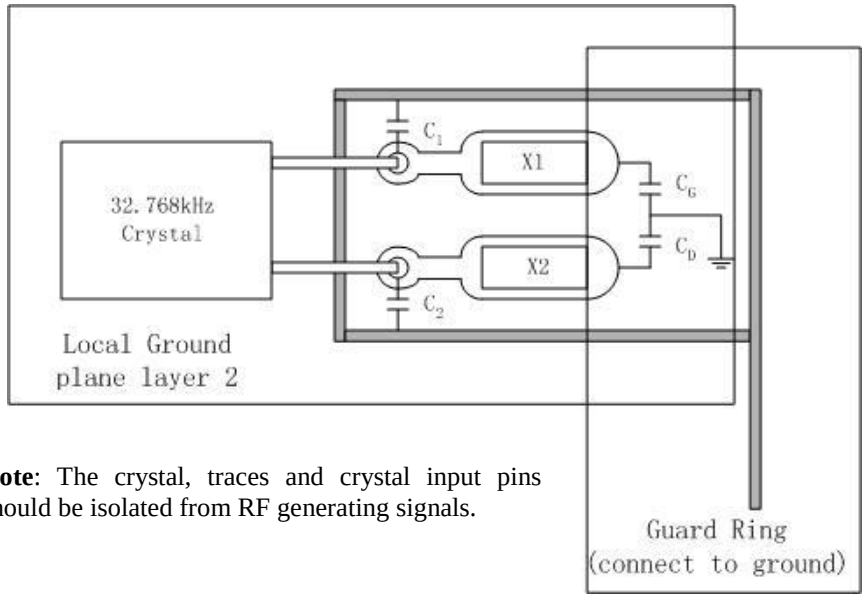
Parameter	Sym		Min	Typ	Max	Unit	Notes
Data to CLK Setup	t_{DC}	V_{CC}=2.0V	200	-	-	ns	1
		V_{CC}=5.0V	50	-	-		
CLK to Data Hold	t_{CDH}	V_{CC}=2.0V	280	-	-	ns	1
		V_{CC}=5.0V	70	-	-		
CLK to Data Delay	t_{CDD}	V_{CC}=2.0V	-	-	800	ns	1,2,3
		V_{CC}=5.0V	-	-	200		
CLK Low Time	t_{CL}	V_{CC}=2.0V	1000	-	-	ns	1
		V_{CC}=5.0V	250	-	-		
CLK High Time	t_{CH}	V_{CC}=2.0V	1000	-	-	ns	1
		V_{CC}=5.0V	250	-	-		
CLK Frequency	t_{CLK}	V_{CC}=2.0V	-	-	0.5	MHz	1
		V_{CC}=5.0V	0	-	2.0		

Parameter	Sym		Min	Typ	Max	Unit	Notes
CLK Rise and Fall	t_R ,t_F	V_{CC}=2.0V	-	-	2000	ns	1
		V_{CC}=5.0V	-	-	500		
$\overline{RST}$ to CLK Setup	t_{CC}	V_{CC}=2.0V	4	-	-	μs	1
		V_{CC}=5.0V	1	-	-		
CLK to $\overline{RST}$ Hold	t_{CCH}	V_{CC}=2.0V	240	-	-	ns	1
		V_{CC}=5.0V	60	-	-		
$\overline{RST}$ Inactive Time	t_{CWH}	V_{CC}=2.0V	4	-	-	μs	1
		V_{CC}=5.0V	1	-	-		
$\overline{RST}$ to I/O High-Z	t_{CDZ}	V_{CC}=2.0V	-	-	280	ns	1
		V_{CC}=5.0V	-	-	70		
SCLK to I/O High-Z	t_{CCZ}	V_{CC}=2.0V	-	-	280	ns	1
		V_{CC}=5.0V	-	-	70		

Note:

1. Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.
2. Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.
3. Load capacitance = 50pF.

Recommended Layout for Crystal



Note: The crystal, traces and crystal input pins should be isolated from RF generating signals.

Built-in Capacitors Specifications and Recommended External Capacitors

Parameter		Symbol	Typ	Unit
Build-in capacitors	X1 to GND	C_G	11	pF
	X2 to GND	C_D	11	pF
Recommended External capacitors for	X1 to GND	C_1	12	pF
crystal C_L=12.5pF	X2 to GND	C_2	12	pF
Recommended External capacitors for crystal C_L=6pF	X1 to GND	C_1	0	pF
	X2 to GND	C_2	0	pF

Note: The frequency of crystal can be optimized by external capacitor C_1 and C_2, for frequency=32.768 KHz, C_1 and C_2 should meet the equation as below:

$Cpar + [(C_1+C_G)*(C_2+C_D)]/ [(C_1+C_G)+(C_2+C_D)] = C_L$

Cpar is all parasitical capacitor between X1 and X2.

C_L is crystal's load capacitance.

Crystal Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency	f_O	-	32.768	-	kHz
Series Resistance	ESR	-	-	70	kΩ
Load Capacitance	C_L	-	6/12.5	-	pF

Function Description

Overview of Functions

1. Clock function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.

2. Interface with CPU

Simple 3-wire interface.

3. Oscillator enable/disable

Oscillator can be enabled or disable by /EOSC bit. But time count chain does not shut down when the bit is logic 1.

4. Charger function

The function is controlled by trickle charge register. Customer can select the charge current by select the number of diode and resistor value through the register.

For example:
Assume that a system power supply of 5V is applied to VCC2 and a super cap is connected to VCC1. Also assume that the trickle charger has been enabled with one diode and resistor R1 between VCC2 and VCC1. The maximum current IMAX would, therefore, be calculated as follows:

IMAX = (5.0V - diode drop)/R1 _ (5.0V - 0.7V) / 2kΩ _ 2.2mA

As the super cap charges, the voltage drop between VCC1 and VCC2 will decrease and, therefore, the charge current will decrease.

Registers

1. Allocation of registers

Addr. (hex) *1	Function	Register Definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds (00-59)	/EOSC*2	S40	S20	S10	S8	S4	S2	S1
01	Minutes (00-59)	0	M40	M20	M10	M8	M4	M2	M1
02	Hours (00-23 / 01-12)	12, /24	0	H20 or P /A	H10	H8	H4	H2	H1
03	Dates (01-31)	0	0	D20	D10	D8	D4	D2	D1
04	Months (01-12)	0	0	0	MO10	MO8	MO4	MO2	MO1
05	Days of the week (01-07)	0	0	0	0	0	W4	W2	W1
06	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
07	Control	WP*3	0	0	0	0	0	0	0
08	Trickle charger	TCS*4	TCS	TCS	TCS	DS*5	DS	RS*6	RS
1F	Clock burst*7	-	-	-	-	-	-	-	-
20~3E	RAM*9	-	-	-	-	-	-	-	-
3F	RAM burst*8	-	-	-	-	-	-	-	-

Caution points:

*1. PT7C4302 uses 5 bits for address. It's address byte consists of 1 + RAM/Clock select bit +5-bit addr. + Read/Write select bit.

*2. Oscillator Enable bit. When this bit is set to 1, oscillator is stopped but time count chain is still active.

*3. WP: Write Protect bit. WP bit should be cleared before attempting to write to the device.

*4. TCS: Trickle Charger Select.

*5. DS: Diode Select.

*6. RS: Resistor Select.

*7. Clock burst register address is used as clock/calendar burst mode operation address for consecutively read/write 0~7H registers. Clock/calendar burst mode operation can continuously read 0H to maximum 7H registers in order; write 0~7H registers in order. Less or larger than 8 bytes in clock burst write mode are ignored.

*8. RAM burst register address is used as RAM burst mode operation address for consecutively read/write 20~3EH RAM. Less than 31 bytes in RAM burst read/write mode are valid.

*9. PT7C4302 has 31×8 static RAM for customer use. It is volatile RAM.

*10. All bits marked with "0" are read-only bits. Their value when read is always "0". All bits marked with "-" are customer using space.

2. Control and status register

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
07	Control	WP	0	0	0	0	0	0	0
	(default)	0	0	0	0	0	0	0	0

WP: Write Protect bit.

WP	Data	Description
Read / Write	0	Write operation is enabled. Default
	1	Prevent a write operation to any other register.

3. Time Counter

Time digit display (in BCD code):

- Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
- Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
- Hour digits: See description on the /12, 24 bit. Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	Seconds	/EOSC*	S40	S20	S10	S8	S4	S2	S1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
01	Minutes	0	M40	M20	M10	M8	M4	M2	M1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
02	Hours	12, /24	0	H20 or P,/A	H10	H8	H4	H2	H1
	(default)	Undefined	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

*** Note:** /EOSC bit must be written into 0 to start the time count.

a) 12 / 24 bit

This bit is used to select between 12-hour clock operation and 24-hour clock operation.

12, /24	Description	Hours Register
0	24-hour time display	
1	12-hour time display	

24-hour clock	12-hour clock	24-hour clock	12-hour clock
00	92 (AM 12)	12	B2 (PM 12)
01	81 (AM 01)	13	A1 (PM 01)
02	82 (AM 02)	14	A2 (PM 02)
03	83 (AM 03)	15	A3 (PM 03)
04	84 (AM 04)	16	A4 (PM 04)
05	85 (AM 05)	17	A5 (PM 05)
06	86 (AM 06)	18	A6 (PM 06)
07	87 (AM 07)	19	A7 (PM 07)
08	88 (AM 08)	20	A8 (PM 08)
09	89 (AM 09)	21	A9 (PM 09)
10	90 (AM 10)	22	B0 (PM 10)
11	91 (AM 11)	23	B1 (PM 11)

Be sure to select between 12-hour and 24-hour clock operation before writing the time data.

4. Days of the week Counter

The day counter is a divide-by-7 counter that counts from 01 to 07 and up 07 before starting again from 01. Values that correspond to the day of week are user defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
05	Days of the week	0	0	0	0	0	W4	W2	W1
	(default)	0	0	0	0	0	Undefined	Undefined	Undefined

5. Calendar Counter

The data format is BCD format.

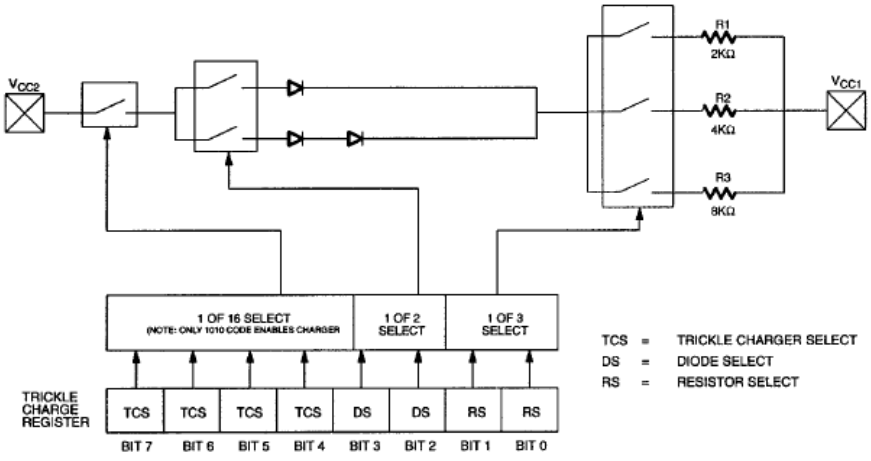
- Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).
  Range from 1 to 30 (for April, June, September and November).
  Range from 1 to 29 (for February in leap years).
  Range from 1 to 28 (for February in ordinary years).
  Carried to month digits when cycled to 1.
- Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99 and 00, 04, 08, …, 92 and 96 are counted as leap years.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
03	Dates	0	0	D20	D10	D8	D4	D2	D1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
04	Months	0	0	0	M10	M8	M4	M2	M1
	(default)	0	0	0	Undefined	Undefined	Undefined	Undefined	Undefined
06	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Note: Any registered imaginary time should be replaced by correct time, otherwise it will cause the clock counter malfunction.

6. Trickle Charger

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
8	Trickle charger	TCS	TCS	TCS	TCS	DS	DS	RS	RS
	(default)	0	1	0	1	1	1	0	0



a) Trickle Charger Select

Control the selection of the trickle charger.

TCS	Data	Description
Read/ Write	Other patent	Disable the trickle charger * Default 0101
	1010	Enable the trickle charger

b) Diode Select

Select whether one diode or two diodes are connected between VCC2 and VCC1.

DS	Data	Description
Read/ Write	00 or 11	The trickle charger is disabled independently of TCS. * Default
	01	One diode is selected.
	10	Two diodes are selected.

c) Resistor Select

Select whether one diode or two diodes are connected between VCC2 and VCC1.

RS	Data	Description
Read/ Write	00	No resistor. * Default
	01	R1 with typ. 2kΩ
	10	R2 with typ. 4kΩ
	11	R3 with typ. 8kΩ

Communication

1. 3-wire Interface

a) Command Byte

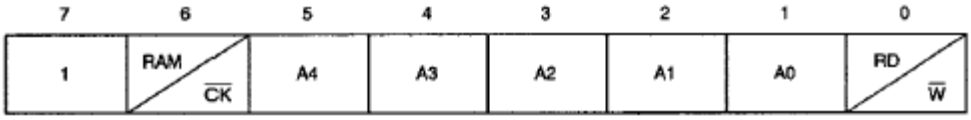


Figure 3: Command byte

The command byte is shown in Figure 1. Each data transfer is initiated by a command byte. The MSB (Bit 7) must be a logic 1. If it is 0, writes to the PT7C4302 will be disabled. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits 1 through 5 specify the designated registers to be input or output, and the LSB (bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic 1. The command byte is always input starting with the LSB (bit 0).

b) $\overline{\text{RST}}$ and SCL Signal

All data transfers are initiated by driving the $\overline{\text{RST}}$ input high and terminated by driving the $\overline{\text{RST}}$ input low. A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. If the $\overline{\text{RST}}$ input is low all data transfer terminates and the SDA pin goes to a high impedance state. Data transfer is illustrated in Figure 2 and Figure 3. At power-up, $\overline{\text{RST}}$ must be a logic 0 until VCC > 2.0V. Also SCLK must be at a logic 0 when $\overline{\text{RST}}$ is driven to a logic 1 state.

c) Single Byte Read

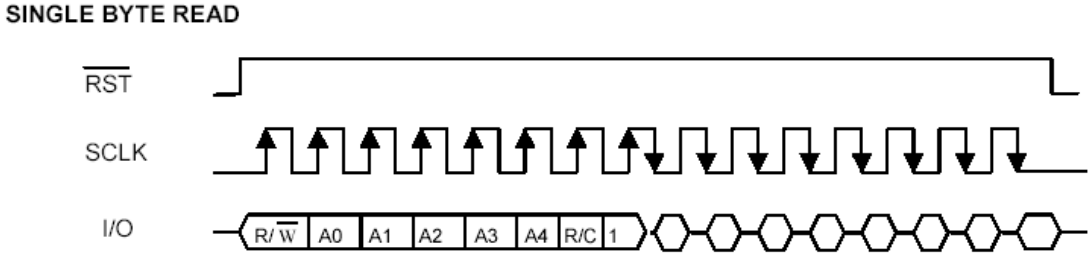


Figure 4: Single byte read

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles will transmit the same data bytes by PT7C4302 so long as $\overline{RST}$ remains high. This operation permits continuous burst mode read capability. Also, the SDA pin is tri-stated upon each rising edge of SCLK. Data is output starting with bit 0.

d) Single Byte Write

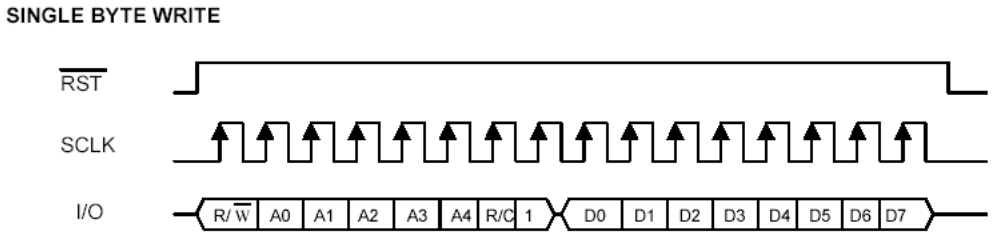


Figure 5: Signal byte write

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored. Data is input starting with bit 0.

e) Burst Mode

Burst mode is specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (Address bits: A4 A3 A2 A1 A0 = 1 1 1 1 1 showed in Figure 1). As before, bit 6 specifies clock or RAM and bit 0 specifies read or write. There is no data storage capacity at locations 9 through 31 in the Clock/Calendar Registers or location 31 in the RAM registers. Reads or writes in burst mode start with bit 0 of address 0.

When writing to the clock registers in the burst mode, the first eight registers must be written in order for the data to be transferred. If the number of transferred bytes is less than eight, the data will be ignored. However, when writing to RAM in burst mode, it is not necessary to write all 31 bytes for the data to transfer. Each byte that is written will be transferred to RAM regardless of whether all 31 bytes are written or not. Additional SCLK cycles are ignored.

- **Clock/Calendar Burst Mode**

The clock/calendar command byte specifies burst mode operation. In this mode the first eight clock/calendar registers can be consecutively read or written starting with bit 0 of address 0.

If the write protect bit is set high when a write clock/calendar burst mode is specified, no data transfer will occur to any of the eight clock/calendar registers (this includes the control register). The trickle charger is not accessible in burst mode.

At the beginning of a clock burst read, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

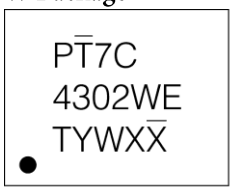
- **RAM Burst Mode**

The RAM command byte specifies burst mode operation. In this mode, the 31 RAM registers can be consecutively read or written starting with bit 0 of address 0.

Note: PT7C4302 use 94H, 96H as test mode address. Customer should not use the address.

Part Marking

W Package



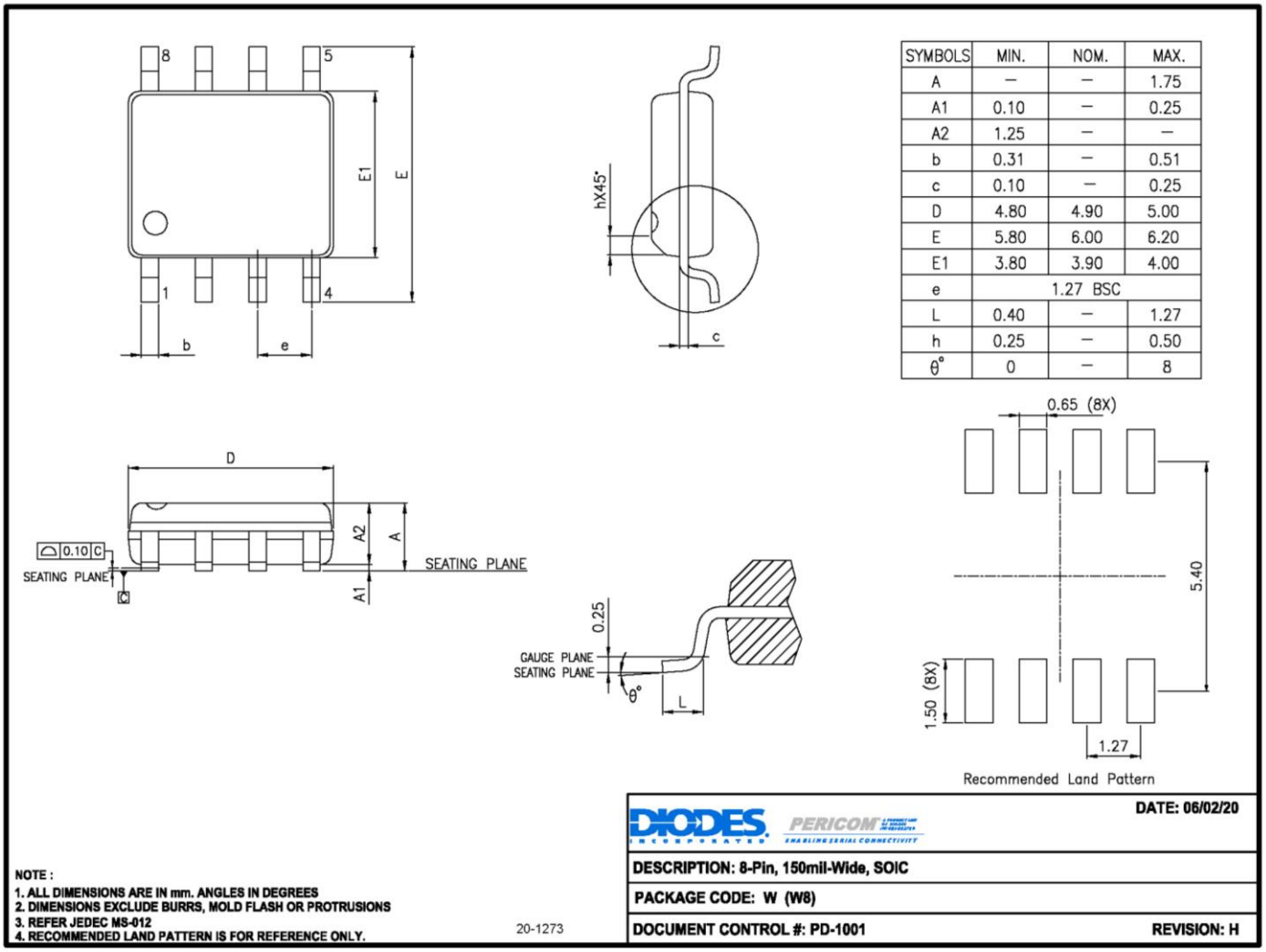
T: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code
Bar above "T" means Fab3 of MGN
Bar above 2nd "X" means Cu wire

ZE Package

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

Packaging Mechanical

8-SOIC (W)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. DIMENSIONS EXCLUDE BURRS, MOLD FLASH OR PROTRUSIONS
3. REFER JEDEC MS-012
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.

20-1273

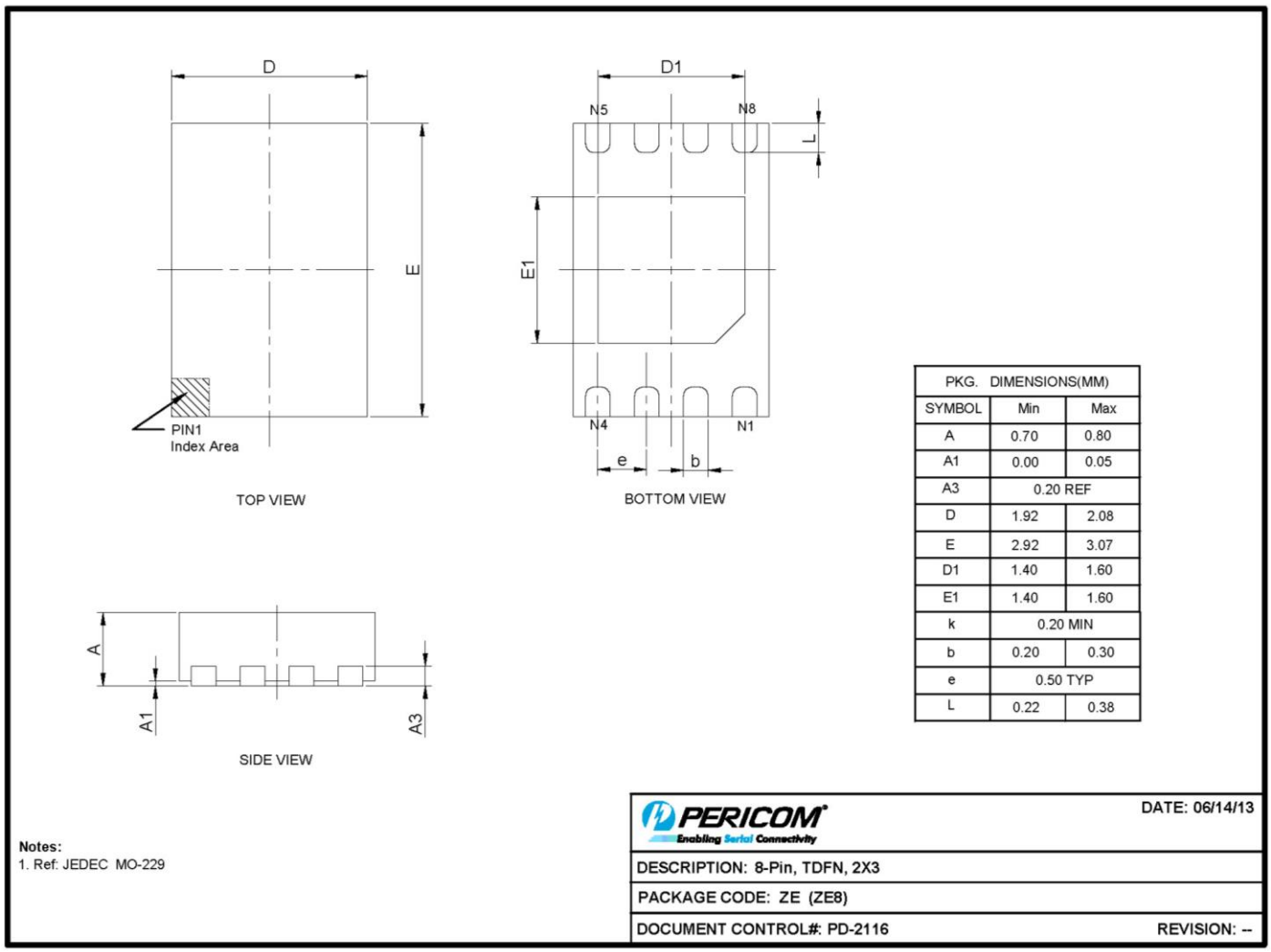
DATE: 06/02/20

DESCRIPTION: 8-Pin, 150mil-Wide, SOIC

PACKAGE CODE: W (W8)

DOCUMENT CONTROL #: PD-1001 REVISION: H

8-TDFN (ZE)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
D	1.92	2.08
E	2.92	3.07
D1	1.40	1.60
E1	1.40	1.60
k	0.20 MIN	
b	0.20	0.30
e	0.50 TYP	
L	0.22	0.38

13-0155

For latest package info.

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Ordering Information

Part Number	Package Code	Package Description
PT7C4302WEX	W	8-Pin, 150mil-Wide (SOIC)
PT7C4302ZEEX	ZE	8-Pin, 2x3 (TDFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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