SET-TOP BOX SERIES SINGLE LNB CONTROLLER AND POWER SUPPLY IC

Summary

The ZLPM8012 is a power management and control solution for satellite set-top boxes (STBs). Based on an efficient boost converter the ZLPM8012 provides the power supply and all the control signals required by a single port satellite Low Noise Block (LNB). The ZLPM8012 includes an accurate 22kHz tone generator to provide DiSEqC™ control words or continuous tone for band switching control. Controlled by I^2C and with the minimal external components the ZLPM8012 provides a high performing cost efficient solution.

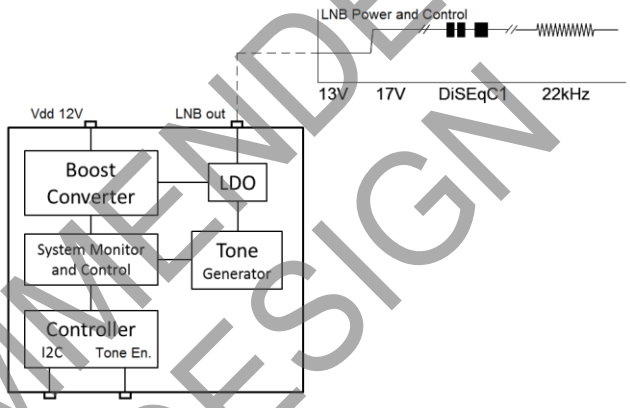
Features

- Efficient boost converter providing an accurate adjustable power supplies LNBs
- Operates from a single rail supply
- Provides a protected output of up to 550mA
- Adjustable current limit for system flexibility
- Designed for stability with low power LNBs
- Provides standard voltage / tone and DiSEqC control signals and allows for regional variations.
- Internal 22kHz generator for DiSEqC control and traditional band switching
- 22kHz maintains shape across all load conditions
- Controlled by I^2C
- Built in multiple diagnostics and protection for IC and LNB protection
- Minimal external components for a simple, reliable and cost effective solution
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- Single tuner Satellite Set-top boxes
  - High current LNBs
  - Stability with minimal current LNBs
- Satellite PC Cards
- TV's with integrated satellite tuners
- Hybrid Set-top boxes
- Suitable for Digital and Analog satellite systems

System Diagram



Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

DiSEqC is a trademark of Eutelsat.

Product Description

The ZLPM8012 range provides a highly integrated monolithic power management solution to meet the demands of satellite receiver Low Noise Blocks (LNBs). Its internal circuit blocks include an efficient boost converter, a low noise low dropout regulator (LDOR), a tone generator and modulator, an I^2C interface and a logic tone enable pin. Most internal circuits are powered by an internal 3.3V regulator. A block diagram of the ZLPM8012 is shown in Figure 1.

Boost Converter and LNB Power Supply

The boost converter is used to generate a user trimable 13V/18V LNB supply using a standard STB power rail of 12V. The operating frequency of this switching converter is user controlled over the range 100kHz to 500kHz. The frequency is selected using an external capacitor wired to pin Fosc. The ZLPM8012 uses internal frequency compensation to maintain the loop stability of the switching regulator. This highly efficient converter includes over-voltage and over-current protection.

The boost converter supplies a low noise, low voltage drop linear regulator used for tone modulation and LNB isolation as part of STB power saving strategies. The LDOR also provides line open-circuit, line short circuit, soft start and current limiting systems. The boost converter/LDOR combination can supply a continuous LNB load of up to 550mA. The LNB supply V_{OUT} is programmable to allow the user to provide accurate cable length compensation, specialist markets or to search for the voltage threshold level of the LNB.

The slew rate of V_{OUT} is programmable via capacitor CS. This capacitor is not required for stability reasons so it can be omitted.

The V_{OUT} output of the ZLPM8012 can be enabled or disabled using the I^2C Enable control bit. When disabled, the IC adopts a very low current Stand-By mode where all non-essential circuits are shut down.

22kHz Generation

The ZLPM8012 includes a 22kHz tone generator that can be used for LNB band switching or DiSEqC signalling. The tone frequency is user adjustable over the range 12kHz to 50kHz, set by a capacitor-resistor network connected to pin Tosc. Alternately, the RC network can be omitted and an external tone source can be applied via the Tosc pin instead. Tone on/off is controlled using the I^2C or an independent logic pin Ten. When the tone generator is enabled the tone generated is modulated on the DC output of the LDOR via the pin V_{OUT}.

Internal 3.3V Supply Availability

An internal 3.3V regulated supply is made available on the Creg pin to be utilised by other systems within the set-top box. Care should be taken that any load applied here should not exceed the limit quoted in the Specifications table and also that the total power dissipation limit of the ZLPM8012 is also observed.

System Control and Features Using I^2C

To minimise STB micro-controller IO pin requirements, I^2C is used as the primary control interface for the ZLPM8012, providing bi-directional information exchange containing a range of control signals, DiSEqC data and diagnostics. ZLPM8012 features controlled via the I^2C bus include output enable, polarisation selection, regional selection Standard/Japanese, output voltage trim covering the range of 10.25V to 19.5V in 0.25V steps, V_{OUT} rise and fall time, tone on and current limit adjustment. Diagnostic information available includes over-temperature shutdown, over-current shutdown, over-current shutdown, output not-in regulation, short on V_{OUT} line, remote tone present and under-voltage lockout. The active I^2C address of the IC is user selected from one of four possible addresses, allowing re-use of the I^2C bus without address conflicts and hence further minimising micro-controller IO requirements.

System Control Using Logic

To further increase STB system design flexibility a logic tone enable pin is provided in addition to I^2C control.

Protection and Diagnostics

The ZLPM8012 provides a wide range of system protection and diagnostic features. These include Over Current Limit, Line Short Circuit, Line Open Circuit, Over Temperature Shutdown and Under Voltage alerts.

Current Limit

A user defined low power resistor (Riset) sets the maximum current limit for the LNB port, adjustable over the range 200mA to 550mA. This control provides two levels of over-current protection for the V_{OUT} port. If load current reaches the defined current limit, V_{OUT} is controlled (allowed to fall) to ensure that the current limit is not exceeded, the Out Of Regulation flag is set in the I^2C status register and an internal timer is started. If the over-load persists for longer than 65ms, the STS/INT pin is set low, the Over-Current flag in the I^2C status register is set and the port is permanently disabled. The port can re-enabled by re-starting the (V_{IN}) power supply or by clearing then re-enabling the I^2C Enable control bit, once the fault condition has been resolved.

There are also two secondary current limits which can be set by the I^2C control registers. These can be used by the STB controlling firmware to reduce output current capability for certain applications (see I^2C control register definition section).

Enable Sequence

Each time the ZLPM8012 is enabled, the IC performs a Shorted Line test by a sourcing a small current (10mA typical) to determine the V_{OUT} pin load resistance. If a short is detected, the Short on V_{OUT} line flag in the I^2C status register is set. If no short-circuit is detected, the IC then initiates a Soft-Start sequence where the programmed V_{OUT} pin output voltage is applied using a controlled ramp-up time.

Line Check

At any time the IC is enabled, it can perform a Line Open Circuit test. To activate this test, the Nlnb bit in the I^2C control register should be set. When set, the IC outputs a V_{OUT} target voltage of 22V, current limited to 5mA. If a load greater than 5mA is present (indicating an LNB is connected), the Output Not In Regulation flag will remain clear. If no load is present (indicating an open line), the flag will be set. Once the test has established the load status, the No LNB control bit can be cleared and normal operation resumed.

Over Temperature Protection

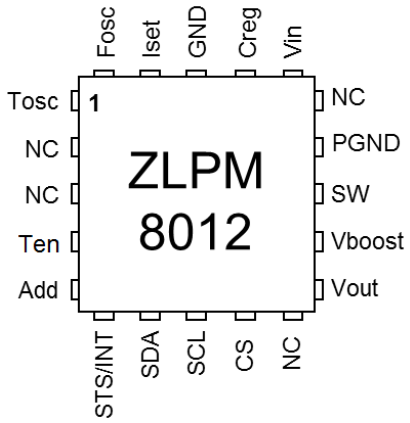
To enhance system reliability, the ZLPM8012 includes an Over-Temperature Shutdown circuit which is set internally at a typical junction temperature of +145°C. Under this fault condition, the V_{OUT} output will be disabled, the STS/INT pin will be set low and the Over-Temperature flag in the I^2C status register will be set. Once the die temperature falls back within acceptable operational limits, the V_{OUT} output can be re-enabled and the STS/INT and I^2C status register Over-Temperature flags cleared by toggling I^2C EN bit.

Power Up Sequence

Each time the ZLPM8012 is powered up, all internal functions of the IC are inhibited by an Under Voltage Lockout circuit until the voltage on the V_{IN} pin exceeds 8.5V. Once V_{IN} is above this level, the internal control registers of the ZLPM8012 are set to default levels. The STS/INT pin is set low to mark an Under Voltage event and to request microcontroller attention. The V_{OUT} output will be in a disabled state. The STS/INT flag can be cleared by reading the I^2C status register. The ZLPM8012 can be enabled by setting the I^2C EN control bit high.

This power-up sequence ensures that the IC will not give spurious outputs during power-up.

Pin Assignments



Pin Description

Pin	Pin Name	Function
16	V_{IN}	Input Supply
18	GND	Signal GND
14	PGND	Power GND
13	SW	Internal boost converter MOSFET drain
12	V_{BOOST}	Boost converter output voltage sense
11	V_{OUT}	Linear regulator output to LNB
9	CS	Capacitor setting V_{OUT} slew-rate
17	C_{REG}	Bypass capacitor for internal 3.3V supply regulator
20	F_{OSC}	Capacitor setting boost converter operating frequency
19	I_{SET}	Current limit setting resistor
1	T_{OSC}	R/C network setting tone oscillator frequency or External tone input
4	T_{EN}	Enable tone modulation of V_{OUT} output
6	STS/INT	Status pin (or host interrupt signal output) used to indicate alert status or request the host microcontroller to read its status register.
7	SDA	I2C data line
8	SCL	I2C clock line
5	ADD	Resistor selecting active I2C address
2, 3, 10, 15	NC	No connect, these pins should be left open or connected to Gnd
PAD	PAD	Ground / Heatsink (internally connected to Gnd)

Functional Diagram

The functional diagram below in Figure 1 shows the internal architecture of the ZLPM8012.

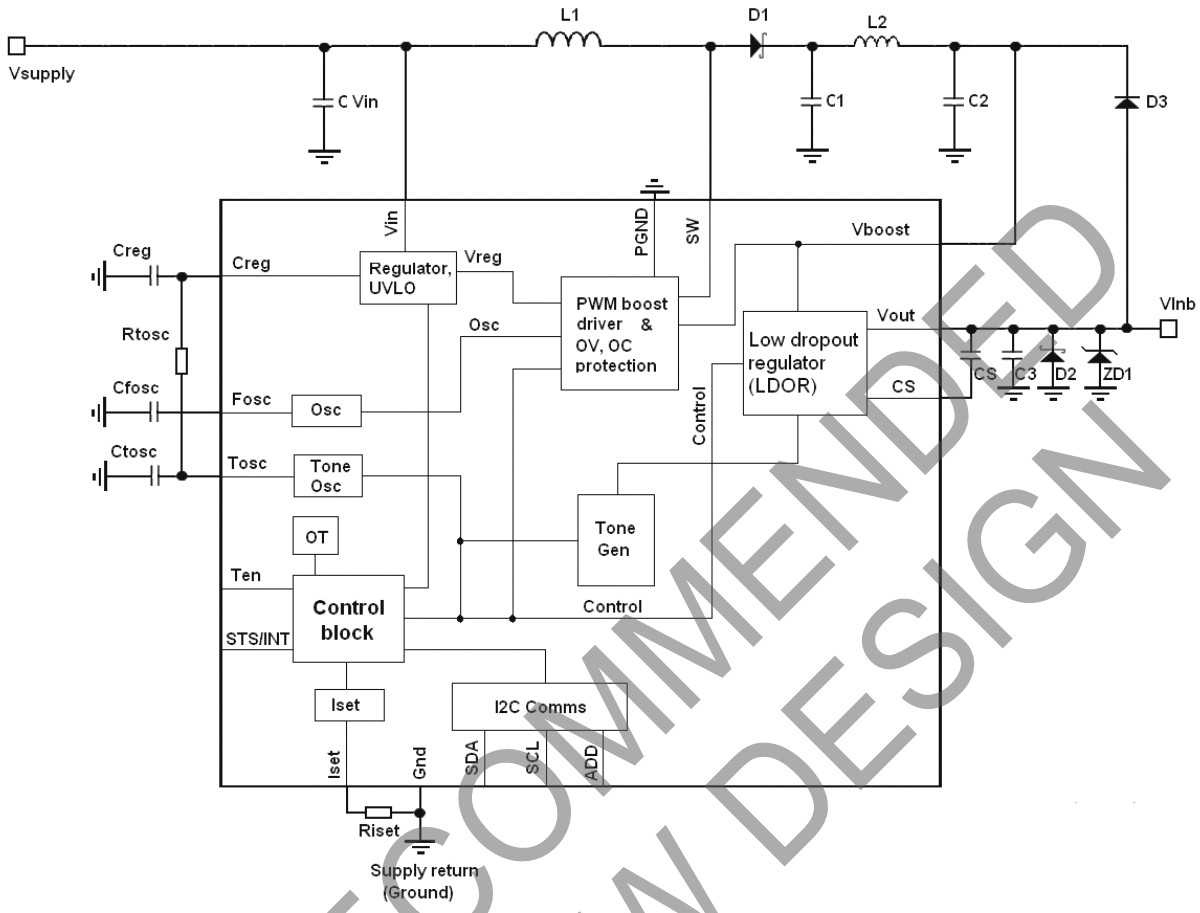


Figure 1. ZLPM8012 Functional Diagram

Component List			
Name	**Value**	**Name**	**Value**
R_{TOSC} (Note 4)	60k	C3	330nF
RI_{SET}	130k for 550mA see I_{SET} chart for other values	C_{VIN}	4.7µF
C_{REG}	2.2µF Ceramic	L1	6.8µH, 3A $I_{\_SAT}$, 60mΩ
C_{FOSC}	47pF	L2	2.2µH, 1A $I_{\_SAT}$
C_{TOSC} (Note 4)	500pF	D1	B130L
CS	1nF	D2	B130L
C1	10uF Ceramic 1210 25V X5R 10% generic	D3	ES1A
C2	20µF Ceramic (2X10µF) 1210 25V X5R 10% generic	ZD1	3.0SMCJ20A

Note: 4. Can be omitted if an external tone source is used.

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{IN})	-0.3 to +20	V
V_{OUT}, V_{BOOST}, CS	-0.3 to +40	V
SW	-0.3 to +26	V
T_{OSC}, ADD, I_{SET}, F_{OSC}, C_{REG}	-0.3 to +3.6	V
T_{EN}. STS/INT, SDA, SCL	-0.3 to +5.5	V
Maximum V_{OUT} Load Current	1	A
Operating Temperature	-20 to +85	°C
Storage Temperature	-55 to +150	°C
Junction Temperature	+125	°C

Electrical Characteristics (T_{AMB} = +25°C, Supply Voltage = 12V, I_{OUT} = 80mA, $V_{SET}1$ = 0, $V_{SET}2$ = 1, $V_{SET}3$ = 0, unless otherwise specified.)

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage Operating Range	(Note 5)	9	12	16	V
V_{IN} Supply Current	I_{OUT} = 0mA, Enable = 1, boost disconnected	—	3.5	—	mA
Supply Current (Ena.)	I_{OUT} = 0mA, Enable = 1	—	6	—	mA
Supply Current (Disab.)	Enable = 0, I_{CREG} = 0	—	600	1000	µA
UVL Threshold	Supply voltage rising	7.5	8.0	8.5	V
UVL Hysteresis	—	—	0.29	—	V
Switching Freq.					
Range	—	100	—	500	kHz
Frequency	C_{FOSC} = 47pF	200	300	370	kHz
Power Switch (SW)					
On Resistance	I_{SW} = 300mA	—	300	—	mΩ
Current Limit	—	—	2	—	A
Leakage(Off)	Enable = 1, V_{SW} = 20V	—	10	20	µA
V_{OUT}					
Output Voltage Low (Std)	Test Circuit Figure 1, I_{LOAD} = 300mA, Pol Sel = 0	12.75	13.25	13.75	V
Output Voltage High (Std)	Test Circuit Figure 1, I_{LOAD} = 300mA, Pol Sel = 1	17.75	18.25	18.75	V
Output range Low (Std)	—	12.75	—	14.5	V
Output range High (Std)	—	17.75	—	19.5	V
Output Voltage Low (LR)	Test Circuit Figure 1, I_{LOAD}= 300mA, Pol Sel = 0	10.25	10.75	11.25	V
Output Voltage High (LR)	Test Circuit Figure 1, I_{LOAD} = 300mA, Pol Sel = 1	14.25	14.75	15.25	V
Output range Low (LR)	—	10.25	—	12.0	V
Output range High (LR)	—	14.25	—	16.0	V
V_{STEP}	Set by I^2C	—	0.25	—	V
Output rise time	From 13.25 to 18.25V, CS = 1nF	—	500	—	µs
Output fall time	From 18.25 to 13.25V, Total C_{OUT} < 1µF	—	500	—	µs
Output Current	V_{OUT} active (Note 6)	0	—	550	mA
Output Ripple	Test Circuit Figure 1, I_{LOAD} = 550mA, Pol Sel = 1	—	20	—	mV

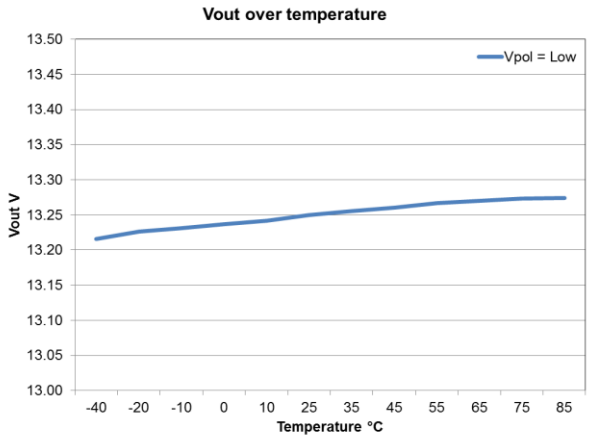
Notes: 5. V_{SUPPLY} – 1.5V should not exceed V_{OUT} under normal operating conditions.
6. The V_{OUT} supply will not start-up if the load resistance is less than target stated (start-up only).

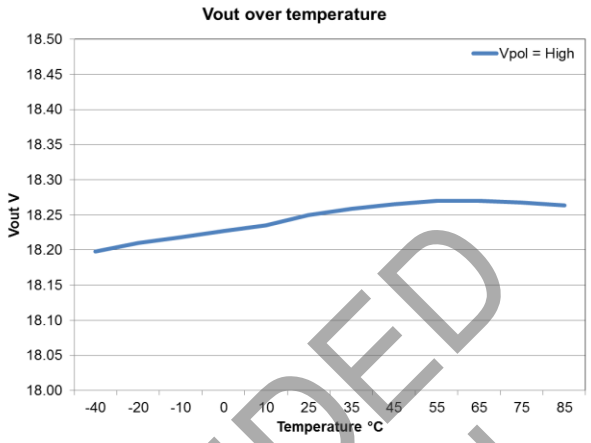
Electrical Characteristics (continued) (T_{AMB} = +25°C, Supply Voltage = 12V, I_{OUT} = 80mA, $V_{SET}1$ = 0, $V_{SET}2$ = 1, $V_{SET}3$ = 0, unless otherwise specified.)

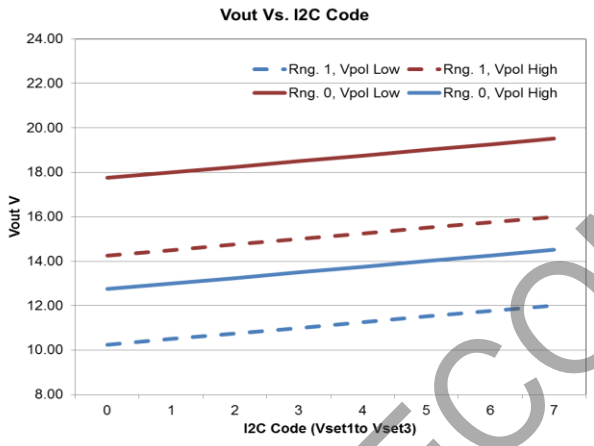
Parameter	Conditions	Min	Typ	Max	Unit
dV_{OUT} / dV_{IN}	—	—	0.5	5	mV/V
dV_{OUT} / dIl	Pol Sel = 0	—	220	—	mV/A
dV_{OUT} / dT	—	—	50	—	ppm/°C
Startup					
Soft start	Standard applications circuit	—	1.3	—	ms
Short circuit detect	(Note 6)	—	20	—	Ω
Tone Generator					
Tone frequency	C_{TOSC} = 500pF, R_{TOSC} = 60k	20	22	24	kHz
Tone amplitude pk-pk	V_{OUT} load capacitance < 500nF	400	600	800	mV
Tone duty cycle	—	45	50	55	%
Tone rise and fall times	V_{OUT} load capacitance < 500nF Trf = 0	5	7.5	15	µs
Tone rise and fall times	V_{OUT} load capacitance < 500nF Trf = 1	2.5	5	7.5	µs
Tone start up	Tone frequency = 22kHz	0	22	50	µs
Tone shut down	Tone frequency = 22kHz	0	22	50	µs
Tosc Input frequency rng.	3.3V logic signal, 50% duty cycle	12	—	50	kHz
I^2C Interface					
Input voltage low	—	—	—	0.94	V
Input voltage high	—	2.4	—	5.5	V
Input current (SCL/ SDA)	Input voltage = 0 to 5.5V	-10	—	10	µA
SDA logic out	I_{SDA} = 3mA	—	—	0.4	V
SCL clock frequency	—	—	—	400	kHz
Logic Control					
Tenable inactive	—	0	—	0.8	V
Tenable active	—	2.4	—	5.5	V
Input current	Input voltage = 0 to 5.5V	-10	—	10	µA
Internal Regulator (C_{REG})					
Output Current Range	—	0	—	50	mA
Current Limit	V_C_{REG} = 0V	50	95	115	mA
Output Voltage	—	3.135	3.3	3.465	V
Protection and Diagnostics					
Thermal Shutdown	Junction temperature increasing	—	+145	—	°C
Thermal Shutdown Hysteresis	—	—	+15	—	°C
Over current shutdown	—	550	—	850	mA
Over current shut down delay timer	—	—	65	—	ms
LNB detect current	V_{OUT} = 22V, Status Register N_{REG} flag set on No LNB	3	5	8	mA
I_{VOUT} Reverse (En.)	Enabled, V_{OUT} = 21V, (Note 7)	—	100	—	mA
I_{VOUT} Reverse (Dis.)	Disabled, V_{OUT} = 21V	—	600	2000	µA
$V_{STS/INT}$ Low	$I_{STS/INT}$ = 3mA	0	—	0.4	V
$I_{STS/INT}$ Leakage	$V_{STS/INT}$ = 5.5V	—	—	10	µA
ESD					
All Pins except Iset	HBM test conditions	4	—	—	kV
I_{SET}	HBM test conditions	2	—	—	kV

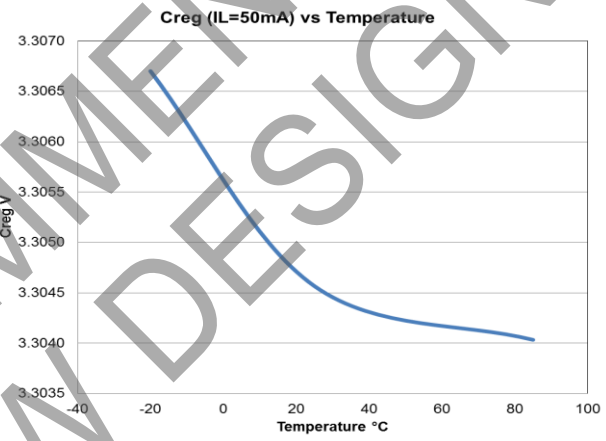
Notes: 6. The V_{OUT} supply will not start-up if the load resistance is less than target stated (start-up only).
7. After 65ms, the output will be automatically disabled and the OCS and STS/INT flags will be set.

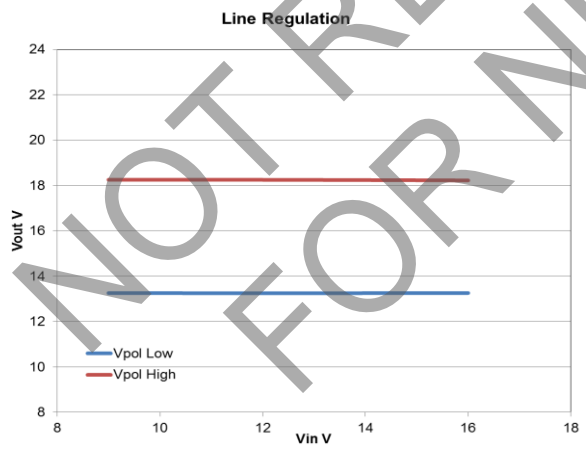
Typical Characteristics

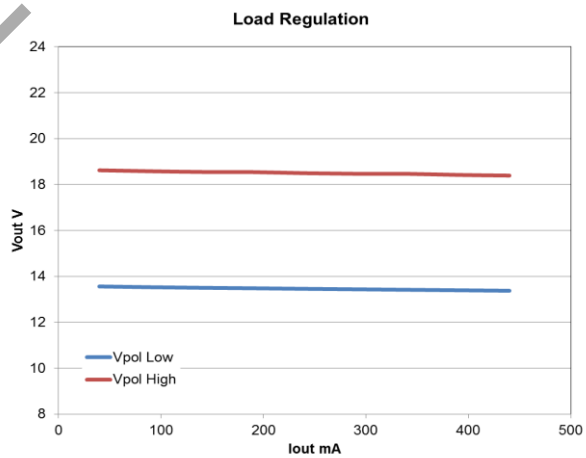




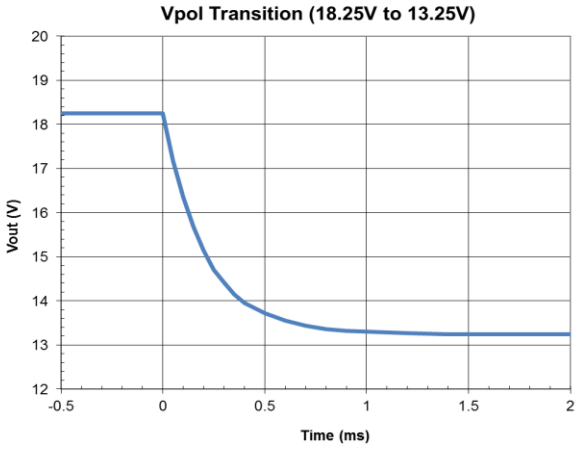


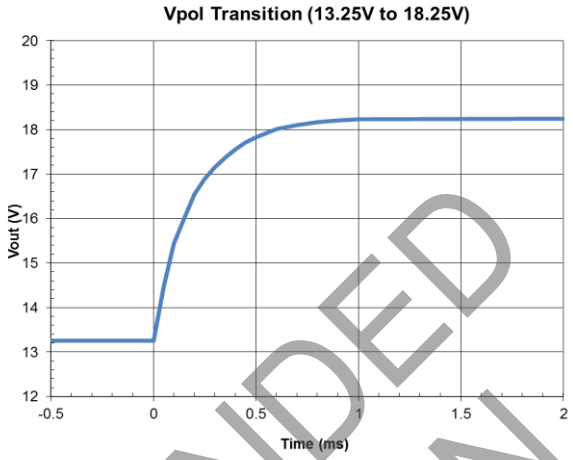


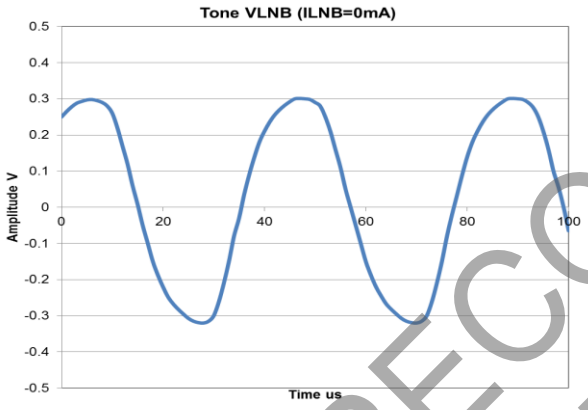


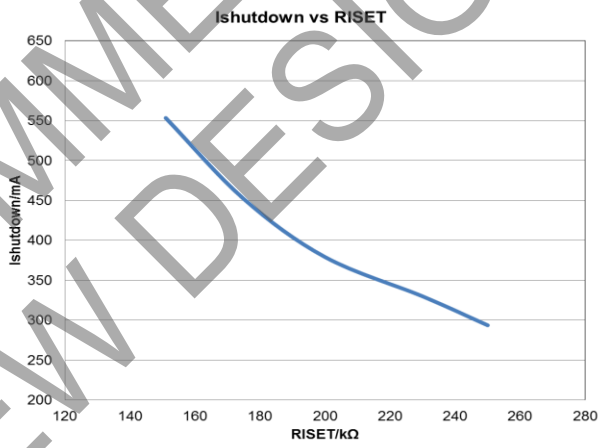


Typical Characteristics (continued)









Application Information

Boost Converter

The ZLPM8012 uses internal frequency compensation to maintain the loop stability of the switching regulator. This compensation places some limits on the allowable inductor and load capacitor used in the switching converter. Please follow the application circuit examples for typical values and limits.

The boost converter includes over-current and other protection circuits. Current limiting is performed cycle by cycle with a trip threshold set by the RI_{SET} resistor. To minimize external components the RI_{SET} has a dual purpose, it's also used to control the LDO current limit as described in the LDO section below. The default RI_{SET} value of 160kΩ gives a SW pin current limit of approximately 2.2A. Exceeding this current will cause the present switching cycle to be terminated immediately, however the converter will continue to function.

The operating frequency of the boost converter is controlled by Cfosc. The default value of 47pF gives a typical frequency of 290kHz. By adjusting C_{FOSC}, this frequency can be varied over the range 100kHz to 500kHz (130pF to 27pF respectively). If this frequency is changed, it is possible that the values of related components of the boost generator (L1, L2, C1 and C2 in Fig. 1) will need adjustment.

Boost converter stability is not sensitive to low ESR output capacitor types. Output ripple is dependent on the ESR of C1 and C2. Dependent on output ripple requirements, inductor L2 can be omitted and C1 and C2 can merged as a single ceramic capacitor (consider values around 47µF).

Given the low resistance and fast switching speed of the boost converter switching transistor of the ZLPM8012, the boost circuit is capable of achieving a conversion efficiency of >96%. The boost inductor L1 and rectifier D1 are important in achieving this performance. Inductor L1 must be low resistance (preferably <60mΩ), have low core losses and have an adequate saturation current (>2A). Avoid inductors with air-gaps close to the PCB since they can cause power loss and coupled noise into adjacent circuits. The rectifier D1 must have a low Vf and very fast reverse-recovery time. Be aware that the very lowest Vf Schottky diodes can have considerable leakage, particularly when hot. Allow for diode leakage losses in power dissipation calculations. Mount D1 and C1 close to the SW and Pgnd pins of the ZLPM8012 to minimize radiated EMI. The ZLPM8012 evaluation board provides a good layout example, please contact Diodes Incorporated for more details.

Low Dropout Regulator (LDOR)

The LDOR block of the ZLPM8012 performs a number of important tasks including output enable control, tone signal insertion, soft-start control, polarisation change slew-rate control, LNB present detection, shorted line detection, externally applied over-voltage detection and output current limit control.

The LDOR has been designed to operate into a capacitive load in the range of 200nF to 1µF, using a push-pull circuit to output tone signals without any DC load requirements.

The LDOR of the ZLPM8012 is protected against externally applied over-voltage events. These can come from sources such as shorts to other STBs or nearby lightning discharges. If shorted to a STB that is set to give a higher output voltage, the ZLPM8012 will respond by setting its N_{REG} status flag and also attempting to pull down the V_{OUT} pin to its target output voltage. If the external source is low impedance, then the ZLPM8012 will current limit at a safe level (100mA typical). Should the fault continue for more than 65ms, the STS/INT pin will be pulled low, the OCS status flag will be set and the LDOR will be disabled, switching into a high impedance state. Once the fault is removed, the device can be re-enabled. Lightning surges are dealt with by the protection components ZD1, D2 and D3.

The maximum (V_{OUT}) output current capability of the ZLPM8012 is user adjustable over the range 200mA to 550mA using RI_{SET}. The graph I_Shutdown vs RI_{SET} in the *Typical Characteristics* section shows the relationship between Riset and maximum I_load. This control can be used to limit not only the maximum LNB load current but also the peak current taken from the system 12V power supply during start-up and polarisation voltage changes. An additional control of peak system current is the capacitor CS which sets the slew-rate of V_{OUT} during polarisation voltage changes. The recommended value of CS (1nF) gives typical 10%-90% transition times of 500us. The minimum recommended value for CS is 100pF. Note that the slew-rate control given by CS is not active when the tone generator of the ZLPM8012 is enabled.

Application Information (continued)

Tone Generator

The ZLPM8012 includes a versatile tone generator/modulator that can be used for LNB band switching or DiSEqC signalling. An internal tone oscillator or an external (logic) signal can be used as the tone source. Tone On/Off (V_{OUT} modulation) is controlled using the I^2C bus. Possible tone generator implementations include:

1) Internal tone oscillator switched/modulated using I^2C .
2) External tone input (to the T_{OSC} pin) switched/modulated using I^2C.
3) External tone burst input pre-modulated with Band/ DiSEqC control (with Ten logic pin wired permanently high). Please note that tone burst inputs must always end logic low in this mode.

ZLPM8012 internal logic ensures that above modes (1) and (2) always gives complete cycles of tone, regardless of modulation timing. This logic also generates envelope information for mode (3). The tone signal processing ensures that the DC voltage level on V_{OUT} is not affected by tone modulation.

To use the internal tone oscillator, a resistor capacitor network (as shown in Fig.1) should be connected to pin T_{OSC}. The following table shows the recommended component values required for commonly used oscillator output frequencies.

Output Tone Frequency (kHz)	R_T_{OSC} (kΩ)	C_T_{OSC} (pF)
22	60	500
43	56	270

Tone Frequency = (660000/(R x C) kHz (Approx.)
(R in kΩ, C in pF)

Regardless of the signal waveform applied to the Fosc pin of the ZLPM8012, the IC will always generate a square-wave tone output. Edge speeds can be user selected using the I^2C Trf control bit. When the Trf bit is set to 0 (default), tone signal rise high). Please note that tone burst inputs must always end logic low in this mode.

I^2C Interface

For generic information about the electrical specifications and protocols of an I^2C interface, please consult the NXP document UM10204 I^2C-bus specification and user manual Rev.03 – 19th June 2007.

The I^2C interface of the ZLPM8012 provides access to a single status register and two control registers. All registers are 8 bits in length and use the same I^2C bus address. The status register can be read by submitting an I^2C read command using the bus address of the ZLPM8012. On receipt of this command, the ZLPM8012 will acknowledge the request and then output the status byte, sending the MSB first. The bus master can re-read the status byte indefinitely if it acknowledges each byte received. A read sequence can be finished either by sending a “not-acknowledge” signal at the end of a byte read or by sending a Stop command. The I^2C bus master cannot write to the status register.

The control registers can be written by submitting an I^2C write command using the bus address of the ZLPM8012. On receipt of this command, the ZLPM8012 will acknowledge the request. Following this acknowledge signal, the I^2C bus master will then be able to write to the control registers, one byte at a time, under the control of a register address counter. The first data byte sent will be copied into Control Register 1 and the second into Control Register 2. Each byte received by the ZLPM8012 will be acknowledged. If further bytes are sent by the I^2C bus master, the register address counter will wrap around so that the next byte will be copied into Control Register 1 and the next into Control register 2 etc.

A write sequence is terminated by the I^2C bus master sending a Stop command. It is permissible to write just one byte (which will be copied into Control Register 1). The I^2C bus master cannot read the contents of the control registers.

Application Information (continued)

I²C Addressing

To avoid system conflicts the ZLPM8012 provides a choice of four I²C addresses. To help minimise the pin count the ZLPM8012 uses a single pin to set the address. This is achieved by adding a single resistor connected between the Add pin and Gnd. The table below shows the address to resistor value relationship. A resistor tolerance of +/-5% is sufficient. The address bit marked "x" denotes the I²C R/W bit, which should be low for Write and high for Read.

	Address	Resistor value
Address 1	0001000x	Zero Ω (GND)
Address 2	0001001x	68k
Address 3	0001010x	360k
Address 4	0001011x	Open Circuit

I²C Registers

Status register

Bit	Name	Description	STS/INT	Flag
0	OTS	Over temperature shutdown	Yes	Cleared by Status read after cooling
1	OCS	Over current shutdown	Yes	Cleared when Enable is reset
2	N_{REG}	Output not in regulation	No	Cleared Automatically
3	S_{LNB}	Short on V_{OUT} line (active low)	No	Cleared Automatically
4	TBD	To be defined	—	—
5	UVL	Under voltage lock	Yes	Set when Vin enters normal working range
6	TBD	To be defined	—	—
7	TBD	To be defined	—	—

Over Temperature Shut Down (OTS)

If the junction temperature of the ZLPM8012 exceeds +145°C, the over temperature register and STS/INT flags are set. Also the boost converter and the V_{OUT} output are disabled, regardless of the state of the Enable control. The device can only be re-enabled once the junction temperature has fallen to a safe operating level. The OTS flag can be cleared by a status register read. The STS/INT flag can be cleared by reading the status register, by changing the I²C Enable control.

Over Current Shut Down (OCS)

If the V_{OUT} output of the ZLPM8012 is overloaded, the device will initially allow Vout to fall to limit the output current to the level set by R_I_{SET}. The fault is indicated by setting the N_{REG} flag but an interrupt is not given at this time to avoid flagging spurious current spikes such as transients from polarization changes. However, after 65ms the over current is determined as a real fault and the OCS register and the STS/INT flags are set. The over current and interrupt flags can be reset using a status register read operation. The ZLPM8012 can be restarted by clearing then re-enabling the active enable control input (I2C). If the over current fault still persists, the process will be repeated.

The OCS flag can also be set if an external voltage source is used to drive the V_{OUT} pin to greater than its target voltage. (This can happen if two STB LNB outputs are accidentally connected together.) The ZLPM8012 is designed to withstand this fault and to limit the resulting input current to 100mA typical. To avoid the risk of excessive power dissipation in a sustained fault condition of this type, the OCS control circuit will trigger after 65ms, shutting down the V_{OUT} output and setting the STS/INT pin low. The ZLPM8012 can be restarted normally once the fault has been rectified.

Output Not in Regulation (N_{REG})

The output not in regulation register flag is set when the V_{OUT} output is pulled away from its target voltage, usually by a faulty load. This flag automatically clears when the fault is removed. Its primary use is in detecting an open circuit LNB line (see the N_{LNB} control bit). The Nreg bit may be set transiently during start-up or polarisation change events if the V_{OUT} load includes a large capacitor. An N_{REG} event does not set the STS/INT flag.

Application Information (continued)

Short on V_{OUT} Line (S_{LNB})

Whenever the V_{OUT} output is enabled, the ZLPM8012 executes a shorted-line test. During this test, the device outputs a current of 10mA typical and monitors the output voltage. The ZLPM8012 will only enable its full output current capability when V_{OUT} exceeds 200mV during this test. The short on V_{OUT} line register flag is active (low) for the duration of the test and is automatically cleared (high) if and when V_{OUT} rises above 200mV. The S_{LNB} test has no effect on the STS/INT flag.

Under Voltage Lock (UVL)

The under voltage lockout circuit of the ZLPM8012 inhibits all device operation when voltage on V_{IN} is below the UVL threshold. Once V_{IN} returns to its normal operating range, the UVL register and STS/INT flags are set to signal the power-up/brown-out event. Also, all I^2C control registers are set to default states and V_{OUT} is disabled. The UVL register flag can be cleared by a status register read. The STS/INT flag can be cleared by reading the I^2C status register and changing the I^2C EN control bit.

Control Register 1

Bit	Name	POR Value	Bit Setting	Description
0	V_{SET} 1	0	See V_{OUT} control table	3 bits are used for LNB supply voltage trimming, adjusting the output voltage in 0.25V increments
1	V_{SET} 2	1	See V_{OUT} control table	
2	V_{SET} 3	0	See V_{OUT} control table	
3	Pol Sel	0	0 = low V_{OUT} range 1 = high V_{OUT} range	Single bit selection of the polarization channel
4	V_{POL} Rng.	0	0 = standard V_{POL} range 1 = Japan V_{POL}	Sets the LNB to the Standard or Japanese voltage range
5	—	0	Set to 0	Not Used
6	Tone	0	0 = tone output disabled 1 = tone output enabled	Tone output on or off
7	Enable	0	0 = V_{OUT} disabled 1 = V_{OUT} enabled	Enable/Disable the V_{OUT} Output

Control Register 2

Bit	Name	POR Value	Bit Setting	Description
0	I_{SET}1	0	See I_{SET} table	Current limit bit 1
1	I_{SET}2	0	See I_{SET} table	Current limit bit 2
2	N_{LNB}	0	0 = LNB test disable 1 = Test for LNB presence	Activates the No LNB test. The Status N_{REG} bit set if no LNB is found.
3	Trf	0	0 = 10µs 1 = 5µs	Sets the rise and fall time of the tone
4	—	0	Set to 0	Not used
5	—	0	Set to 0	Not used
6	—	0	Set to 0	Not used
7	—	0	Set to 0	Not used

Application Information (continued)

V_{OUT} Control

To simplify the I^2C commands the ZLPM8012 has 5 bits to select and control the output. The LNB polarization select (Pol Sel) bit is used to select between horizontal and vertical or left and right polarisation to eliminate difficult calculations when compensating for line lengths. If necessary the output voltage can be trimmed in increments of +/- 0.25V steps from the centre voltages of 13.25V/10.75V and 18.25V/14.75V. Once the adjustment has been decided the V_{SET} bits can remain constant for each state. This makes it possible to switch between the compensated V_{OUT} voltages by using pol select alone. To provide greater market flexibility the ZLPM8012 has a regional bit which sets the V_{OUT} centres at 10.75V and 14.75V instead of 13.25V and 18.25V.

		Enable	V_{POL} Rng.	Pol Sel	$V_{SET}3$	$V_{SET}2$	$V_{SET}1$	V_{OUT} Adj	LNB V
LNB Range Standard	Vertical	1	0	0	0	0	0	-0.50	12.75
		1	0	0	0	0	1	-0.25	13.00
		1	0	0	0	1	0	0.00	13.25
		1	0	0	0	1	1	0.25	13.50
		1	0	0	1	0	0	0.50	13.75
		1	0	0	1	0	1	0.75	14.00
		1	0	0	1	1	0	1.00	14.25
		1	0	0	1	1	1	1.25	14.50
	Horizontal	1	0	1	0	0	0	-0.50	17.75
		1	0	1	0	0	1	-0.25	18.00
		1	0	1	0	1	0	0.00	18.25
		1	0	1	0	1	1	0.25	18.50
		1	0	1	1	0	0	0.50	18.75
		1	0	1	1	0	1	0.75	19.00
		1	0	1	1	1	0	1.00	19.25
		1	0	1	1	1	1	1.25	19.50
LNB Range Low	Vertical	1	1	0	0	0	0	-0.50	10.25
		1	1	0	0	0	1	-0.25	10.50
		1	1	0	0	1	0	0.00	10.75
		1	1	0	0	1	1	0.25	11.00
		1	1	0	1	0	0	0.50	11.25
		1	1	0	1	0	1	0.75	11.50
		1	1	0	1	1	0	1.00	11.75
		1	1	0	1	1	1	1.25	12.00
	Horizontal	1	1	1	0	0	0	-0.50	14.25
		1	1	1	0	0	1	-0.25	14.50
		1	1	1	0	1	0	0.00	14.75
		1	1	1	0	1	1	0.25	15.00
		1	1	1	1	0	0	0.50	15.25
		1	1	1	1	0	1	0.75	15.50
		1	1	1	1	1	0	1.00	15.75
		1	1	1	1	1	1	1.25	16.00

Application Information (continued)

Tone On (Tone)

When set, this control bit selects the addition of a low level tone signal to the Vout output of the ZLPM8012. Please refer to the Applications section of this datasheet for advice on tone source and frequency selection.

Enable

This control bit activates the Boost converter and LDO stages of the ZLPM8012 to provide the pre-determined output voltage at Vout. If whilst the Enable control is set, the ZLPM8012 gets internally disabled by an OTS or OCS event, then the control bit must be cleared before the device can be re-enabled.

I^2C Current Limit ($I_{SET}1$, $I_{SET}2$)

In addition to the maximum current setting via Iset, the ZLPM8012 allows an additional three current limit steps by using I^2C control. This allows STB firmware to set-up the LNB power supply to match the intended application. The three extra steps are 40%, 50% and 67% of I_{SET}. The truth table below shows the I^2C register set-up and an example of the maximum output current based on an Iset of 550mA.

I2C Register		LNB Supply Current	
$I_{SET}2$ (Bit 1)	$I_{SET}1$ (Bit 0)	% of I_{SET}	I_{OUT} Max (mA)
0	0	100%	550
0	1	67%	368
1	0	50%	275
1	1	40%	220

No LNB Present (N_{LNB})

Set this control bit to select the No LNB Detection mode. In this mode, the ZLPM8012 will generate a V_{OUT} of 22V with a pre-set current limit of 5mA nominal. If a load of less than 5mA is connected to V_{OUT}, its output will remain at 22V and the ZLPM8012 will set the Nreg flag of the Status register, indicating that no LNB is present. If an LNB load of greater than 5mA is connected to the V_{OUT}, current limiting will occur and the voltage on V_{OUT} will fall. This is detected by the ZLPM8012 which will clear the Nreg flag of the Status register. De-select the LNB Detection mode for normal operation of the ZLPM8012.

Tone Risetime (Trf)

The bit controls the rise and fall times of the any tone added to its V_{OUT} output by the ZLPM8012. When clear, rise and fall times of 10µs nominal are generated. When set, rise and fall times of 5µs nominal are generated. Generally, 10us is used for standard (22kHz) tone signals and 5µs for Japanese (higher frequency tones).

System Design Considerations - Device Mounting

Under normal STB operation, the boost converter and regulator functions of the ZLPM8012 can result in an internal power dissipation of 0.5W to 2W dependant on the STB load. To help remove the heat generated by this power dissipation the device must be provided with adequate heatsinking. Most of the heat dissipated in the components of the IC flows through the die, die attach and finally the package frame, exiting through the metal tab in the base of the device. It is vital that this tab is soldered to a PCB designed to give a low thermal resistance. This can be achieved by using the following recommendations:

1) Use a double-sided multi-(4) layer PCB with 1 ounce copper (35µm) or thicker on top/bottom sides. The inner layers and back-side of the PCB should have substantial unbroken areas of copper directly underneath the ZLPM8012.
2) There should be at least 4, but preferably 9 or more thermal vias in the PCB between the device tab and the back of the board. These should be plated with 0.5 ounce copper (18µm) or thicker.
3) The PCB housing must be designed so that the back of the PCB adequate air-flow, particularly near the ZLPM8012.Other components mounted on the PCB that may dissipate high power levels should not be placed close to the ZLPM8012.

The J-C (junction-to-case) thermal resistance of the ZLPM8012 is typically 5.5°C/W. When designing a PCB for use with the ZLPM8012, the user must take into account the likely power dissipation, the recommended maximum die temperature, the maximum ambient temperature and the combined thermal resistance of the device and its PCB mounting arrangement.

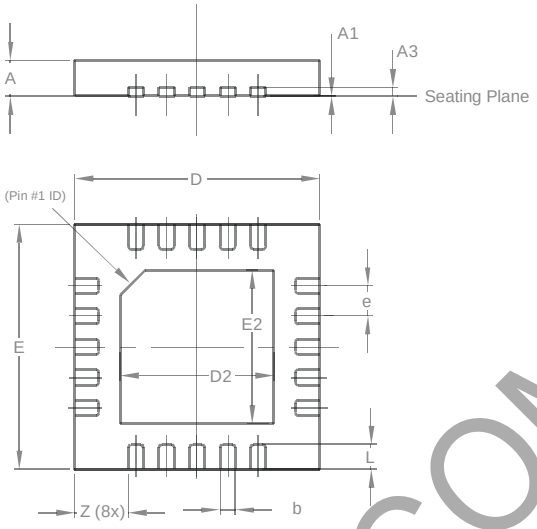
Ordering Information

Device	Package	Reel Size	Tape Width	Quantity per Reel
ZLPM8012JB20TC	U-QFN4040-20	13” (330mm)	12mm	3000

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-QFN4040-20

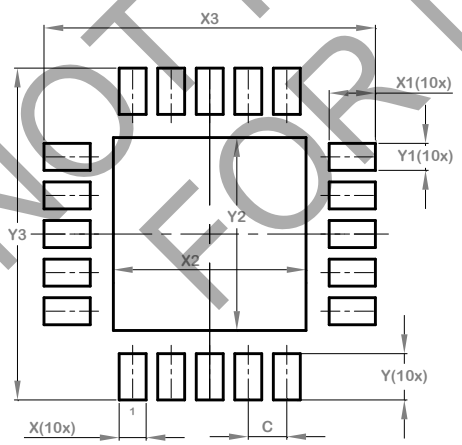


U-QFN4040-20			
Dim	Min	Max	Typ
A	0.55	0.65	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	3.95	4.05	4.00
D2	2.40	2.60	2.50
E	3.95	4.05	4.00
E2	2.40	2.60	2.50
e	0.50 BSC		
L	0.35	0.45	0.40
Z	-	-	0.875
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-QFN4040-20



Dimensions	Value (in mm)
C	0.500
X	0.350
X1	0.600
X2	2.500
X3	4.300
Y	0.600
Y1	0.350
Y2	2.500
Y3	4.300

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