

ZXMN2F30FH

20V SOT23 N-channel enhancement mode MOSFET

Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ (Ω)	I_D (A)
20	0.045 @ $V_{GS} = 4.5V$	4.9
	0.065 @ $V_{GS} = 2.5V$	4.1



Description

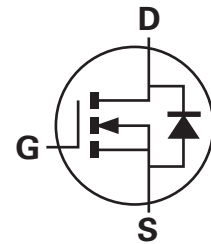
This new generation Trench MOSFET from Zetex features low on-resistance achievable with low (2.5V) gate drive.

Features

- Low on-resistance
- 2.5V gate drive capability
- SOT23 package

Applications

- Buck/Boost DC-DC Converters
- Load switching and SMPS
- Charging applications in portable equipment
- Motor Control
- LED Lighting

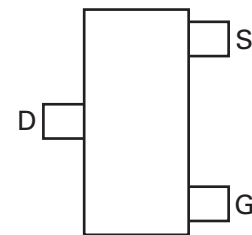


Ordering information

DEVICE	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMN2F30FHTA	7	8	3000

Device marking

KNC



Top view

ZXMN2F30FH

Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Drain source voltage	V_{DSS}	20	V
Gate source voltage	V_{GS}	± 12	V
Continuous Drain Current @ $V_{GS}=4.5$; $T_A=25^\circ\text{C}^{(b)}$ @ $V_{GS}=4.5$; $T_A=70^\circ\text{C}^{(b)}$ @ $V_{GS}=4.5$; $T_A=25^\circ\text{C}^{(a)}$	I_D	4.9	A
		4.0	A
		4.1	A
Pulsed drain current ^(c)	I_{DM}	22.6	A
Continuous source current (body diode) ^(b)	I_S	1.6	A
Pulsed source current (body diode) ^(c)	I_{SM}	22.6	A
Power dissipation at $T_A=25^\circ\text{C}^{(a)}$	P_D	0.96	W
Linear derating factor		7.6	mW/°C
Power dissipation at $T_A=25^\circ\text{C}^{(b)}$	P_D	1.4	W
Linear derating factor		11.2	mW/°C
Operating and storage temperature range	T_j, T_{stg}	-55 to 150	°C

Thermal resistance

Parameter	Symbol	Limit	Unit
Junction to ambient ^(a)	$R_{\theta JA}$	131	°C/W
Junction to ambient ^(b)	$R_{\theta JA}$	89	°C/W
Junction to Lead ^(d)	$R_{\theta JL}$	68	°C/W

NOTES:

(a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.

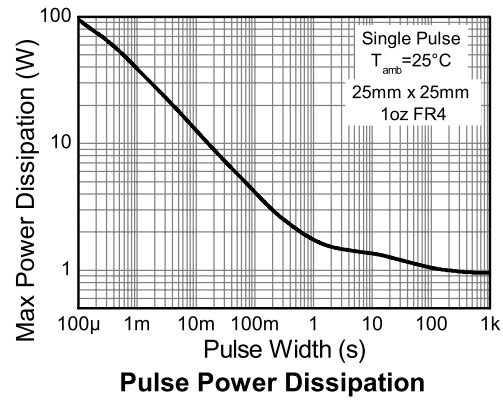
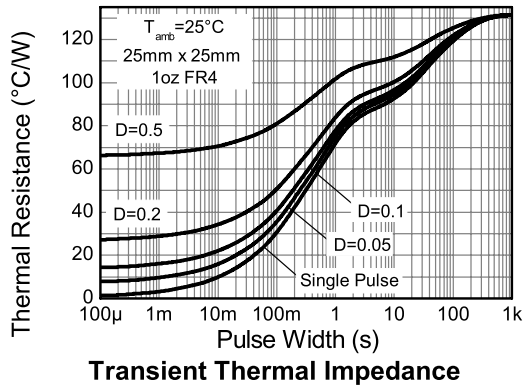
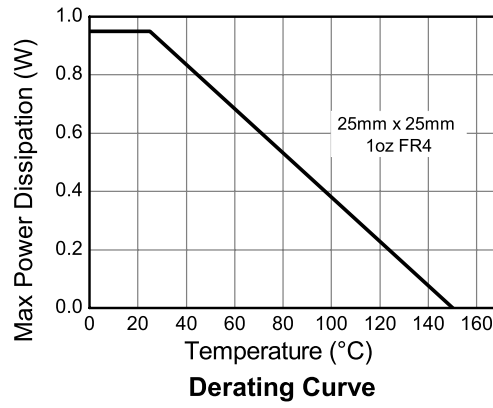
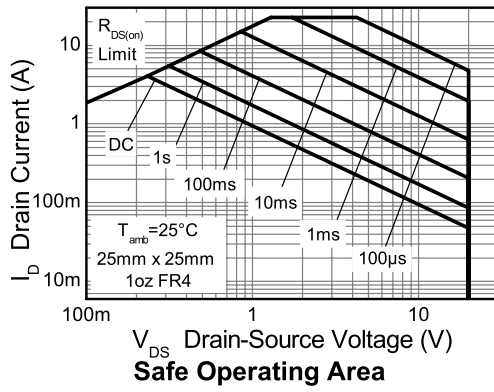
(b) For a device surface mounted on FR4 PCB measured at $t \leq 5$ sec.

(c) Repetitive rating - 25mm x 25mm FR4 PCB, $D=0.02$, pulse width 300 μs - pulse width limited by maximum junction temperature.

(d) Thermal resistance from junction to solder-point (at the end of the drain lead).

ZXMN2F30FH

Thermal characteristics



ZXMN2F30FH

Electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	20			V	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	$V_{DS} = 20\text{V}$, $V_{GS} = 0\text{V}$
Gate-Body Leakage	I_{GSS}			100	nA	$V_{GS} = \pm 12\text{V}$, $V_{DS} = 0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.6	0.9	1.5	V	$I_D = 250\mu\text{A}$, $V_{DS} = V_{GS}$
Static Drain-Source On-State Resistance (*)	$R_{DS(on)}$			0.045 0.065	Ω Ω	$V_{GS} = 4.5\text{V}$, $I_D = 2.5\text{A}$ $V_{GS} = 2.5\text{V}$, $I_D = 2.0\text{A}$
Forward Transconductance ^{(*)(†)}	g_{fs}		8.6		S	$V_{DS} = 10\text{V}$, $I_D = 3\text{A}$
Dynamic (†)						
Input Capacitance	C_{iss}		452		pF	$V_{DS} = 10\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	C_{oss}		102		pF	
Reverse Transfer Capacitance	C_{rss}		58		pF	
Switching (‡)(†)						
Turn-On-Delay Time	$t_{d(on)}$		2.9		ns	$V_{DD} = 10\text{V}$, $V_{GS} = 4.5\text{V}$ $I_D = 1\text{A}$ $R_G \approx 6.0\Omega$
Rise Time	t_r		5.6		ns	
Turn-Off Delay Time	$t_{d(off)}$		19.4		ns	
Fall Time	t_f		10.2		ns	
Total Gate Charge	Q_g		4.8		nC	$V_{DS} = 10\text{V}$, $V_{GS} = 4.5\text{V}$ $I_D = 3.5\text{A}$
Gate-Source Charge	Q_{gs}		1		nC	
Gate Drain Charge	Q_{gd}		1.2		nC	
Source-drain diode						
Diode Forward Voltage ^(*)	V_{SD}		0.75	1.2	V	$I_S = 1.25\text{A}$, $V_{GS} = 0\text{V}$

NOTES:

(*) Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

(†) For design aid only, not subject to production testing.

(‡) Switching characteristics are independent of operating junction temperature.

Typical characteristics

Fig1. $I_D - V_{DS}$

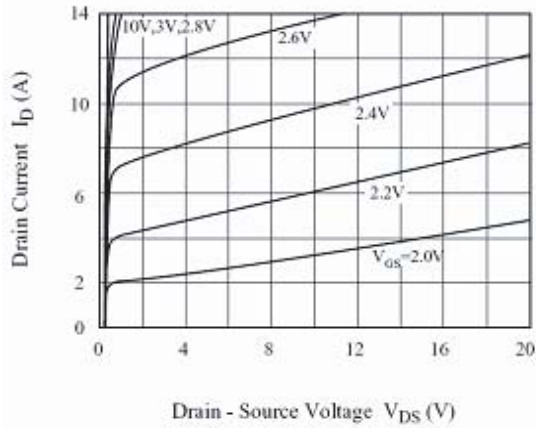


Fig2. $R_{DS(on)} - I_D$

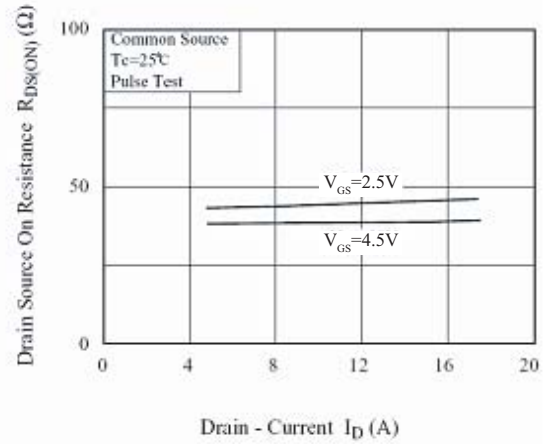


Fig3. $I_D - V_{GS}$

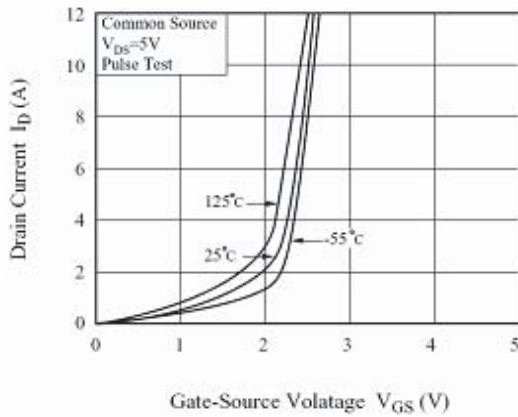


Fig4. $R_{DS(on)} - T_J$

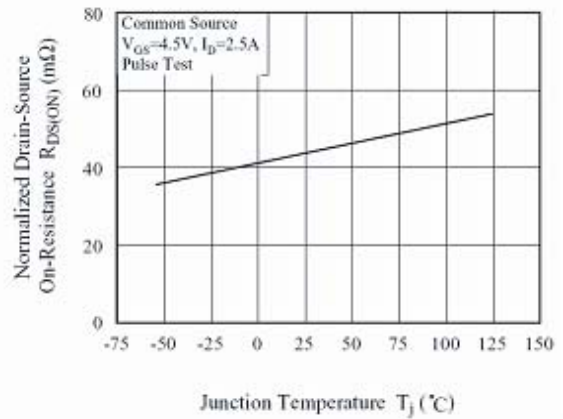


Fig5. $V_{th} - T_J$

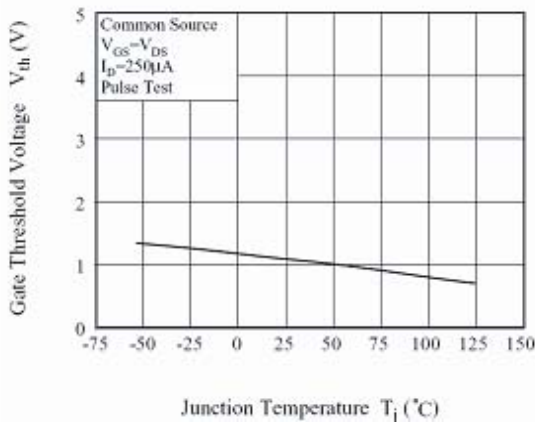
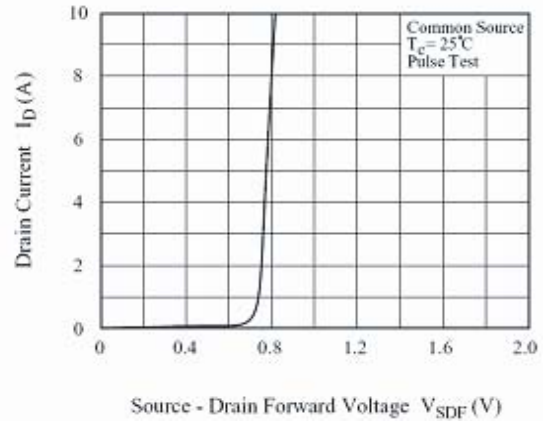
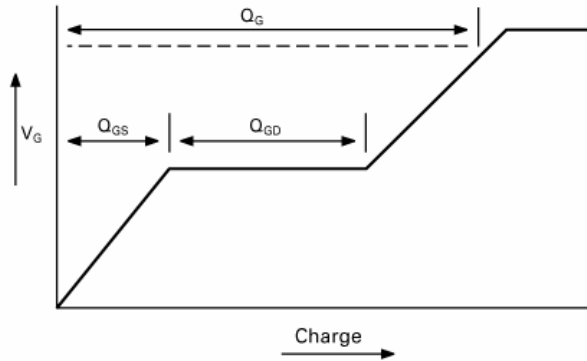


Fig6. $I_S - V_{SDF}$

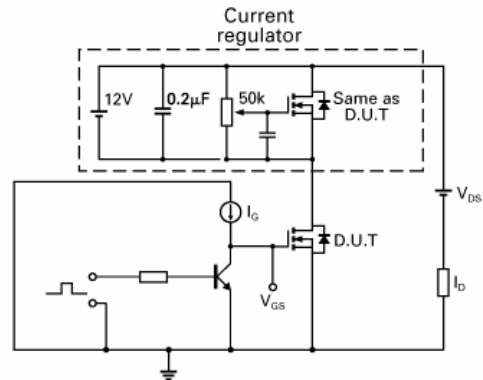


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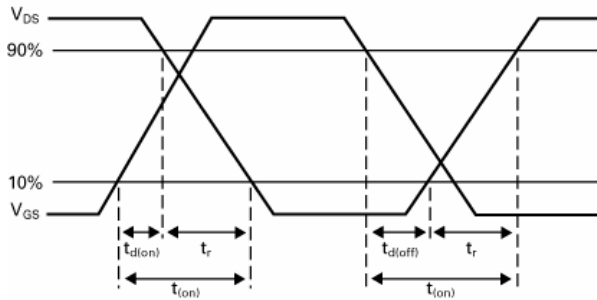
Test circuits



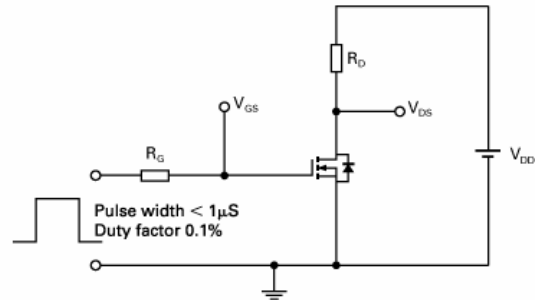
Basic gate charge waveform



Gate charge test circuit



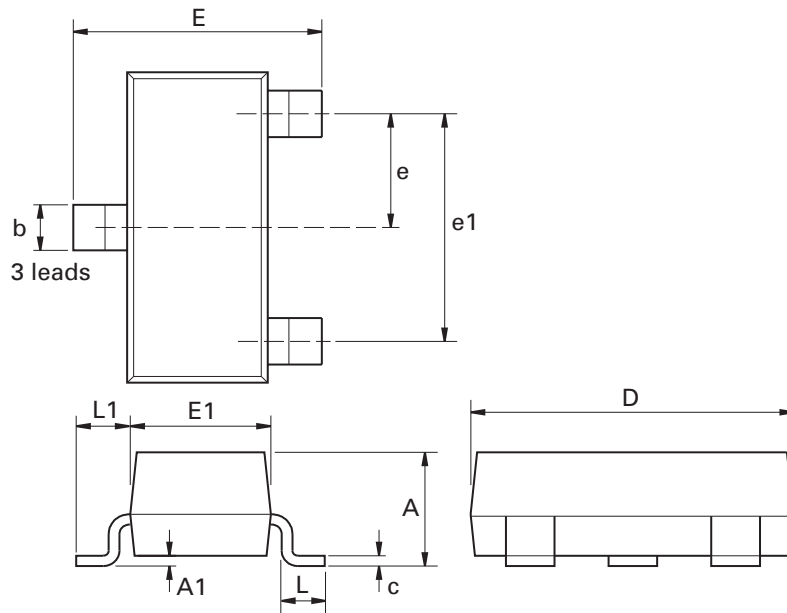
Switching time waveforms



Switching time test circuit

ZXMN2F30FH

Package outline - SOT23



Dim.	Millimeters		Inches		Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	-	1.12	-	0.044	e1	1.90 NOM		0.075 NOM	
A1	0.01	0.10	0.0004	0.004	E	2.10	2.64	0.083	0.104
b	0.30	0.50	0.012	0.020	E1	1.20	1.40	0.047	0.055
c	0.085	0.20	0.003	0.008	L	0.25	0.60	0.0098	0.0236
D	2.80	3.04	0.110	0.120	L1	0.45	0.62	0.018	0.024
e	0.95 NOM		0.037 NOM		-	-	-	-	-

Note: Controlling dimensions are in millimeters. Approximate dimensions are provided in inches

ZXMN2F30FH

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Europe	Americas	Asia Pacific	Corporate Headquarters
Zetex GmbH Kustermann-park Balanstraße 59 D-81541 München Germany Telephone: (49) 89 45 49 49 0 Fax: (49) 89 45 49 49 49 europe.sales@zetex.com	Zetex Inc 700 Veterans Memorial Highway Hauppauge, NY 11788 USA Telephone: (1) 631 360 2222 Fax: (1) 631 360 8222 usa.sales@zetex.com	Zetex (Asia Ltd) 3701-04 Metroplaza Tower 1 Hing Fong Road, Kwai Fong Hong Kong Telephone: (852) 26100 611 Fax: (852) 24250 494 asia.sales@zetex.com	Zetex Semiconductors plc Zetex Technology Park, Chadderton Oldham, OL9 9LL United Kingdom Telephone: (44) 161 622 4444 Fax: (44) 161 622 4446 hq@zetex.com

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