DIA2602

High Voltage, Rail-to-Rail Output Operational Amplifiers

Description

The DIA2602 (dual) is an amplifier with very low noise, high voltage, and low power. The DIA2602 has a high gain-bandwidth product of 3.5 MHz, a slew rate of 2.5 V/μs, and a quiescent current of 0.75 mA per amplifier at 4.5 V typically.

The DIA2602 is designed to provide optimal performance in low voltage and low noise systems. All these chips provide rail-to-rail output swing into heavy loads. The input common-mode voltage ranges from -0.1 to (+V_S - 1.5) V, and the maximum input offset voltage is 3.5 mV for the DIA2602.

It is specified over the extended industrial temperature range -40°C to 125°C. The operating range is from 4.5 V to 36 V.

Features

- AEC-Q100 qualified
- Device temperature grade 1: -40°C ~ 125°C
- HBM ESD at ±2000 V
- CDM ESD at ±500 V
- Supply voltage range: 4.5 V ~ 36 V
- Low supply current:
  -0.95 mA per channel at V_S = 36 V
  -0.75 mA per channel at V_S = 4.5 V
- Input voltage range: -0.1 V ~ (+V_S - 1.5 V)
- Low offset voltage: 3.5 mV (max)
- Rail-to-rail output: -V_S ~ +V_S
- 3.5 MHz high gain-bandwidth product
- High slew rate: 2.5 V/μs
- Settling time to 0.1% with 2 V step: 0.9 μs
- Package: SOIC-8

Applications

- Automotive lighting
- Body electronics
- Automotive head unit
- Telematics control unit
- Emergency call (eCall)
- Passive safety: brake system

Ordering Information

Part Number	Top Marking	RoHS	T_A	Package	
DIA2602SO8	DIA62AH	Green	-40 to 125°C	SOIC-8	Tape & Reel, 2500

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

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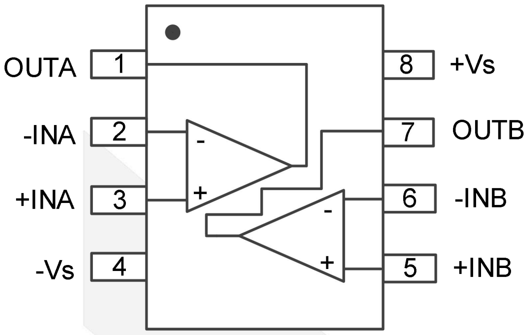


SOIC-8
Top view

Pin No.	Pin name	Description
8	+V_S	Positive supply
4	-V_S	Negative supply
3, 5	+IN (+INA/+INB)	Positive input (channel A/B)
2, 6	-IN (-INA/-INB)	Negative input (channel A/B)
1, 7	OUT (OUTA/OUTB)	Output (channel A/B)

2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
V_S	Supply voltage	40	V
V_{IN}	Input voltage	(-V_S - 0.3) to (+V_S + 0.3)	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Julction temperature	150	°C
T_L	Lead temperature range	260	°C

3. Recommended Operating Condition

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Rating	Unit
V_S	Supply voltage	4.5 to 36	V
V_{IN}	Input voltage	-0.1 to (+V_S - 1.5 V)	V
T_A	Operating temperature range	-40 to 125	°C

4. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Condition	Value	Unit
HBM	AEC Q100-002	±2000	V
CDM	AEC Q100-011	±500	V

5. Electrical Characteristics

Typical value: T_A = 25°C, $+V_S$ = 30 V, $-V_S$ = 0 V, R_L = 10 kΩ, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power supply						
V_S	Supply voltage range		4.5		36	V
PSRR	Power supply rejection ratio			120		dB
I_Q	Supply current per channel/amplifier	V_S = 4.5 V		0.75		mA
		V_S = 36 V		0.95		mA
Input characteristics						
V_{OS}	Input offset voltage	$V_{CM} = +V_S/2$, T_A = 25°C	-3.5		3.5	mV
V_{CM}	Common mode voltage range		-0.1		$+V_S$ - 1.5	V
CMRR	Common mode rejection ratio	-40°C ≤ T_A ≤ 125°C, $+V_S$ = 36 V, V_{CM} = 0.5 V to 28 V		90		dB
A_{OL}(1)	Open loop voltage gain			155		dB
V_O	Output swing high from supply rail	R_L = 50 kΩ, rising		20		mV
	Output swing low from supply rail	R_L = 50 kΩ, falling		15		mV
$\Delta V_{OS}/\Delta T$	Input offset voltage drift	-40°C ≤ T_A ≤ 125°C		5		μV/°C
Output characteristics						
I_{SC}	Output short-circuit current	Sink current		14		mA
		Source current		14		mA
Dynamic performance						
GBP	Gain bandwidth product	f = 1 kHz		3.5		MHz
SR	Slew rate	A_V = 1, 10 V step		2.5		V/μs
t_S	Settling time	A_V = -1, 2 V step, 0.1%		0.9		μs
		A_V = -1, 2 V step, 0.01%		1.2		μs
t_{OR}	Positive overload recovery time			1.4		μs
	Negative overload recovery time			1		μs
Noise performance						
THD+N	Total harmonic distortion and noise	f = 1 kHz, A_V = 1 V, R_L = 2 kΩ, V_{OUT} = 3.5 V_{RMS}		0.0005		%
e_n	Input voltage noise density	f = 1 kHz		32		nV/√Hz
V_n	Input voltage noise	f = 0.1 Hz to 10 Hz		2.35		μV_{RMS}
X_{talk}	Channel separation	f = 1 kHz, R_L = 1 kΩ		-100		dB

Note:

(1) Guaranteed by design.

(2) Specifications subject to change without notice.

6. Typical Performance Characteristics

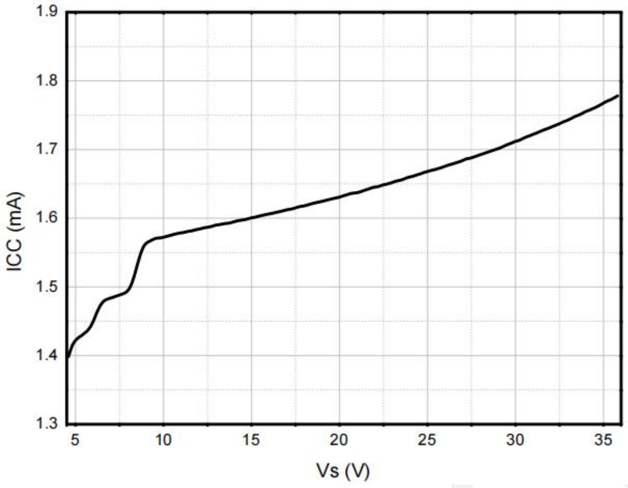


Figure 1. Quiescent current vs. Supply voltage

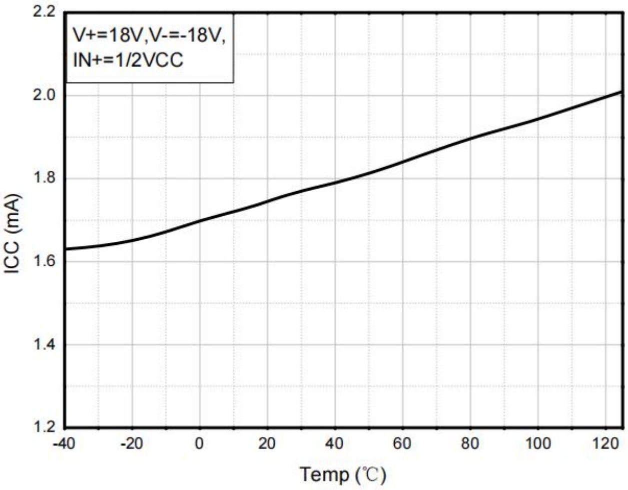


Figure 2. Quiescent current vs. Temperature

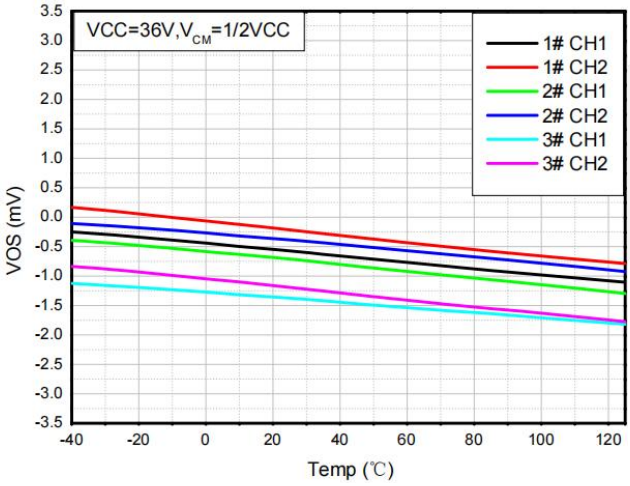


Figure 3. VOS vs. Temperature

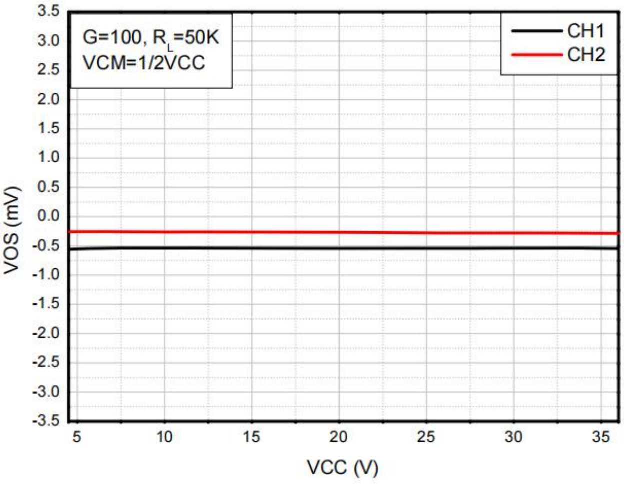
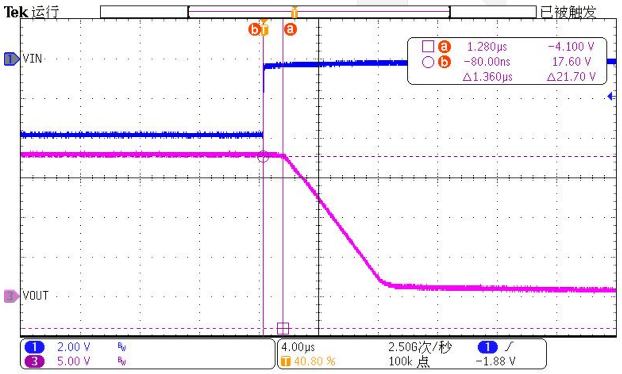


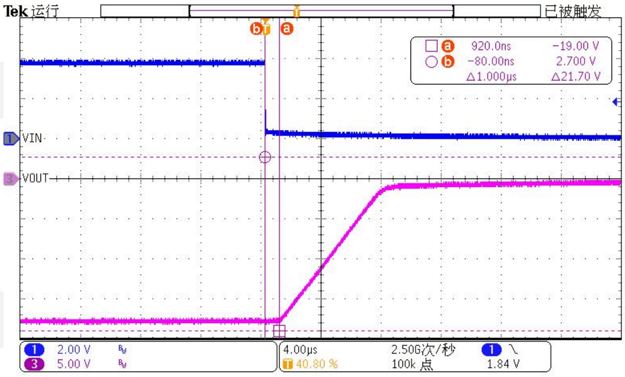
Figure 4. V_{OC} vs. V_{CC}



+V_S = 18 V, V- = -18 V, G = 10, R_L = 2 kΩ, C_L = 100 pF,

V_{IN} = 3.8 Vpp at 1.9 V

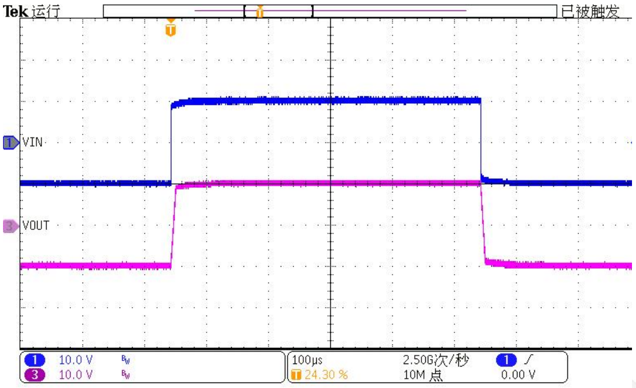
Figure 5. Positive overload recovery



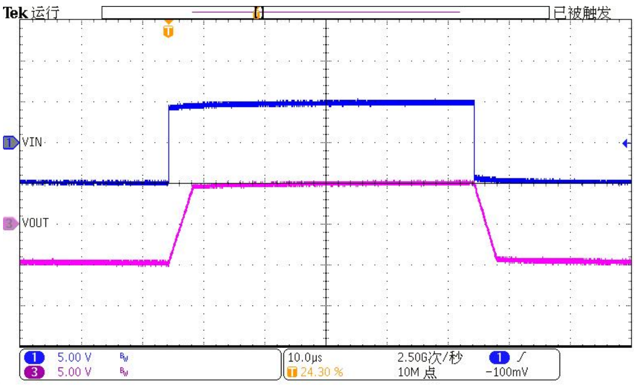
+V_S = 18 V, V- = -18 V, G = 10, R_L = 2 kΩ, C_L = 100 pF,

V_{IN} = 3.8 Vpp at -1.9 V

Figure 6. Negative overload recovery



+V



$+V_S$ = 18 V, $-V_S$ = -18 V,G = 1, R_L = 2 kΩ, C_L = 100 pF

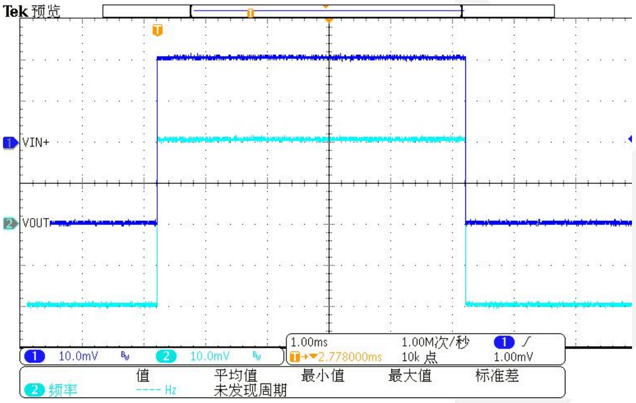
V_{IN} = 10 Vpp at 1 kHz, 0 V bias

Figure 7. Signal step response

$+V_S$ = 18 V, $-V_S$ = -18 V,G = 1, R_L = 2 kΩ, C_L = 100 pF

V_{IN} = 10 Vpp at 10 kHz, 0 V bias

Figure 8. Signal step response



$+V_S$ = 18 V, $-V_S$ = -18 V, G = 1, C_L = 100 pF, R_L = 2 kΩ to GND,

40 mVpp at 0 V bias, 100 Hz

Figure 9. Small-signal response

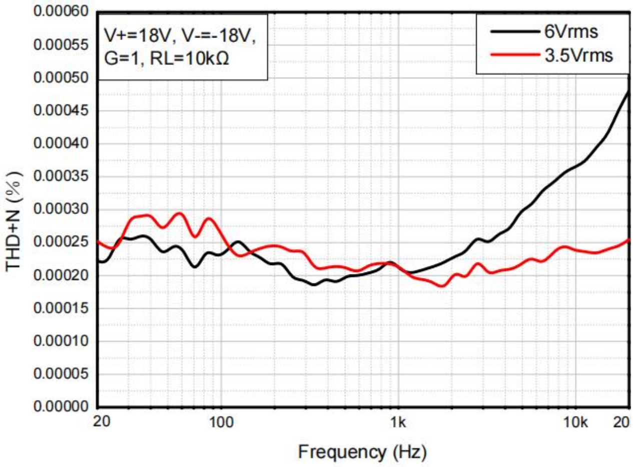


Figure 10. THD+N vs. Frequency

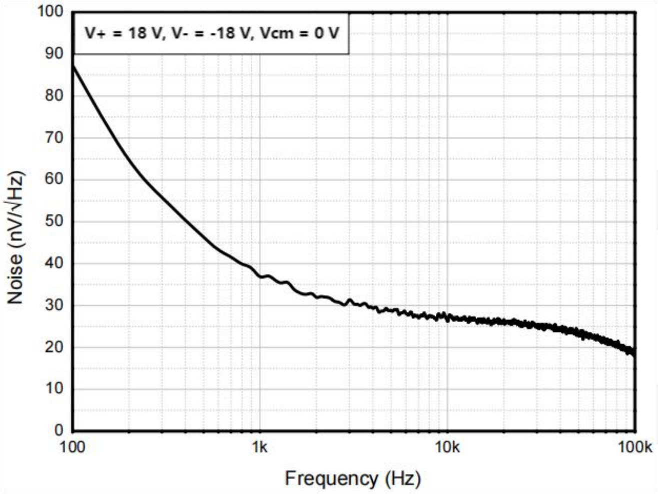


Figure 11. Voltage noise spectral density vs. Frequency

7. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purposes only.

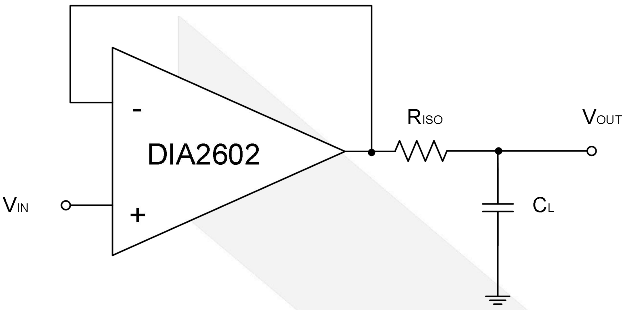


Figure 12. Indirectly driving heavy capacitive load

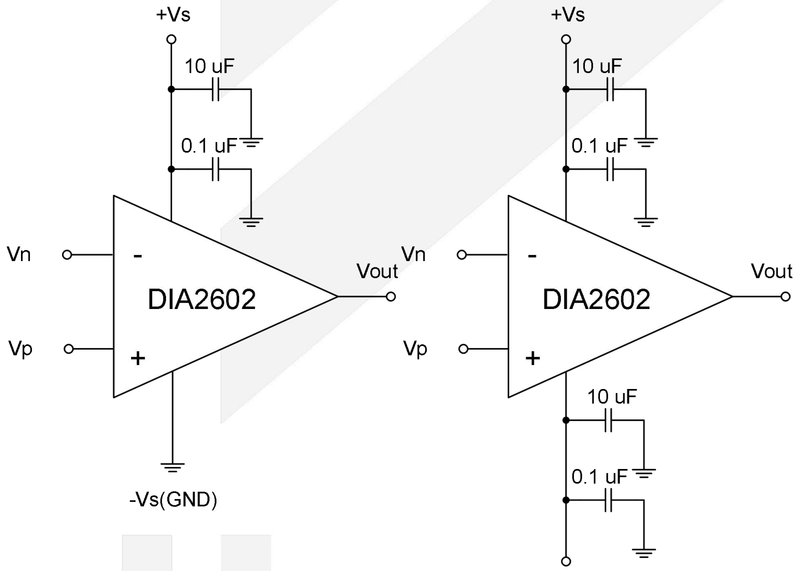


Figure 13. Indirectly driving heavy capacitive load with DC accuracy

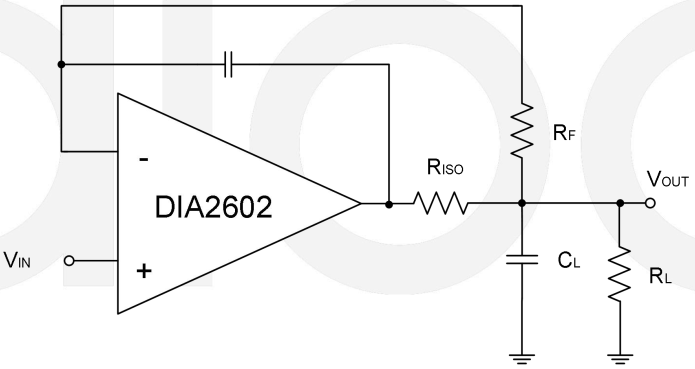
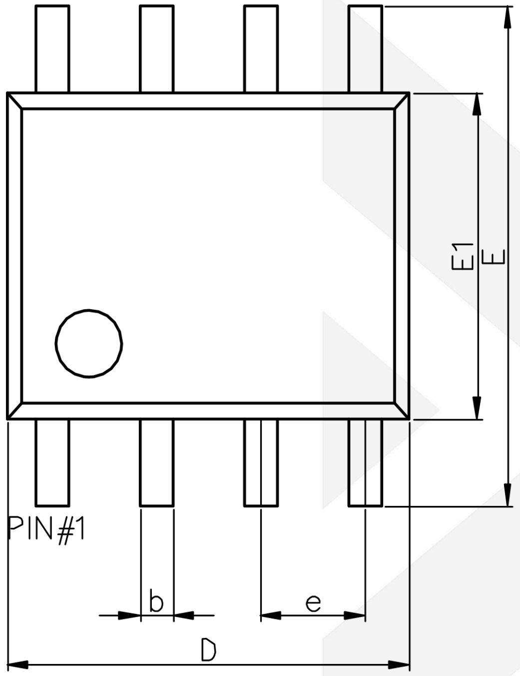
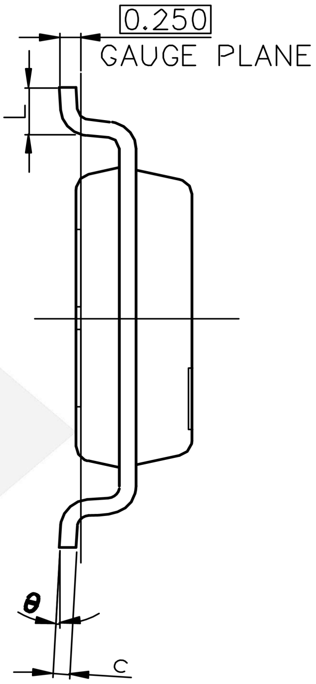
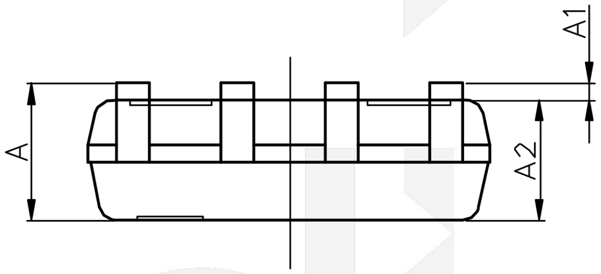


Figure 14. Amplifier with bypass capacitors

8. Physical Dimensions: SOIC-8







Common Dimensions Units of measure = Millimeter		
Symbol	**Min**	**Max**
A	1.450	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
E	5.800	6.200
E1	3.800	4.000
e	1.270 BSC	
L	0.400	1.270
θ	0°	8°

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