

DIO3402

Dual SPDT Switch with 20V Overvoltage Protection

Features

- Operating Voltage Range: 2.3V to 5.5V
- Differential 2:1 or 1:2 Switch/Multiplexer or Flexible Dual Single Ended Cross Switch
- V_{CC}=0V Powered Off Protection
- Low R_{ON}: 5.2Ω
- BW: 1.5GHz
- Overvoltage Protection (OVP) on Common Pins up to 20V DC
- Surge Protection Up to 35V
- ESD (HBM): 4kV
- Temperature Range of -40°C to 85°C
- WLCSP-12 Package

Descriptions

The DIO3402 is a high-speed USB2.0 low-power dual SPDT, analog switch with overvoltage protection. The device is configured as a dual 2:1 or 1:2 switch and is optimized for handling the USB2.0 D+/- lines in a USB Type-C system.

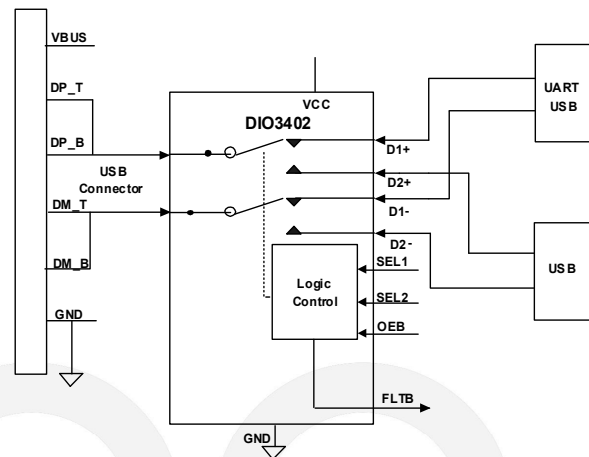
The DIO3402 protects the system components behind the switch with over voltage fault protection up to 20V.

The DIO3402 is available in a small WLCSP-12 package, which making it a perfect solution for mobile applications.

Applications

- Mobile
- PC/Notebook
- Tablet
- USB Type-C

Simplified Schematic



Ordering Information

Order Part Number	Top Marking		T _A	Package	
DIO3402WL12	3402	Green	-40 to 85°C	WLCSP-12	Tape & Reel, 3000

Pin Assignments

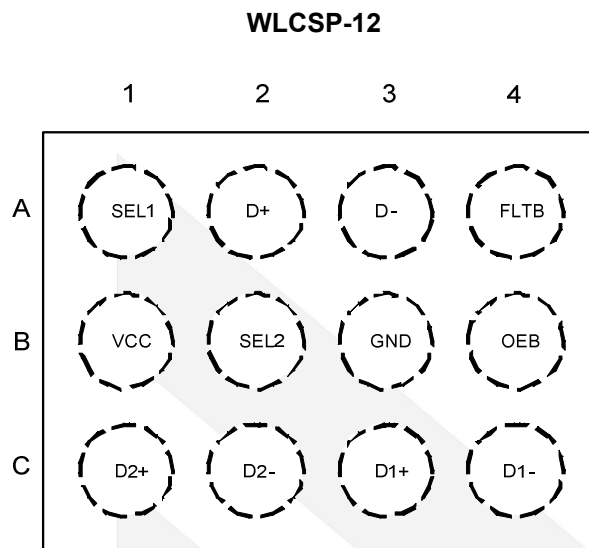


Figure 1 Top View

Pin Description

Name	Bump	Type	Description
SEL1	A1	I	Switch select1 (Active high)
D+	A2	I/O	Data switch input (Differential+)
D-	A3	I/O	Data switch input (Differential-)
FLT B	A4	O	Fault indicator output pin (Active low)-open drain
VCC	B1	PWR	Supply Voltage
SEL2	B2	I	Switch select2 (Active high)
GND	B3	GND	Ground
OEB	B4	I	Output enable (Active low)
D2+	C1	I/O	Data switch output 2 (Differential+)
D2-	C2	I/O	Data switch output 2 (Differential-)
D1+	C3	I/O	Data switch output 1 (Differential+)
D1-	C4	I/O	Data switch output 1 (Differential-)



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Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage ⁽¹⁾	-0.5	6	V
V _{I/O}	Input /Output DC Voltage (D+,D-) ⁽¹⁾	-0.5	28	V
V _{I/O}	Input /Output DC Voltage (D1+/D1-, D2+/D2-) ⁽¹⁾	-0.5	6	V
V _I	Digital Input Voltage (SEL1, SEL2, OEB)	-0.5	6	V
V _O	Digital Output Voltage (FLT B)	-0.5	6	V
I _K	Input-Output Port Diode Current (D+, D-, D1+, D1-, D2+, D2-) (V _{IN} <0)	-50		mA
I _{IK}	Digital Logic Input Clamp Current (SEL1, SEL2, OEB) ⁽¹⁾ (V _I <0)	-50		mA
I _{CC}	Continuous Current Through VCC		100	mA
I _{GND}	Continuous Current Through GND	-100		mA
T _{stg}	Storage Temperature	-65	150	°C
ESD	Human body model (HBM)	-4000	4000	V

(1) All voltages are with respect to ground, unless otherwise specified.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Rating	Unit
V _{CC}	Supply Voltage	2.3 ~ 5.5	V
V _{I/O (D+, D-)}	Analog Input /Output Voltage	0 ~ 20	V
V _{I/O (D1+, D1-, D2+, D2-)}		0 ~ 3.6	V
V _I	Digital Input Voltage (SEL1, SEL2, OEB)	0 ~ 5.5	V
V _O	Digital Output Voltage (FLT B)	0 ~ 5.5	V
I _{I/O (D+,D-,D1+,D1-,D2+,D2-)}	Analog Input /Output Port Continuous Current	-50 ~ 50	mA
I _{OL}	Digital Output Current	3	mA
T _A	Operating Free-Air Temperature	-40 ~ 85	°C
T _J	Junction Temperature	-40 ~ 125	°C



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Electrical Characteristics

$T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 2.3\text{V}$ to 5.5V , $\text{GND} = 0\text{V}$, Typical values are at $V_{CC} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$, (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY						
V_{CC}	Power Supply Voltage		2.3		5.5	V
I_{CC}	Active Supply Current	OEB=0V, SEL1, SEL2=0V, 1.8V or V_{CC} $V_{CC} \leq 4.4\text{V}$, $T_A = 25^{\circ}\text{C}$ to 65°C $0\text{V} < V_{I/O} < 3.6\text{V}$		25	40	μA
	Supply Current During OVP Condition	OEB=0V, SEL1, SEL2=0V, 1.8V or V_{CC} $V_{CC} \leq 4.4\text{V}$, $T_A = 25^{\circ}\text{C}$ to 65°C $V_{I/O} > V_{POS_THLD}$		25	40	μA
I_{CC_PD}	Standby Powered Down Supply Current	OEB=1.8V or V_{CC} , SEL1=0V, 1.8V, or V_{CC} SEL2=0V, 1.8V, or V_{CC}		1.5	10	μA
DC Characteristics						
R_{ON}	ON-State Resistance	$V_{I/O} = 0.4\text{V}$, $I_{SINK} = 8\text{mA}$ Refer to ON-State Resistance Figure		5.2	9	Ω
ΔR_{ON}	ON-State Resistance Match Between Channels	$V_{I/O} = 0.4\text{V}$, $I_{SINK} = 8\text{mA}$ Refer to ON-State Resistance Figure			0.3	Ω
$R_{ON(FLAT)}$	ON-State Resistance Match Flatness	$V_{I/O} = 0\text{V}$ to 0.4V , $I_{SINK} = 8\text{mA}$ Refer to ON-State Resistance Figure		0.1	0.4	Ω
I_{OFF}	I/O Pin OFF Leakage Current	$V_{D\pm} = 0\text{V}$ or 3.6V , $V_{CC} = 2.3\text{V}$ to 5.5V $V_{D1\pm}$ or $V_{D2\pm} = 3.6\text{V}$ or 0V , Refer to OFF Leakage Figure	-1	1	6	μA
		$V_{D\pm} = 0\text{V}$ or 20V , $V_{CC} = 2.3\text{V}$ to 5.5V $V_{D1\pm}$ or $V_{D2\pm} = 0\text{V}$, Refer to OFF Leakage Figure	-1	160	200	μA
I_{ON}	ON Leakage Current	$V_{D\pm} = 0\text{V}$ or 3.6V , $V_{D1\pm}$ and $V_{D2\pm} = \text{High-Z}$ Refer to ON Leakage Figure	-1	1	6	μA
Digital Characteristics						
V_{IH}	Input Logic High	SEL1, SEL2, OEB	1.4			V
V_{IL}	Input Logic Low	SEL1, SEL2, OEB			0.5	V
V_{OL}	Output Logic Low	FLTB, $I_{OL} = 3\text{mA}$			0.4	V
I_{IH}	Input High Leakage Current	SEL1, SEL2, OEB=1.8V, V_{CC}	-1	0.5	5	μA



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I_{IL}	Input Low Leakage Current	SEL1, SEL2, OEB=0V	-1	0	5	μA
R_{PD}	Internal Pull-Down Resistor On Digital Input Pins			6		$M\Omega$
C_i	Digital Input Capacitance	SEL1, SEL2=0V, 1.8V or VCC, f=1MHz		3.3		pF
Protection						
V_{OVP_TH}	OVP Positive Threshold		4.5	4.85	5.2	V
V_{OVP_HYST}	OVP Threshold Hysteresis		80	260	400	mV
V_{CLAMP_V}	Maximum Voltage To Appear On D1 \pm And D2 \pm Pins During OVP Scenario	$V_{D\pm}=0$ to 18V t_{RISE} and $t_{FALL}(10\% \text{ to } 90\%)=100ns$ $R_L=Open$, Switch ON or OFF OEB=0V	0		8.5	V
		$V_{D\pm}=0$ to 18V t_{RISE} and $t_{FALL}(10\% \text{ to } 90\%)=100ns$ $R_L=50\Omega$, Switch ON or OFF OEB=0V	0		7.0	V
t_{EN_OVP}	OVP Enable Time	$R_{PU}=10k\Omega$ to VCC(FLTB) $C_L=35pF$ Refer to OVP Timing Diagram Figure		0.5	3	μs
t_{REC_OVP}	OVP Recovery Time	$R_{PU}=10k\Omega$ to VCC(FLTB) $C_L=35pF$ Refer to OVP Timing Diagram Figure		1.5	5	μs





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Dynamic Characteristics

$T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 2.3\text{V}$ to 5.5V , $\text{GND} = 0\text{V}$, Typical values are at $V_{CC} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$, (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
C_{OFF}	D+, D- OFF Capacitance	$V_{D+/-} = 0$ or 3.3V , $\text{OEB} = V_{CC}$ $f = 240\text{MHz}$, Switch OFF		3.3		pF
	D1+, D1-, D2+, D2- OFF Capacitance	$V_{D+/-} = 0$ or 3.3V , $\text{OEB} = V_{CC}$ or $\text{OEB} = 0\text{V}$ with SEL1, SEL2 (switch not selected) $f = 240\text{MHz}$ Switch OFF or not selected		3.3		pF
C_{ON}	IO Pins ON Capacitance	$V_{D+/-} = 0$ or 3.3V , $f = 240\text{MHz}$ Switch ON		4.3		pF
O_{ISO}	Differential OFF Isolation	$R_L = 50\Omega$, $C_L = 5\text{pF}$, $f = 100\text{kHz}$ Refer to OFF Isolation Figure Switch OFF		-100		dB
		$R_L = 50\Omega$, $C_L = 5\text{pF}$, $f = 240\text{MHz}$ Refer to OFF Isolation Figure Switch OFF		-30		dB
X_{TALK}	Channel To Channel Crosstalk	$R_L = 50\Omega$, $C_L = 5\text{pF}$, $f = 100\text{kHz}$ Refer to Crosstalk Figure Switch ON		-90		dB
BW	Bandwidth	$R_L = 50\Omega$ Refer to BW and Insertion Loss Figure Switch ON		1.5		GHz
I_{LOSS}	Insertion Loss	$R_L = 50\Omega$, $f = 240\text{MHz}$ Refer to BW and Insertion Loss Figure Switch ON		-0.7		dB

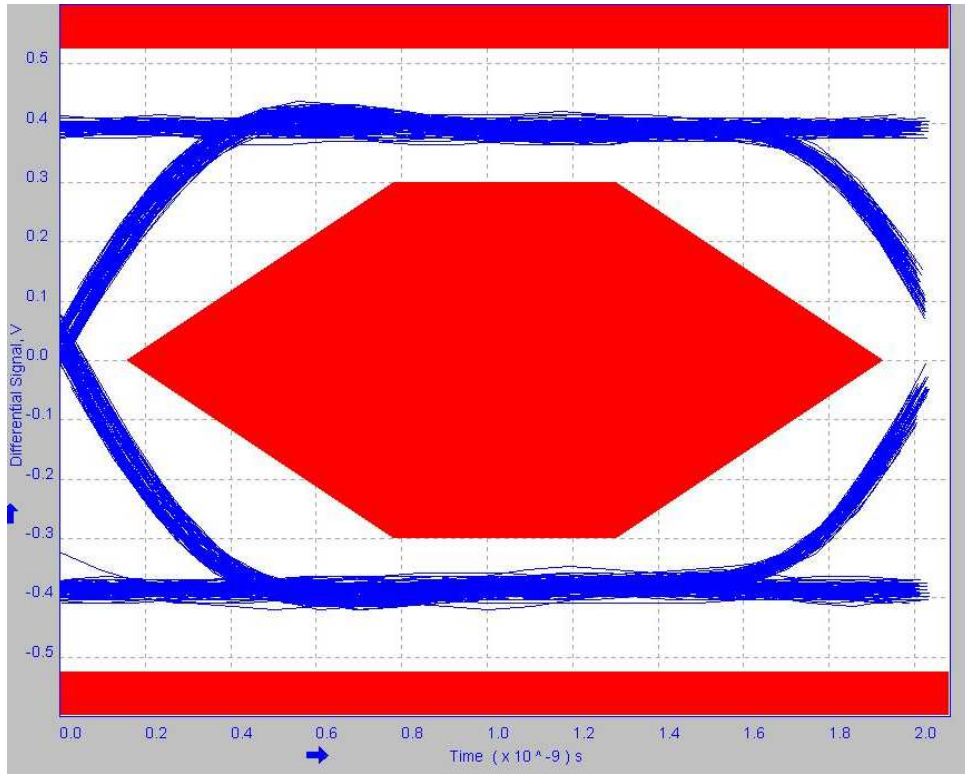
Timing Requirements

$T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 2.3\text{V}$ to 5.5V , $\text{GND} = 0\text{V}$, Typical values are at $V_{CC} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$, (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Nom	Max	Unit
t_{switch}	Switching Time Between Channels (SEL1, SEL2 To Output)	$V_{D+/-} = 0.8\text{V}$ Refer to t_{switch} Timing Figure		0.6		μs
t_{ON}	Device Turn ON Time (OEB To Output)	$V_{D+/-} = 0.8\text{V}$ Refer to T_{ON} and T_{OFF} Figure		80		μs
t_{OFF}	Device Turn OFF Time (OEB To Output)	$V_{D+/-} = 0.8\text{V}$ Refer to T_{ON} and T_{OFF} Figure		0.1		μs

Typical Performance Characteristics

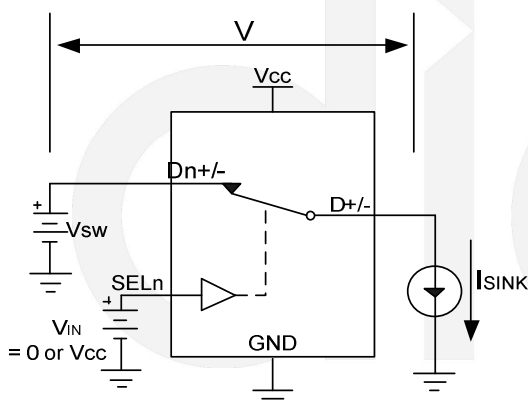
DIO3402 USB 2.0 high speed (480Mbps) eye pattern



TIME SCALE (0.2ns/DIV)

Figure 2 Eye Pattern: 480Mbps with USB switch In signal path

Application Information



Channel ON, $R_{ON} = V / I_{SINK}$

Figure 3 ON-State Resistance (R_{ON})

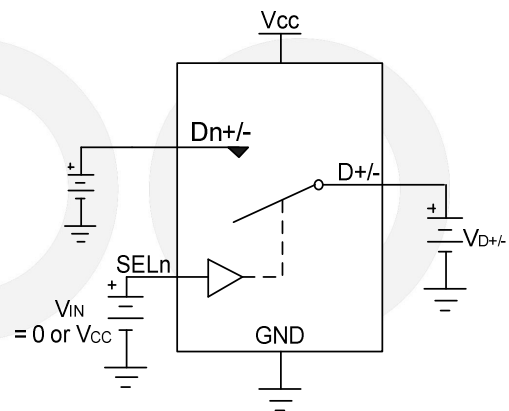


Figure 4 OFF Leakage

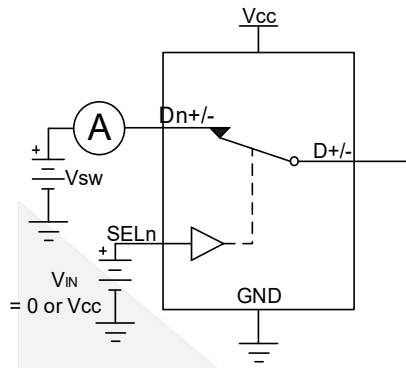
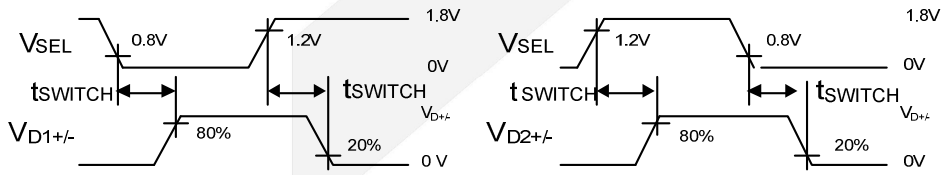
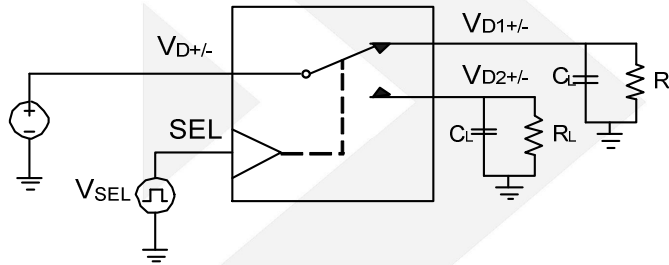
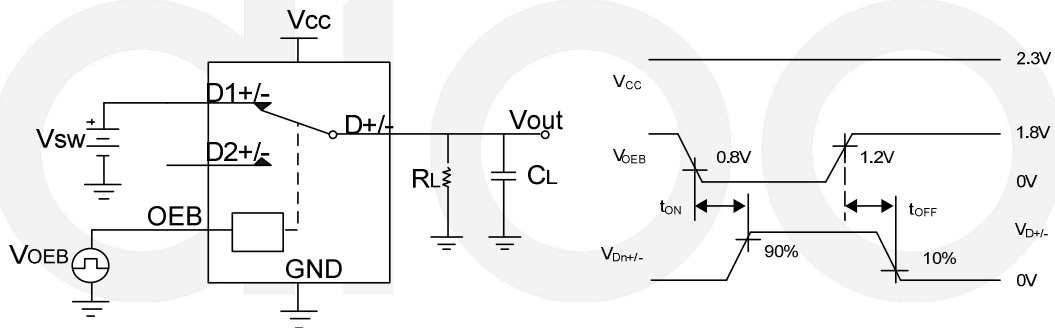


Figure 5 ON Leakage



- (1) All input pulses are supplied by generators having the following characteristics: PRR≤10MHz, Z_O=50Ω, t_r<500ps, t_f<500ps.
- (2) C_L includes probe and jig capacitance.

Figure 6 tsWITCH Timing



- (1) All input pulses are supplied by generators having the following characteristics: PRR≤10MHz, Z_O=50Ω, t_r<500ps, t_f<500ps.
- (2) C_L includes probe and jig capacitance.

Figure 7 t_{ON}, t_{OFF} for OEB

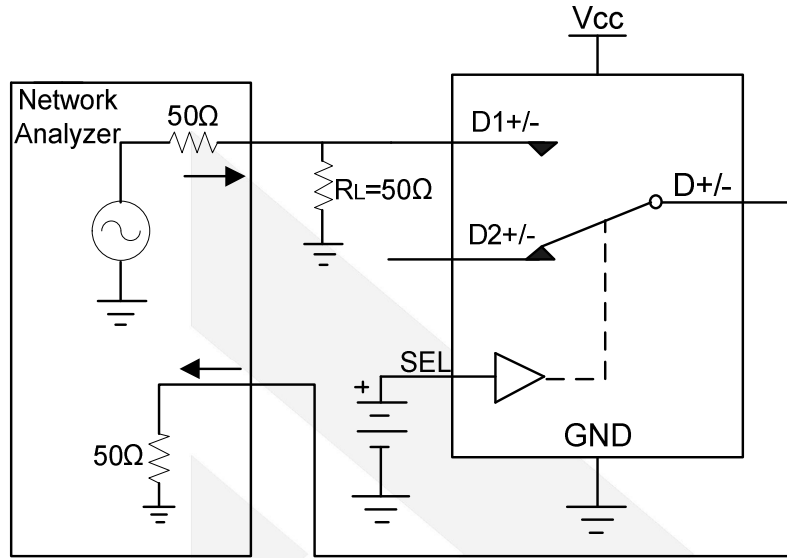


Figure 8 OFF Isolation

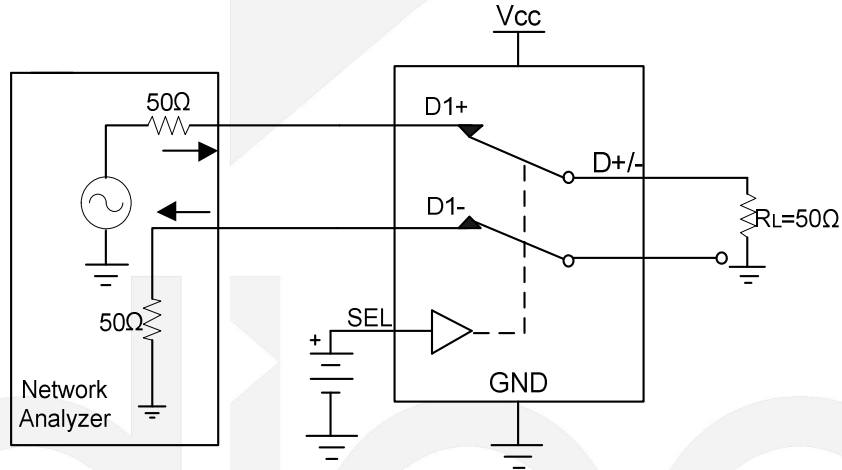


Figure 9 Cross Talk

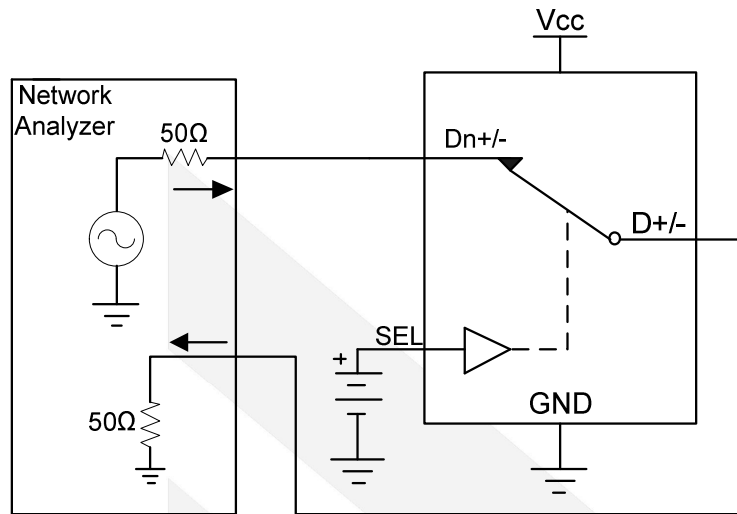


Figure 10 BW and Insertion Loss

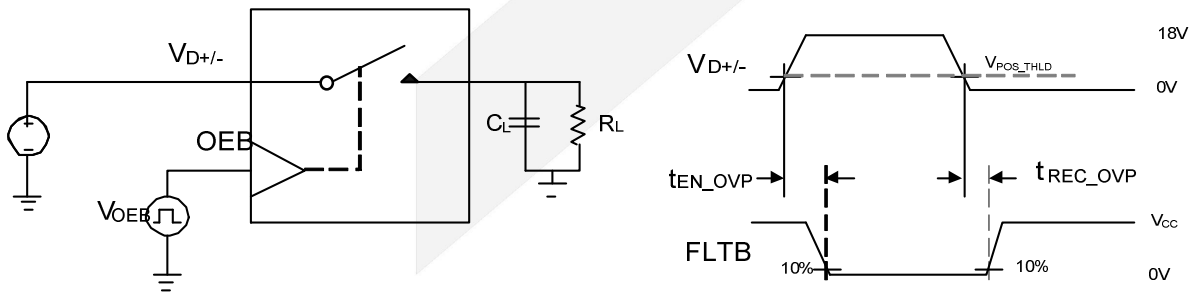


Figure 11 t_{EN_OVP} and t_{DIS_OVP} Timing Diagram

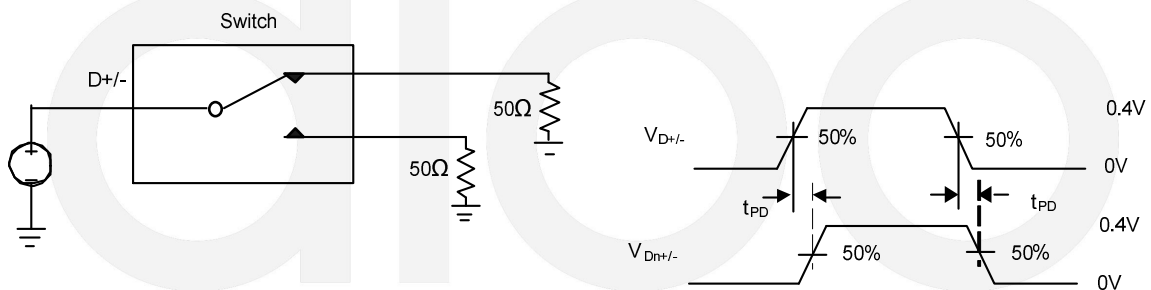
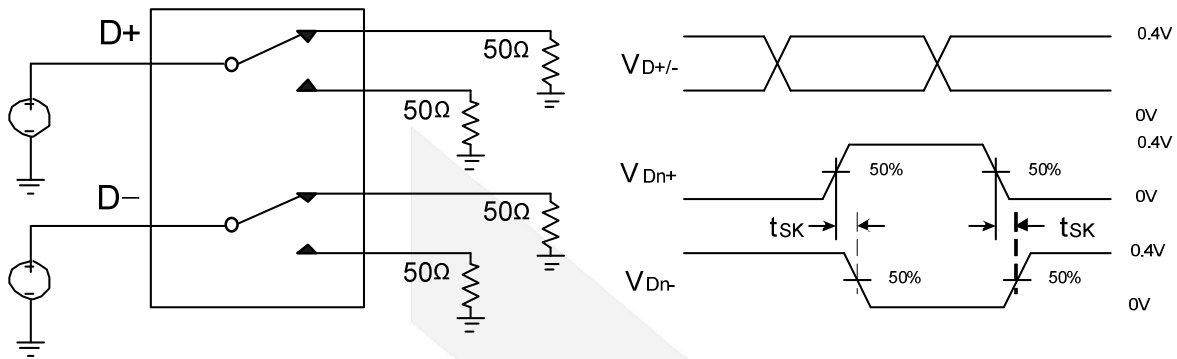


Figure 12 t_{PD}

- (1) All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{MHz}$, $Z_0 = 50\Omega$, $t_r < 500\text{ps}$, $t_f < 500\text{ps}$.
- (2) C_L includes probe and jig capacitance.



- (1) All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{MHz}$, $Z_o = 50\Omega$, $t_r < 500\text{ps}$, $t_f < 500\text{ps}$.
- (2) C_L includes probe and jig capacitance.

Figure 13 t_{sk}

Detailed Description

Overview

The DIO3402 is a bidirectional USB2.0 high speed (480Mbps) switch, designed to fully protect the USB Type-C data ports (D+ and D- differential data lines). The device can function as either two channel 2:1 multiplexer or 1:2 de-multiplexer. Meanwhile DIO3402 can also be used in typical type C USB 2.0 data ports sharing as shown in Figure 14.

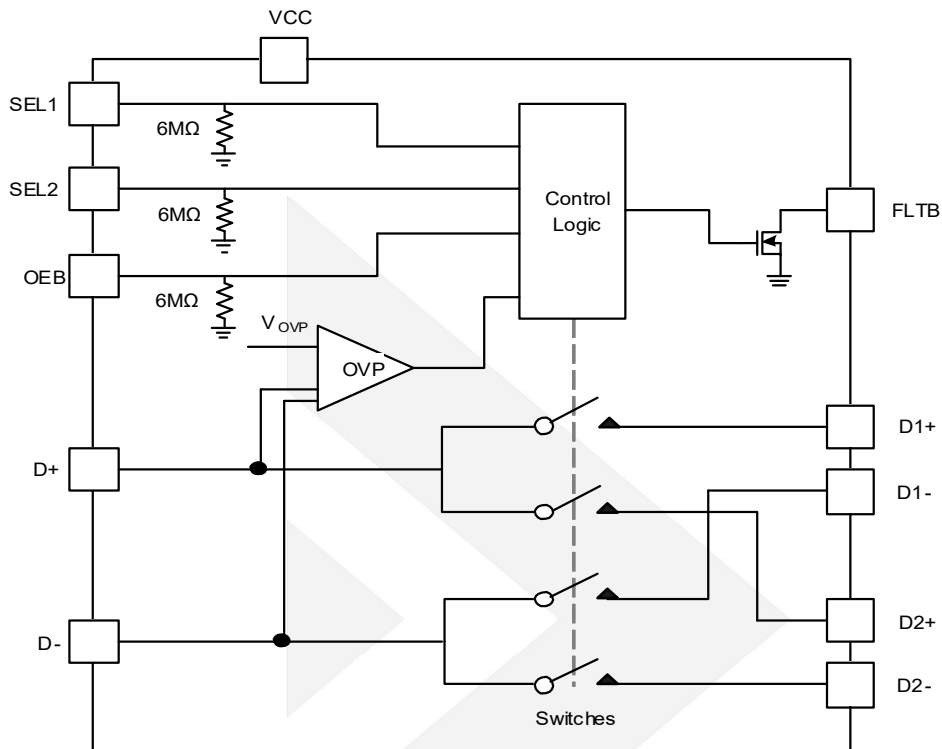
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	+V	CC1	D+	D-	SBU1	+V	RX2-	RX2+	GND
GND	RX1+	RX1-	+V	SBU2	D-	D+	CC2	+V	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

- USB3.1 Super speed+ 10Gbps
- Secondary Bus
- USB2.0 High speed 480Mbps
- USB Power Delivery Communication

Figure 14 Typical USB Type-C Connector Pinout

Secondly, The DIO3402 can also be adopted in such applications where the USB data ports has potential short to Vbus with relatively higher charging voltage. In such scenario, DIO3402 maintains excellent signal integrity and reliability via the internal OVP protection module (tolerate up to and even more than 20V DC) and up to 1.5GHz bandwidth data path.

Functional Block Diagram



Details of Features

Powered-off Protection

When powered down, the inputs and outputs are isolated, and the device outputs remain high impedance. The crosstalk, off-isolation, and leakage performance are remained.

OVP (Overvoltage Protection)

The OVP function of the DIO3402 is designed to isolate the non-common ports from the potential shorts of common port D+/- lines to VBUS at the USB connector. Figure 15 illustrate the potential scenarios that a high voltage event (>20V) could pass through the existing solutions without OVP functions and cause the damages of components behind the device along the signal path.

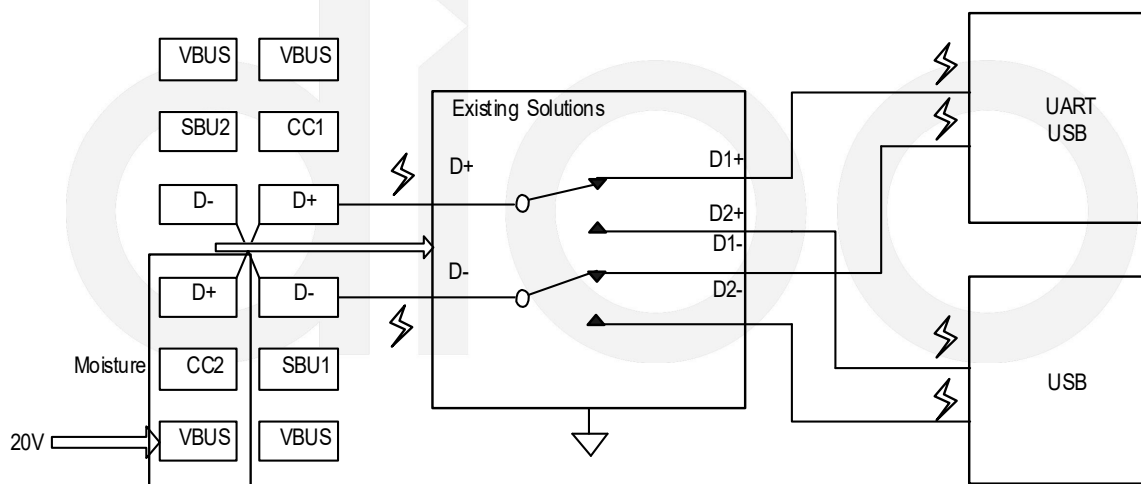


Figure 15 Existing Solution without OVP being Damaged by a Possible Short from Moisture

By comparison, the DIO3402 will immediately turn OFF the internal switches and isolate the rest of data path at lower voltage side (D1+/- and D2+/-) from the high voltage surge of more than 20V appearing at common ports side (D+/-). Refer to Figure 16 for details.

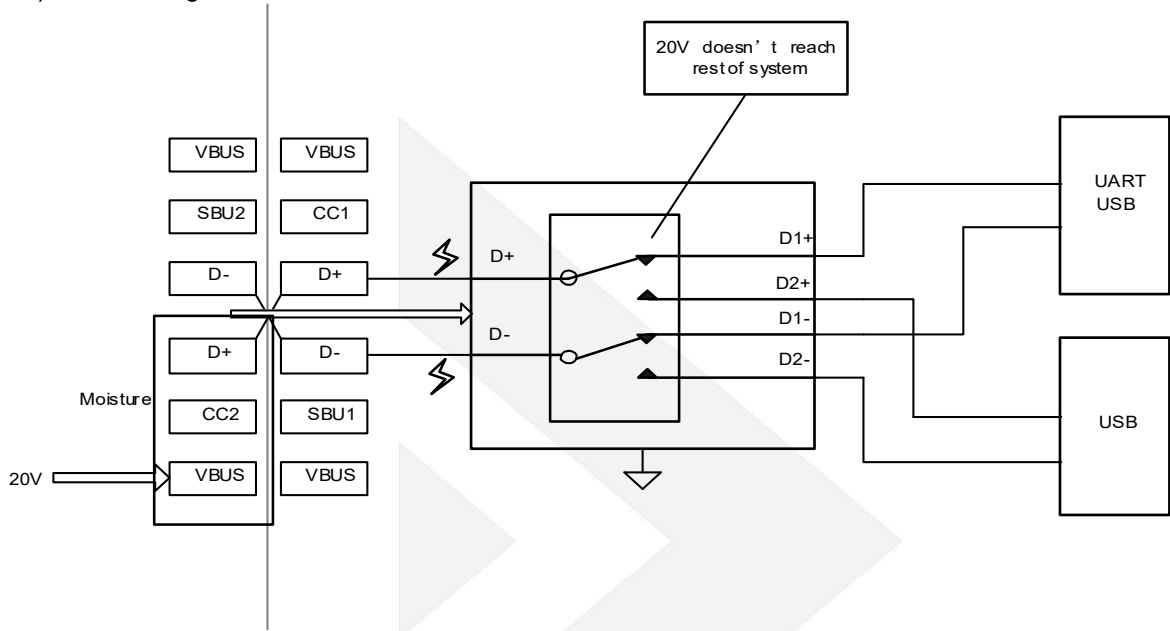


Figure 16 High Voltage Blocking During a 20V Short

Figure 17 is the signal waveform showing the voltage changes on the I/O pins during an over-voltage scenario.

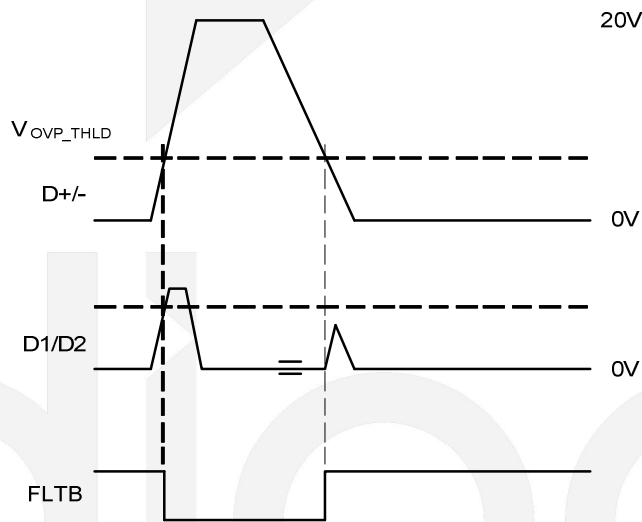


Figure 17 Overvoltage Protection Waveform, 20V



DIO3402

Dual SPDT Switch with 20V Overvoltage Protection

Device Functional Modes

Pin Functions

Table 1. Function Table

OEB	SEL1	SEL2	D- Connection	D+ Connection
H	X	X	High-Z	High-Z
L	L	L	D- to D1-	D+ to D1+
L	L	H	D- to D1-	D+ to D2+
L	H	L	D- to D2-	D+ to D1+
L	H	H	D- to D2-	D+ to D2+



Application and Implementation

Application Information

There are many USB designs in which the USB hubs or controllers have a limited number of USB I/Os or sharing the USB connector. The DIO3402 can effectively expand the limited USB I/Os by multiplexing or de-multiplexing between multiple USB data lines to interface them to a single USB hub or controller or route signals from on connector to two different USB controllers. With the independent control of the two switches (via SEL1 and SEL2), DIO3402 can be used to cross switch single-ended signals in non-USB applications.

Typical Application

Figure 18 is the block diagram illustrating the DIO3402 as USB/UART switch. The DIO3402 is used to switch signals between the USB path, which goes to the baseband/application processor, or the UART pins, which goes to debug port. The DIO3402 has integrated the 6MΩ pull-down resistors at SEL1, SEL2, and OEB pins. The pull-down at SEL1 and SEL2 pins ensure the D1+/D1- channel is selected by default. The pull-down on OEB enables the switch when power is up.

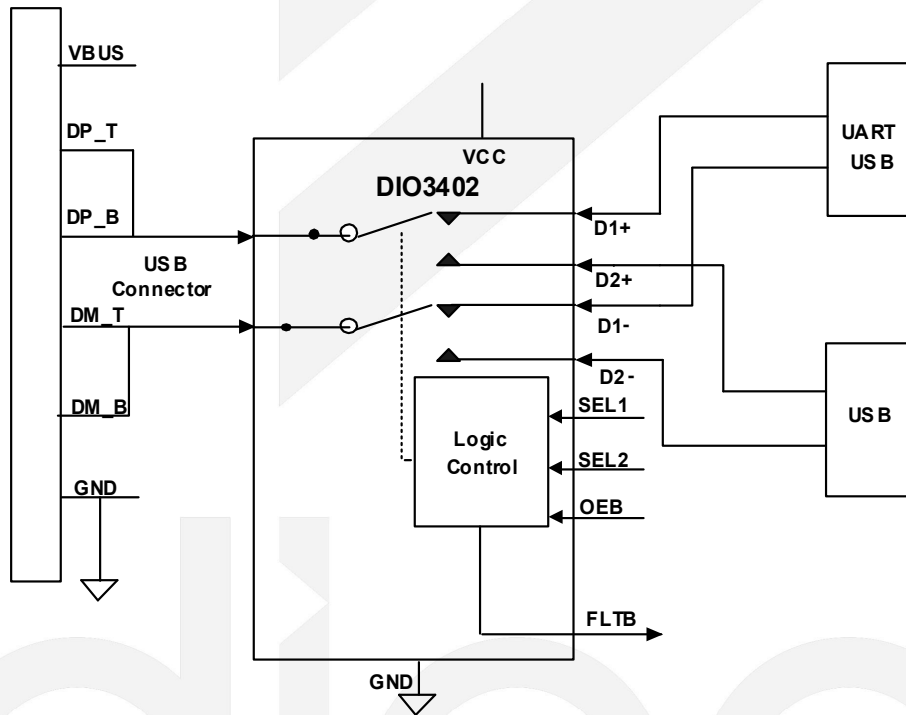


Figure 18 Typical DIO3402 Application

Design Advice

The DIO3402 can function properly without any external components. However, it is highly recommended that unused pins must be connected to ground through a 50Ω resistor to prevent signal reflections back into the device. A 100nF bypass capacitor is recommended to be placed close to DIO3402 VCC pin.



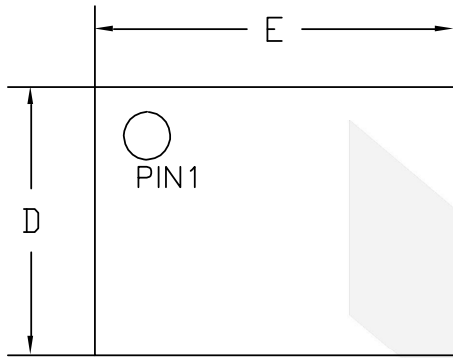
DIO3402

Layout Guidelines

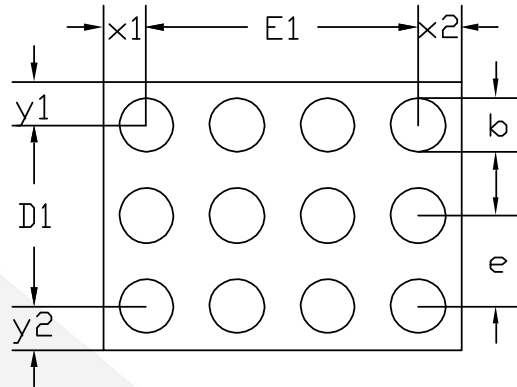
1. Place the bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps close to the D± traces.
2. The high-speed D± must match and less than 4 inches long; otherwise, the eye diagram performance may be degraded. DIO3402 has industrial best eye opening guaranteed by its 1.5GHz bandwidth of data path. In layout, the impedance of D+ and D- traces must match the cable characteristic differential impedance for best signal integrity.
3. Route the high-speed USB signals using a minimum of vias and corners which boost the signal integrity. When the via must be used, increase the clearance size around it to minimize its capacitance which helps the opening of USB eyes. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a sharp single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
5. Do not route USB signals under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
6. Avoid stubs on the high-speed USB signals because they cause signal reflections due to heavy parasitic capacitance. If a stub is unavoidable, then the stub must be less than 200mm.
7. Route all high-speed USB signal traces over continuous GND planes, without interruptions.
8. Meanwhile avoid crossing over anti-etch, commonly found with plane splits.
9. A PCB boards of four layers minimum is recommended for best signal integrity of high speed USB 2.0 (480Mbps) designs.



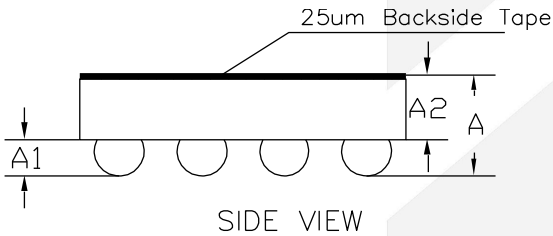
Physical Dimensions: WLCSP-12



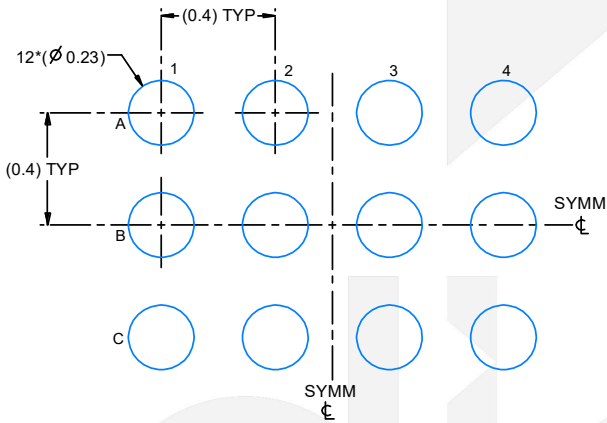
TOP VIEW
(MARK SIDE)



BOTTOM VIEW
(BALL SIDE)



SIDE VIEW



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X

COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)			
Symbol	MIN	NOM	MAX
A	0.420	0.460	0.500
A1	0.157	0.177	0.197
A2	0.263	0.283	0.303
D	1.152	1.182	1.212
D1	0.800BSC		
E	1.552	1.582	1.612
E1	1.200BSC		
b	0.220	0.240	0.260
e	0.400BSC		
x1	0.191REF		
x2	0.191REF		
x3	0.191REF		
x4	0.191REF		



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CONTACT US

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