

DIO6023

High-Efficiency 1MHz, 2.5A continuous, 3A Peak, Synchronous Step Down Converter

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom) 100m Ω /70m Ω , 3A
- 2.7-5.5V input voltage range
- 1MHz switching frequency minimizes the external components
- Internal soft start limits the inrush current
- 100% dropout operation
- RoHS Compliant and Halogen Free
- Compact and thermally enhanced SOT23-6

Applications

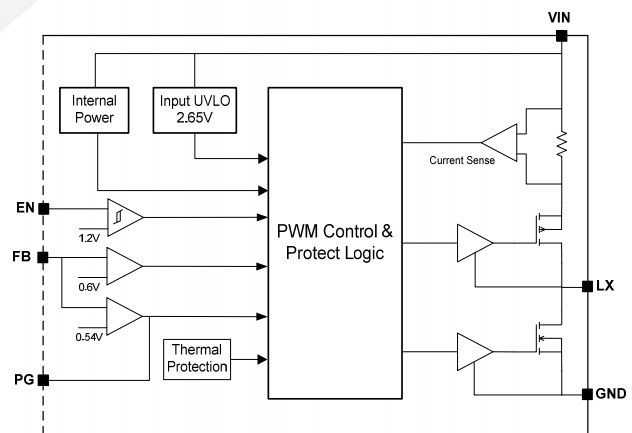
- LCD TV
- Set Top Box
- Net PC
- Mini-Notebook PC
- Access Point Router

Descriptions

The DIO6023 is a high-efficiency 1MHz synchronous step-down DC-DC regulator IC capable of delivering up to 3A output current.

The DIO6023 operates over a wide input voltage ranging from 2.7V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. Low output voltage ripple and small external inductor and capacitor sizes are achieved with 1MHz switching frequency.

Function Block



Ordering Information

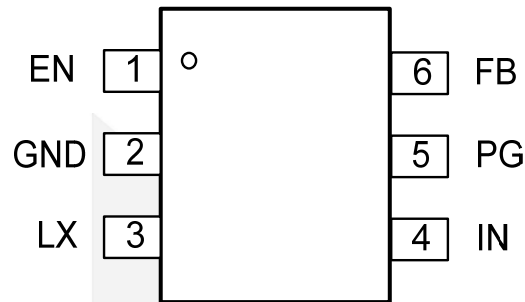
Order Part Number	Top Marking		T_A	Package	
DIO6023CST6	YWXD	RoHS	-40 to +85°C	SOT23-6	Tape & Reel, 3000



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Pin Assignments



SOT23-6

Figure 1 Pin Assignment (Top View)

Pin Definitions

Pin Name	Description
EN	Enable control. Pull high to turn on. Do not float.
GND	Ground
LX	Inductor pin. Connect this pin to the switching node of inductor.
IN	Power Input
PG	Power good indicator. When the output voltage exceeds 90% of regulation point, it becomes open drain; low otherwise.
FB	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{out} = 0.6 * (1 + R1/R2)$.



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Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
Supply Voltage (V+ – V-)		6.0	V
Enable, FB Voltage		$V_{IN}+0.6$	V
Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$, SOT23-6		0.6	W
Package Thermal Resistance	θ_{JA}	170	$^\circ\text{C}/\text{W}$
	θ_{JC}	130	
Storage Temperature Range		-65 to 150	$^\circ\text{C}$
Junction Temperature Range		150	$^\circ\text{C}$
Lead Temperature Range		260	$^\circ\text{C}$
ESD	HBM, JEDEC: JESD22-A114	4000	V
	MM, JEDEC: JESD22-A115	200	
Dynamic LX Voltage in 50ns Duration		$V_{IN}+3$ to GND-4	V

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter	Rating	Unit
Supply Voltage	2.7 to 5.5	V
Junction Temperature Range	-40 to 125	$^\circ\text{C}$
Ambient Temperature Range	-40 to 85	$^\circ\text{C}$



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Electrical Characteristics

$V_{IN} = 3.6V$, $V_{OUT} = 2.5V$, $L = 2.2\mu H$, $C_{OUT} = 22\mu F$, $T_A = 25^\circ C$, $I_{MAX} = 1A$ unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		2.7		5.5	V
I_Q	Quiescent Current	$I_{OUT}=0$, $V_{FB}=V_{REF} \cdot 105\%$		80		μA
I_{SHDN}	Shutdown Current	EN=0		0.1	1	μA
V_{REF}	Feedback Reference Voltage		0.588	0.6	0.612	V
I_{FB}	FB Input Current	$V_{FB}=V_{IN}$	-50		50	nA
$R_{DS(ON),P}$	PFET R_{ON}			100		m Ω
$R_{DS(ON),N}$	NFET R_{ON}			70		m Ω
I_{LIM}	PFET Current Limit		4			A
V_{ENH}	EN Rising Threshold		1.2			V
V_{ENL}	EN Falling Threshold				0.4	V
V_{UVLO}	Input UVLO Threshold				2.65	V
V_{HYS}	UVLO Hysteresis			0.2		V
F_{OSC}	Oscillator Frequency	$I_{OUT}=500mA$,		1		MHz
	Min ON Time			50		ns
	Max Duty Cycle		100			%
T_{SD}	Thermal Shutdown Temperature			150		$^\circ C$





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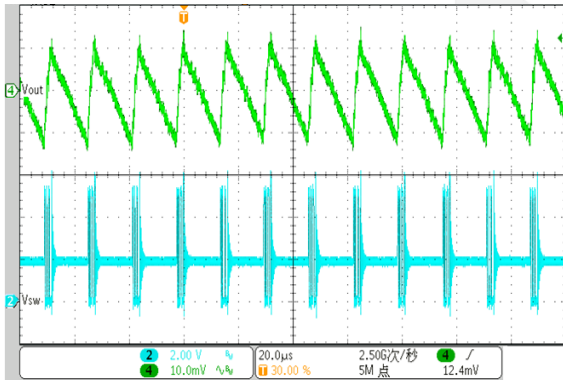
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Typical Performance Characteristics

$V_{IN} = 5V$, $V_{OUT} = 1.8V$, $L = 2.2\mu H$, $C_{OUT} = 22\mu F \times 2$, $T_A = 25^\circ C$, unless otherwise specified.

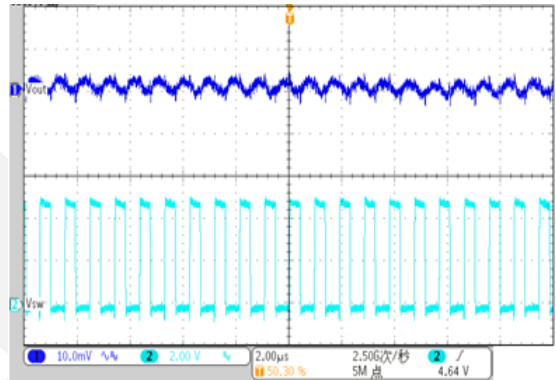
Ripple

($V_{IN}=5V$, $V_{OUT}=1.8V$, $I_{Load}=30mA$, In burst mode)



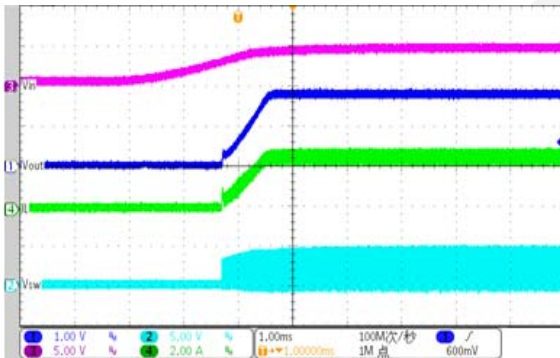
Ripple

($V_{IN}=5V$, $V_{OUT}=1.8V$, $I_{Load}=3A$, In CCM mode)



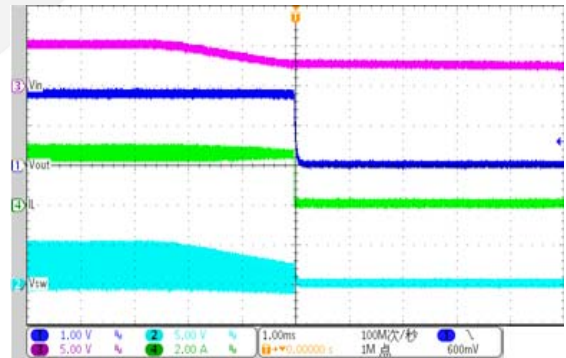
Start up from V_{IN}

($V_{IN}=5V$, $V_{OUT}=1.8V$, $R_{Load}=0.6ohm$)



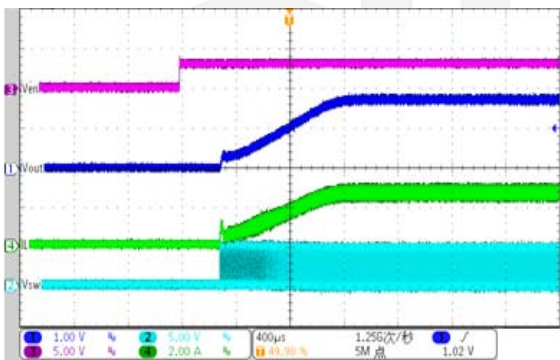
Shut Down from V_{IN}

($V_{IN}=5V$, $V_{OUT}=1.8V$, $R_{Load}=0.6ohm$)



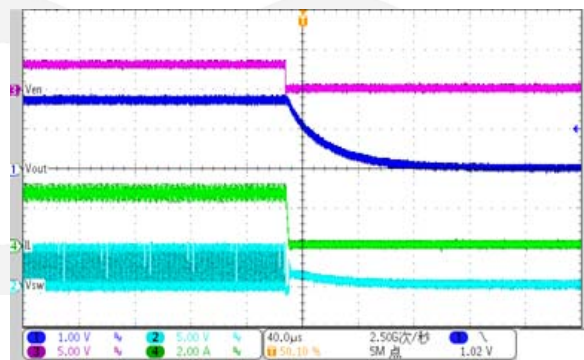
Start up from Enable

($V_{IN}=5V$, $V_{OUT}=1.8V$, $R_{Load}=0.6ohm$)



Shut down from Enable

($V_{IN}=5V$, $V_{OUT}=1.8V$, $R_{Load}=0.6ohm$)



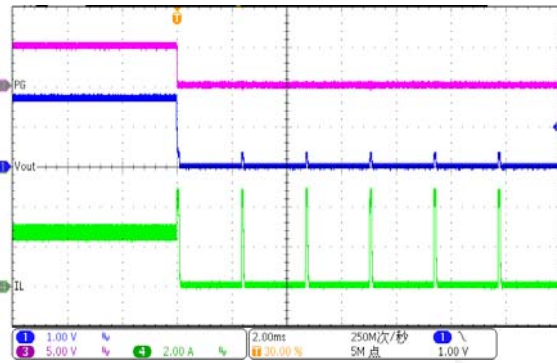


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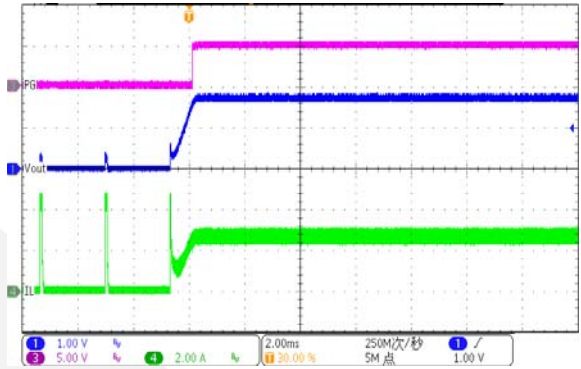
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Typical Performance Characteristics(Continue)

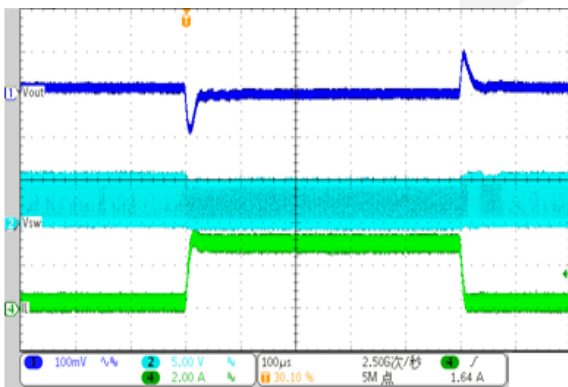
Short Circuit Protection
($V_{IN}=5V$, $V_{OUT}=1.8V$, Load=0.6 to short)



Short Circuit Recovery
($V_{IN}=5V$, $V_{OUT}=1.8V$, Load= short-0.6ohm)



Load Transient
($V_{IN}=5V$, $V_{OUT}=1.8V$, $I_{load}=0.2-3A$)

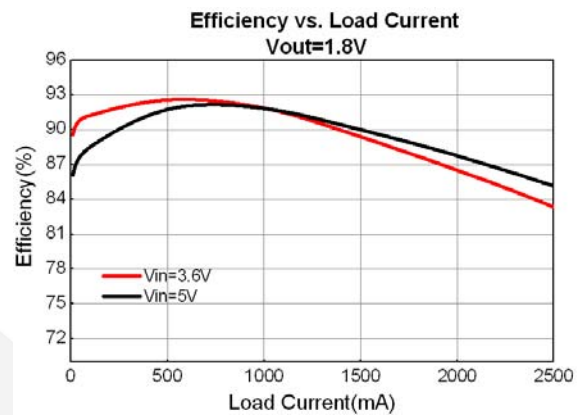
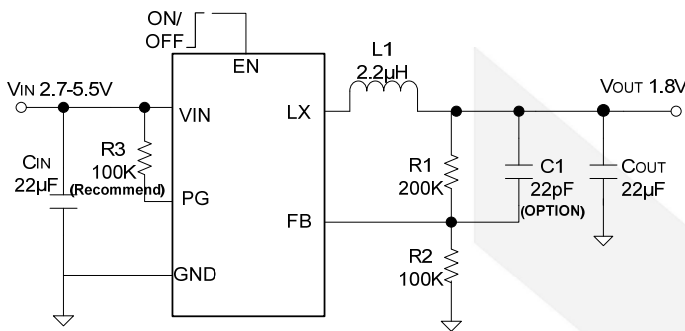




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Typical Application



Application Information

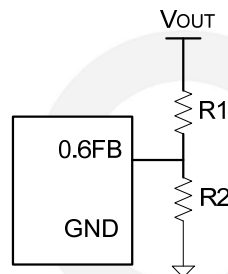
DIO6023 is a synchronous buck regulator IC that integrates the PWM control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low $R_{DS(ON)}$ power switches and proprietary PWM control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

Because of the high integration in the DIO6023 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN} , output capacitor C_{OUT} , output inductor L and feedback resistors ($R1$ and $R2$) need to be selected for the targeted applications specifications.

Feedback resistor dividers $R1$ and $R2$

Choose $R1$ and $R2$ to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both $R1$ and $R2$. A value of between 100k and 1M is highly recommended for both resistors. If $R2=120k$ is chosen, then $R1$ can be calculated to be

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1$$





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Input capacitor C_{IN} :

With the maximum load current at 3A, the maximum ripple current through input capacitor is about 0.6Arms. A typical X7R or better grade ceramic capacitor with 6V rating and greater than 4.7 μ F capacitance can handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} , and IN/GND pins.

Output capacitor C_{OUT} :

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6V rating and greater than 4.7 μ F capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN, MAX})}{F_{SW} \times I_{OUT, MAX} \times 40\%}$$

where F_{sw} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current. The DIO6023 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT} / V_{IN, MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR < 50m Ω to achieve a good overall efficiency.



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Layout Design:

The layout design of DIO6023 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN} , L, R1 and R2.

- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- 2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.
- 3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
- 4) The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.
- 5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down $1M\Omega$ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

Load Transient Considerations:

The DIO6023 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.





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