

DIO7296

Ultra-Small, Low-Input Voltage, Low r_{ON} Load Switch

Features

- Low-Input Voltage: 1.0V to 5.5
- Ultra-Low ON-State Resistance
 - $r_{ON}=45m\Omega$ at $V_{IN}=5.0V$
 - $r_{ON}=52m\Omega$ at $V_{IN}=3.6V$
 - $r_{ON}=64m\Omega$ at $V_{IN}=2.5V$
 - $r_{ON}=83m\Omega$ at $V_{IN}=1.8V$
 - $r_{ON}=151m\Omega$ at $V_{IN}=1.2V$
 - $r_{ON}=190m\Omega$ at $V_{IN}=1.1V$
- 500mA Maximum Continuous Switch Current
- Ultra-Low Quiescent Current: 72nA at 1.8V
- Ultra-Low Shutdown Current: 41nA at 1.8V
- Low Control Input Thresholds Enable Use of 1.2V/1.8V/2.5V/3.3V/5V Logic
- Controlled Slew Rate to Avoid Inrush Current: 244 μ s t_r
- Four-Terminal Wafer-Chip-Scale Package (WLCSP)
 - 0.9mm x 0.9mm, 0.5mm Pitch, 0.5mm Height

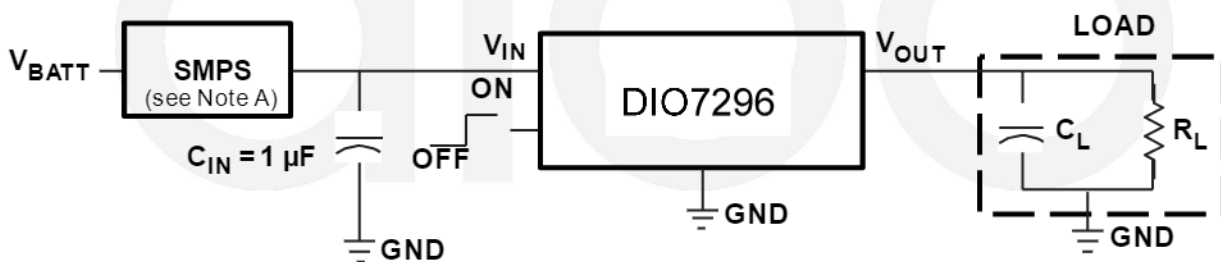
Descriptions

DIO7296 device is an ultra-small, low ON-state resistance (R_{on}) load switch with controlled turn on. The device contains a P-channel MOSFET that operates over an input voltage range of 1.0V to 5.5V. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low voltage control signals. A 120 Ω on chip load resistor is added for output quick discharge when the switch is turned off. DIO7296 is available in a space saving 4 terminal WLCSP with 0.5mm pitch (YZV). The device is characterized for operation over the free-air temperature range of -40°C to 85°C.

Applications

- Personal Digital Assistants (PDAs)
- Cellular Phones
- GPS Devices
- MP3 Players
- Digital Cameras
- Peripheral Ports
- Portable Instrumentation
- RF Modules

Applications





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Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO7296WL4	W76	Green	-40 to +85°C	WLCSP	Tape & Reel, 3000

Pin Assignment

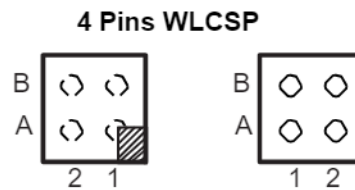


Figure 1 Top View & Bottom View

Pin Descriptions

Name	NO.	Description
V_{OUT}	A1	Switch output
V_{IN}	A2	Switch input, bypass this input with a ceramic capacitor to ground
GND	B1	Ground
ON	B2	Switch control input, active high

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
V_{IN}	Input voltage	-0.3 to 6	V
V_{OUT}	Output voltage	$V_{IN}+0.3$	V
V_{ON}	Input voltage	-0.3 to 6	V
P_D	Power dissipation at $T_A=25^\circ\text{C}$	0.48	W
I_{MAX}	Maximum continuous switch current	500	mA
T_A	Operating free air temperature range	-40 to 85	$^\circ\text{C}$
Maximum lead temperature (10s soldering time), T_{lead}		300	$^\circ\text{C}$
Storage temperature, T_{stg}		-45 to 145	$^\circ\text{C}$
Thermal Resistance	θ_{JA}	189.1	$^\circ\text{C/W}$
ESD	HBM: All Pins	± 4000	V
Latch up		± 400	mA

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter		Rating	Unit
V_{IN}	Input voltage range	1 to 5.5	V
V_{OUT}	Output voltage range	V_{IN}	V
V_{IH}	High level input voltage, ON	0.85 to 5.5	V
V_{IL}	Low level input voltage, ON	0.4	V
C_{IN}	Input capacitor	1	μF



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Electrical Characteristics

$V_{IN}=1.0V$ to $5.5V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$, unless otherwise specified.

Symbol	Parameter	Conditions	T_A	Min.	Typ.	Max.	Unit
I_{IN}	Quiescent current	$I_{OUT}=0$, $V_{IN}=V_{ON}$	$V_{IN}=1.1V$	Full		30	nA
			$V_{IN}=1.2V$	Full		37	
			$V_{IN}=1.8V$	Full		72	
			$V_{IN}=3.6V$	Full		178	
			$V_{IN}=5.0V$	Full		260	
$I_{IN(OFF)}$	OFF-state supply current	$V_{ON}=GND$, $OUT=Open$	$V_{IN}=1.1V$	Full		20	nA
			$V_{IN}=1.2V$	Full		22	
			$V_{IN}=1.8V$	Full		41	
			$V_{IN}=3.6V$	Full		101	
			$V_{IN}=5.0V$	Full		161	
$I_{IN(LEAKAGE)}$	OFF-state switch current	$V_{ON}=GND$, $V_{OUT}=0$	$V_{IN}=1.1V$	Full		20	nA
			$V_{IN}=1.2V$	Full		22	
			$V_{IN}=1.8V$	Full		40	
			$V_{IN}=3.6V$	Full		101	
			$V_{IN}=5.0V$	Full		162	
R_{ON}	ON-state resistance	$I_{OUT}=-200mA$	$V_{IN}=5.0V$	$25^{\circ}C$		45	m Ω
				Full			
			$V_{IN}=3.6V$	$25^{\circ}C$		52	
				Full			
			$V_{IN}=2.5V$	$25^{\circ}C$		64	
				Full			
			$V_{IN}=1.8V$	$25^{\circ}C$		83	
				Full			
			$V_{IN}=1.2V$	$25^{\circ}C$		151	
				Full			
			$V_{IN}=1.1V$	$25^{\circ}C$		190	
				Full			
R_{PD}	Output pulldown resistance	$V_{IN}=3.3V$, $V_{ON}=0$, $I_{OUT}=30mA$	$25^{\circ}C$		92	120	Ω
I_{ON}	ON input leakage current	$V_{ON}=1.1V$ to $5.0V$ or GND	Full			48	nA

Specifications subject to change without notice.



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Switching Characteristics

$R_{L_CHIP}=120\Omega$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IN}=1.1V$						
t_{ON}	Turnon time	$R_L=500\Omega$	$C_L=0.1\mu F$		828	μs
			$C_L=1\mu F$		924	
			$C_L=3.3\mu F$		1016	
t_{OFF}	Turnoff time	$R_L=500\Omega$	$C_L=0.1\mu F$		20	μs
			$C_L=1\mu F$		124	
			$C_L=3.3\mu F$		404	
t_r	V_{OUT} rise time	$R_L=500\Omega$	$C_L=0.1\mu F$		402	μs
			$C_L=1\mu F$		380	
			$C_L=3.3\mu F$		392	
t_f	V_{OUT} fall time	$R_L=500\Omega$	$C_L=0.1\mu F$		29	μs
			$C_L=1\mu F$		316	
			$C_L=3.3\mu F$		1024	
$V_{IN}=1.2V$						
t_{ON}	Turnon time	$R_L=500\Omega$	$C_L=0.1\mu F$		746	μs
			$C_L=1\mu F$		840	
			$C_L=3.3\mu F$		920	
t_{OFF}	Turnoff time	$R_L=500\Omega$	$C_L=0.1\mu F$		16	μs
			$C_L=1\mu F$		94	
			$C_L=3.3\mu F$		360	
t_r	V_{OUT} rise time	$R_L=500\Omega$	$C_L=0.1\mu F$		334	μs
			$C_L=1\mu F$		348	
			$C_L=3.3\mu F$		364	
t_f	V_{OUT} fall time	$R_L=500\Omega$	$C_L=0.1\mu F$		21	μs
			$C_L=1\mu F$		258	
			$C_L=3.3\mu F$		696	
$V_{IN}=1.8V$						
t_{ON}	Turnon time	$R_L=500\Omega$	$C_L=0.1\mu F$		492	μs
			$C_L=1\mu F$		544	
			$C_L=3.3\mu F$		604	
t_{OFF}	Turnoff time	$R_L=500\Omega$	$C_L=0.1\mu F$		10	μs
			$C_L=1\mu F$		60	
			$C_L=3.3\mu F$		212	



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t_r	V_{OUT} rise time	$R_L=500\Omega$	$C_L=0.1\mu F$	244	μs
			$C_L=1\mu F$	232	
			$C_L=3.3\mu F$	240	
t_f	V_{OUT} fall time	$R_L=500\Omega$	$C_L=0.1\mu F$	19	μs
			$C_L=1\mu F$	216	
			$C_L=3.3\mu F$	740	
$V_{IN}=2.5V$					
t_{ON}	Turnon time	$R_L=500\Omega$	$C_L=0.1\mu F$	362	μs
			$C_L=1\mu F$	406	
			$C_L=3.3\mu F$	440	
t_{OFF}	Turnoff time	$R_L=500\Omega$	$C_L=0.1\mu F$	9	μs
			$C_L=1\mu F$	60	
			$C_L=3.3\mu F$	180	
t_r	V_{OUT} rise time	$R_L=500\Omega$	$C_L=0.1\mu F$	194	μs
			$C_L=1\mu F$	194	
			$C_L=3.3\mu F$	136	
t_f	V_{OUT} fall time	$R_L=500\Omega$	$C_L=0.1\mu F$	18	μs
			$C_L=1\mu F$	208	
			$C_L=3.3\mu F$	676	
$V_{IN}=3.0V$					
t_{ON}	Turnon time	$R_L=500\Omega$	$C_L=0.1\mu F$	302	μs
			$C_L=1\mu F$	342	
			$C_L=3.3\mu F$	374	
t_{OFF}	Turnoff time	$R_L=500\Omega$	$C_L=0.1\mu F$	9	μs
			$C_L=1\mu F$	58	
			$C_L=3.3\mu F$	172	
t_r	V_{OUT} rise time	$R_L=500\Omega$	$C_L=0.1\mu F$	174	μs
			$C_L=1\mu F$	168	
			$C_L=3.3\mu F$	180	
t_f	V_{OUT} fall time	$R_L=500\Omega$	$C_L=0.1\mu F$	18	μs
			$C_L=1\mu F$	211	
			$C_L=3.3\mu F$	684	
$V_{IN}=3.6V$					
t_{ON}	Turnon time	$R_L=500\Omega$	$C_L=0.1\mu F$	257	μs
			$C_L=1\mu F$	291	
			$C_L=3.3\mu F$	324	



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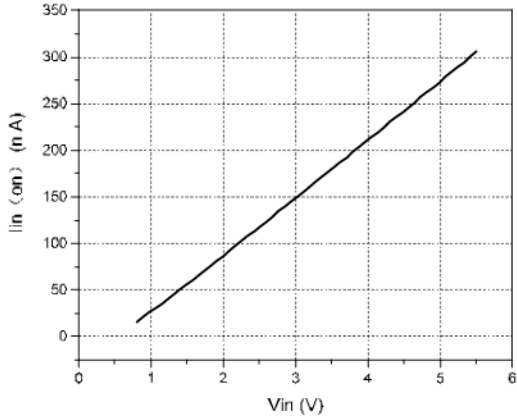
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t_{OFF}	Turnoff time	$R_L=500\Omega$	$C_L=0.1\mu F$	8	μs
			$C_L=1\mu F$	54	
			$C_L=3.3\mu F$	160	
t_r	V_{OUT} rise time	$R_L=500\Omega$	$C_L=0.1\mu F$	158	μs
			$C_L=1\mu F$	156	
			$C_L=3.3\mu F$	160	
t_f	V_{OUT} fall time	$R_L=500\Omega$	$C_L=0.1\mu F$	18	μs
			$C_L=1\mu F$	199	
			$C_L=3.3\mu F$	680	
$V_{IN}=5.0V$					
t_{ON}	Turnon time	$R_L=500\Omega$	$C_L=0.1\mu F$	193	μs
			$C_L=1\mu F$	229	
			$C_L=3.3\mu F$	235	
t_{OFF}	Turnoff time	$R_L=500\Omega$	$C_L=0.1\mu F$	8	μs
			$C_L=1\mu F$	49	
			$C_L=3.3\mu F$	146	
t_r	V_{OUT} rise time	$R_L=500\Omega$	$C_L=0.1\mu F$	139	μs
			$C_L=1\mu F$	135	
			$C_L=3.3\mu F$	143	
t_f	V_{OUT} fall time	$R_L=500\Omega$	$C_L=0.1\mu F$	17	μs
			$C_L=1\mu F$	185	
			$C_L=3.3\mu F$	625	

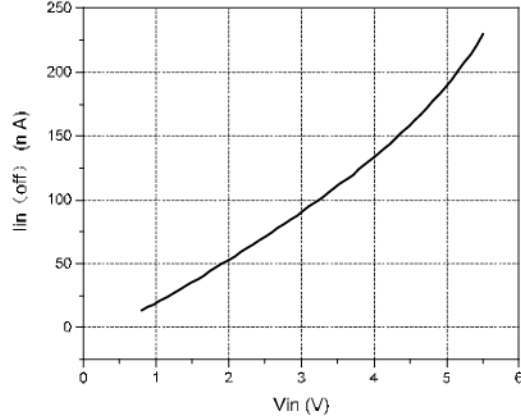
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Typical Performance Characteristics

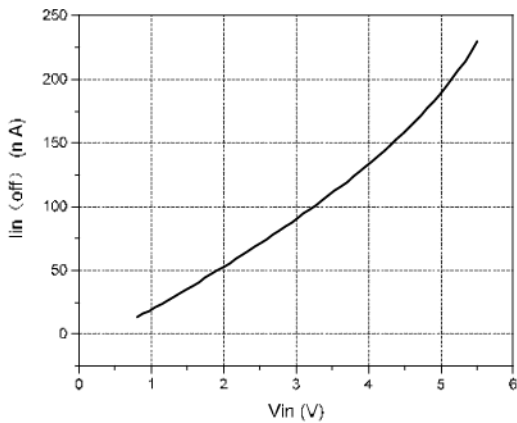
$I_{IN(ON)}$ vs. V_{IN}
($V_{ON}=V_{IN}$, $I_{OUT}=0$)



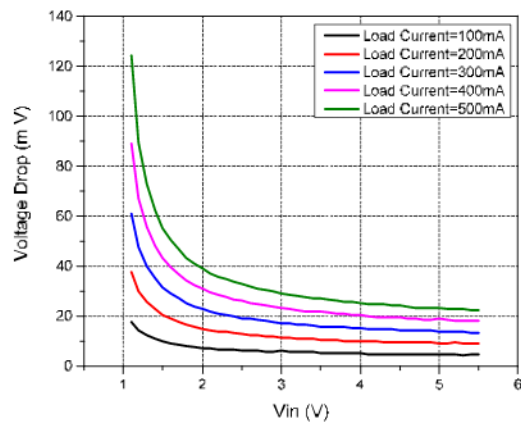
$I_{IN(OFF)}$ vs. V_{IN}
($V_{ON}=0$, $OUT=Open$)



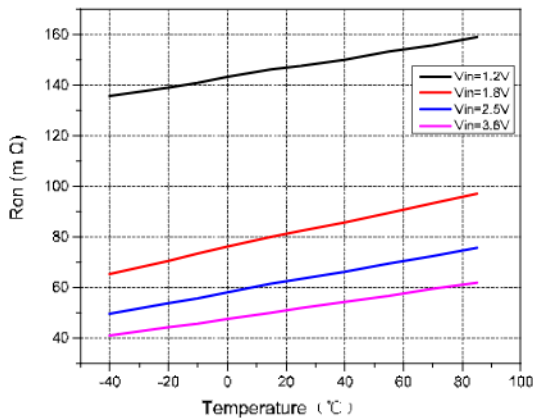
$I_{IN(Leakage)}$ vs. V_{IN}
($V_{ON}=0$, $OUT=0$)



Voltage Drop vs. V_{IN}



R_{ON} vs. Temperature
(Load Current=200mA)



Detailed Description

Overview

DIO7296 is a low ON-state resistance (r_{ON}) load switch with controlled turnon. The device contains a P-channel MOSFET that operates over an input voltage range of 1.0 V to 5.5 V. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. A 120- Ω on-chip load resistor is added for output quick discharge when the switch is turned off.

Functional Block Diagram

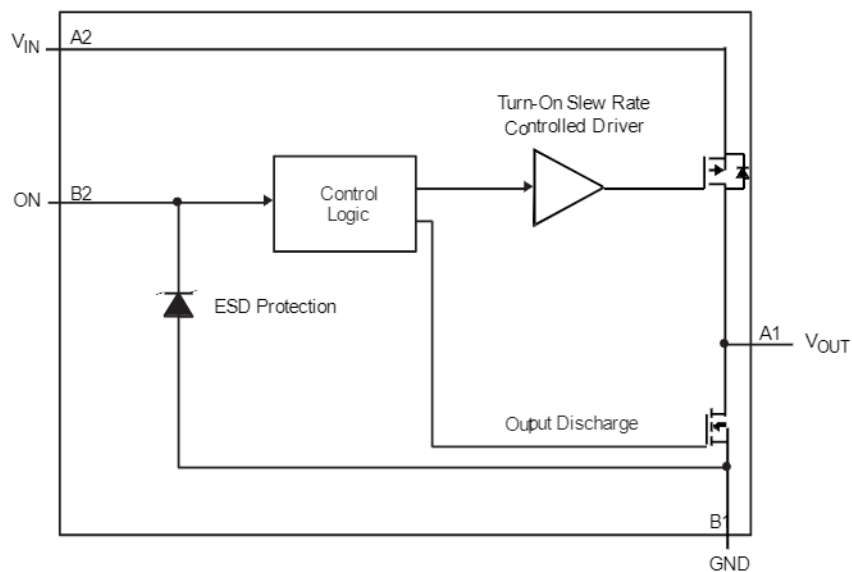


Figure 2. Block Diagram

Feature Description

ON/OFF Control

The ON pin controls the state of the switch. Activating ON continuously holds the switch in the on state so long as there is no fault. ON is active HI and has a low threshold making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, 3.3-V or 5.0-V GPIOs.

Device Functional Modes

Table 1 lists the functional modes of the DIO7296.

Table 1. Function Table

ON (Control Input)	V_{IN} to V_{OUT}	V_{OUT} to GND
L	OFF	ON
H	ON	OFF

Application and Implementation

Application Information

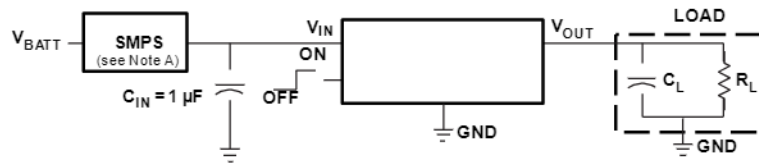
Input Capacitor

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A $1\mu\text{F}$ ceramic capacitor, C_{IN} , placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current application. When switching heavy loads, it is recommended to have an input capacitor approximately 10 times higher than the output capacitor to avoid excessive voltage drop.

Output Capacitor

Due to the integral body diode in the PMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} .

Typical Application



A. Switched mode power supply

Figure 3. Powering a Downstream Module

Design Requirements

Table 2 lists the design parameters for the DIO7296 device.

Table 2. Design Parameters

Design Parameter	Example Value
V_{IN}	1.8V
Load Current	0.3A
Ambient Temperature	25°C

Detailed Design Procedure

V_{IN} to V_{OUT} Voltage Drop

The voltage drop from V_{IN} to V_{OUT} is determined by the ON-resistance of the device and the load current. The r_{ON} can be found in Electrical Characteristics and is dependent on temperature. When the value of r_{ON} is found,

Equation 1 can be used to calculate the voltage drop across the device:

$$\Delta V = I_{LOAD} \cdot r_{ON} \quad (1)$$

Where

- ΔV = Voltage drop across the device
- I_{LOAD} = Load current
- r_{ON} = ON-resistance of the device

At $V_{IN}=1.8V$, the DIO7296 has a r_{ON} value of $83m\Omega$. Using this value and the defined load current, the above equation can be evaluated:

$$\Delta V = 0.30A \cdot 83m\Omega \quad (2)$$

Where

- ΔV = 24.9mV

Therefore, the voltage drop across the device will be 24.9mV.

Power Supply Recommendations

The device is designed to operate with a V_{IN} range of 1.1V to 5.5V. This supply must be well regulated and placed as close to the device terminals as possible. It must also be able to withstand all transient and load currents, using a recommended input capacitance of $1\mu F$ if necessary. If the supply is more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of $10\mu F$ may be sufficient.

Layout

Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short circuit operation. Using wide traces for V_{IN} , V_{OUT} , and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

Layout Example

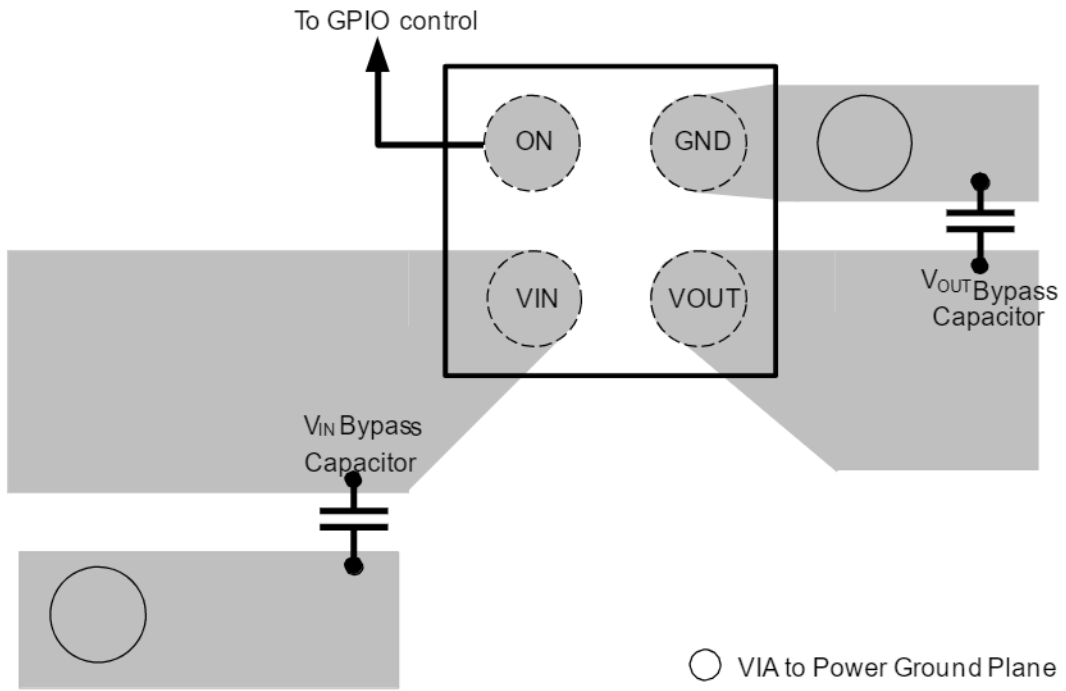


Figure 4. Recommended Board Layout



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