

**DISPLAY Elektronik GmbH**

# DATA SHEET

**LCD MODULE**

**DEM 128064L1 FGH-PW**

*Product Specification*

*Version: 1*

**31.08.2021**

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# GENERAL SPECIFICATION

MODULE NO. :

## DEM 128064L1 SERIES

VERSION NO.	CHANGE DESCRIPTION	DATE
0	Original Version	13.08.2021
1	Correct the module drawing on page 3; Update the LCD drawing on page 17-page 18.	31.08.2021

PREPARED BY: CC

DATE: 31.08.2021

APPROVED BY: WH

DATE: 31.08.2021

*Version: 1*

*PAGE:*

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**1. FUNCTIONS & FEATURES**

┃ DEM 128064L1 Series LCD Type :

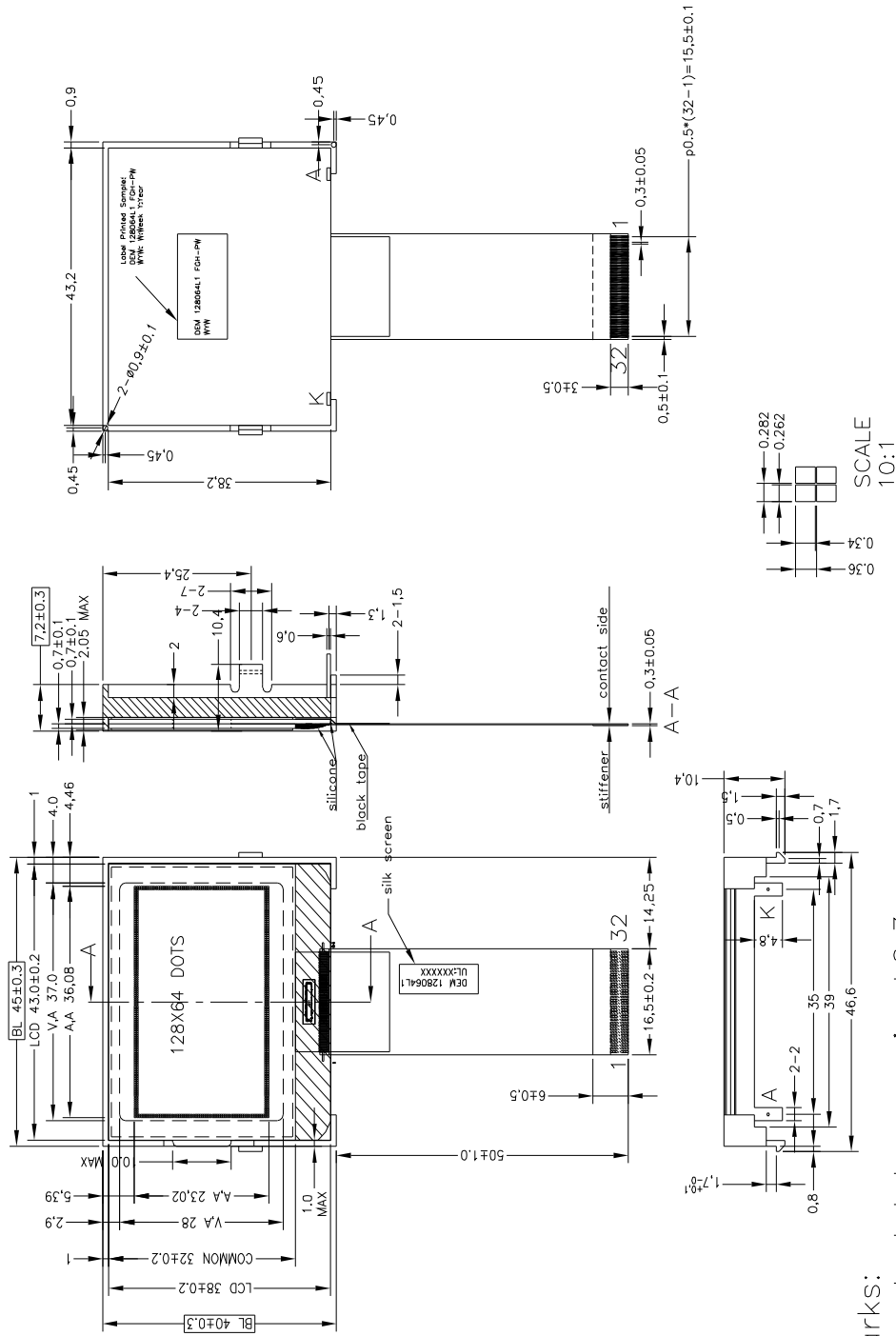
<b>MODULE</b>	<b>LCD TYPE</b>	<b>REMARKS</b>
DEM 128064L1 FGH-PW	FSTN Transflective Positive Mode	

- ┃ Viewing Direction : 6 O'clock
- ┃ Driving Scheme : 1/65 Duty Cycle, 1/9 Bias
- ┃ Power Supply Voltage(Typ.) : 3.3 V
- ┃ LCD Operation Voltage :9.0 V
- ┃ Display Contents :128x64 Dots
- ┃ Backlight : LED,Lightguide,White
- ┃ Operating temperature : -20°C ~ +70°C
- ┃ Storage temperature : -30°C ~ +80°C
- ┃ RoHS Compliant

**2. MECHANICAL SPECIFICATIONS**

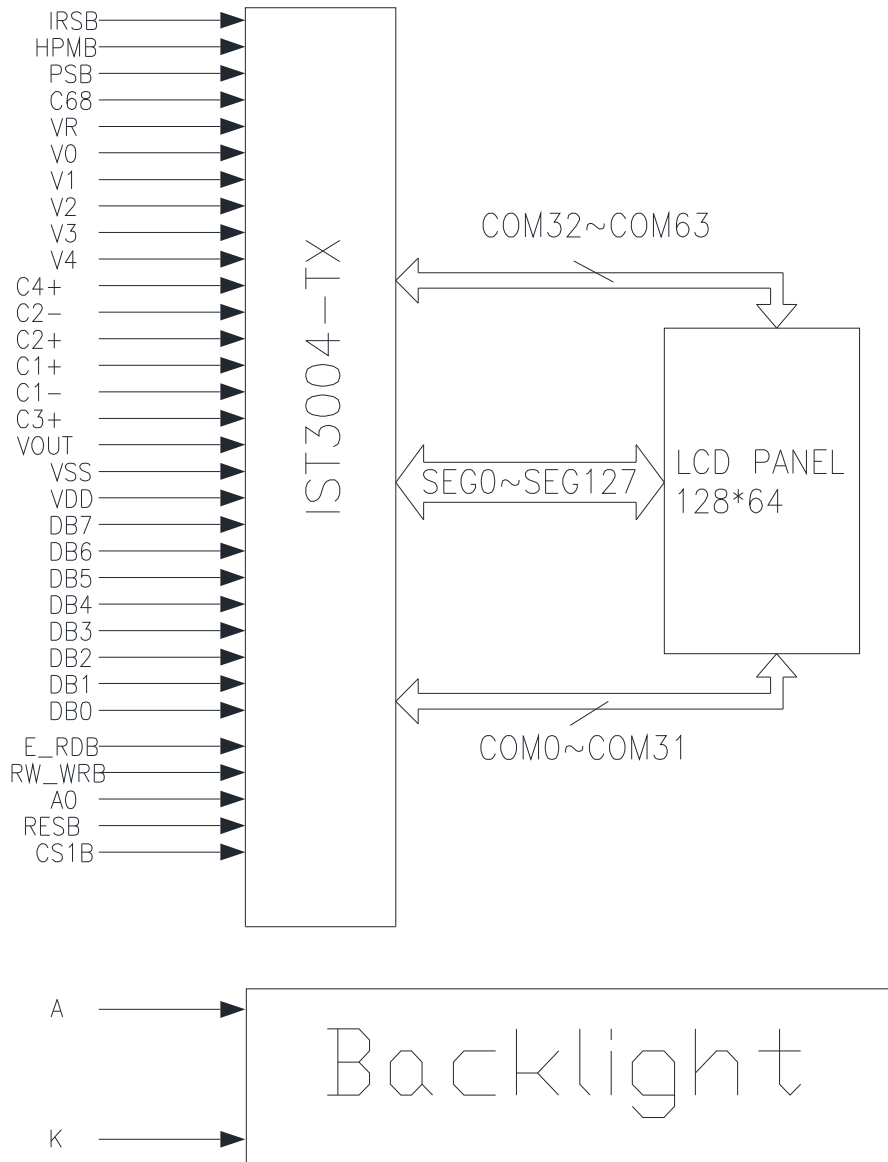
- ┃ Module Size: : 46.60 x 40.00 x 10.40 mm (without FPC)
- ┃ Viewing Area Size: : 37.00 x 28.00 mm
- ┃ Active Area Size : 36.076 x 23.020 mm
- ┃ Dot pitch: : 0.282 x 0.36 mm
- ┃ Dot Size: : 0.262 x 0.34 mm

3. EXTERNAL DIMENSIONS



Remarks:  
 1. Unmarked tolerance is  $\pm 0.3$   
 2. All materials comply with RoHs  
 3.  ...:critical dimension.

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

Pin No.	Name	Description																					
1	IRS	Voltage regulator internal/external resistor source select IRS = "L" → Use external resistor source through VR terminal IRS = "H" → Use internal resistor source																					
2	HPMB	Power circuit driving ability control - HPMB = "H" : Normal mode - HPMB = "L" : High power mode																					
3	PS	Parallel / serial data input select input																					
		<table border="1"> <thead> <tr> <th>PS</th> <th>Interface Mode</th> <th>Chip Select</th> <th>Data / instruction</th> <th>Data</th> <th>Read / Write</th> <th>Serial clock</th> </tr> </thead> <tbody> <tr> <td>"H"</td> <td>Parallel</td> <td>CS1B</td> <td>A0</td> <td>DB0 to DB7</td> <td>E_RDB RW_WRB</td> <td>--</td> </tr> <tr> <td>"L"</td> <td>Serial</td> <td>CS1B</td> <td>A0</td> <td>SDI (DB7)</td> <td>Write only</td> <td>SCL (DB6)</td> </tr> </tbody> </table>	PS	Interface Mode	Chip Select	Data / instruction	Data	Read / Write	Serial clock	"H"	Parallel	CS1B	A0	DB0 to DB7	E_RDB RW_WRB	--	"L"	Serial	CS1B	A0	SDI (DB7)	Write only	SCL (DB6)
		PS	Interface Mode	Chip Select	Data / instruction	Data	Read / Write	Serial clock															
"H"	Parallel	CS1B	A0	DB0 to DB7	E_RDB RW_WRB	--																	
"L"	Serial	CS1B	A0	SDI (DB7)	Write only	SCL (DB6)																	
<NOTE> In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 and E_RDB and RW_WRB must be fixed to either "H" or "L".																							
4	C68	Microprocessor Interface Select input pin in parallel mode - C68 = "H" : 6800-series MPU interface - C68 = "L" : 8080-series MPU interface																					
5	VR	Voltage regulator terminal When IRS = "L", the Voltage Regulator resistor will be decided by the external resistors connected between V0/VR & VR/VSS																					
6	V0	LCD driver supplies voltages																					
7	V1																						
8	V2																						
9	V3																						
10	V4																						
11	C4+	DC/DC voltage converter.																					
12	C2-																						
13	C2+																						
14	C1+																						
15	C1-																						
16	C3+																						
17	VOUT																						
18	VSS	Ground																					
19	VDD	power supply																					
20	DB7	8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L"); - DB0 to DB5 : high impedance - DB6 : serial input clock (SCL) - DB7 : serial input data (SDI) When chip select is not active, DB0 to DB7 may be high impedance.																					
21	DB6																						
22	DB5																						
23	DB4																						
24	DB3																						
25	DB2																						
26	DB1																						
27	DB0																						
28	E-RDB	Read / Write execution control pin																					
		<table border="1"> <thead> <tr> <th>C68</th> <th>MPU Type</th> <th>E_RDB</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>6800-series</td> <td>E</td> <td>Read / Write control input pin - RW = "H" : When E is "H", DB0 to DB7 are in an output status. - RW = "L" : The data on DB0 to DB7 are latched at the falling edge the E signal.</td> </tr> <tr> <td>L</td> <td>8080-series</td> <td>/RDB</td> <td>Read enable clock input pin When / RDB is "L", DB0 to DB7 are in an output status.</td> </tr> </tbody> </table>	C68	MPU Type	E_RDB	Description	H	6800-series	E	Read / Write control input pin - RW = "H" : When E is "H", DB0 to DB7 are in an output status. - RW = "L" : The data on DB0 to DB7 are latched at the falling edge the E signal.	L	8080-series	/RDB	Read enable clock input pin When / RDB is "L", DB0 to DB7 are in an output status.									
		C68	MPU Type	E_RDB	Description																		
H	6800-series	E	Read / Write control input pin - RW = "H" : When E is "H", DB0 to DB7 are in an output status. - RW = "L" : The data on DB0 to DB7 are latched at the falling edge the E signal.																				
L	8080-series	/RDB	Read enable clock input pin When / RDB is "L", DB0 to DB7 are in an output status.																				

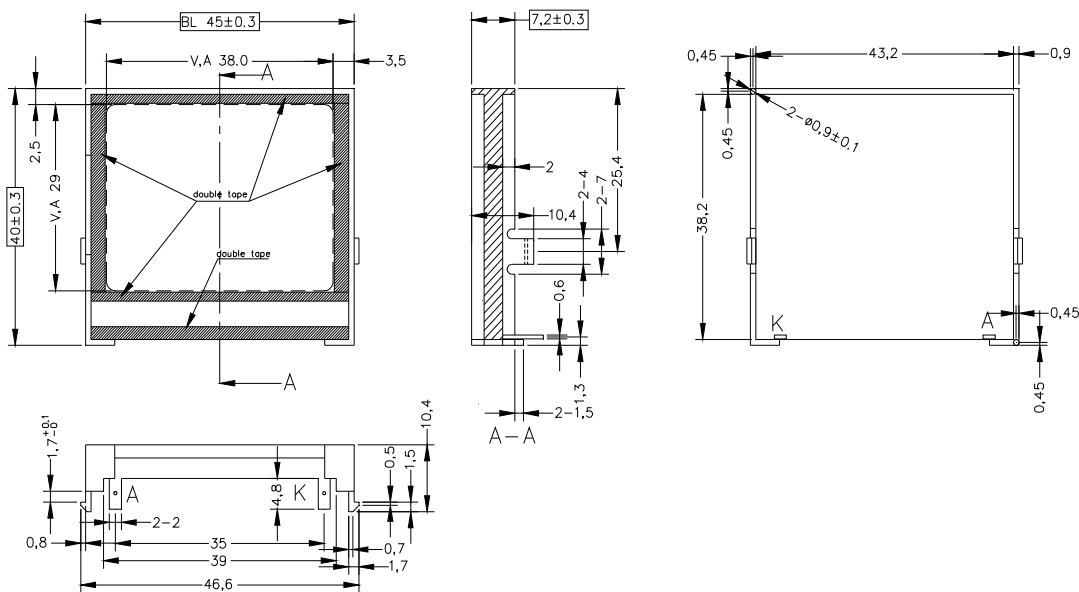
29	RW_WRB	Read / Write execution control pin			
		C68	MPU Type	RW_WRB	Description
		H	6800-series	RW	Read / Write control input pin - RW = "H" : read - RW = "L" : write
		L	8080-series	/WRB	Write enable clock input pin The data on DB0 to DB7 are latched at the rising edge of the /WRB signal.
30	A0	Register select input pin - A0 = "H" : DB0 to DB7 are display data - A0 = "L" : DB0 to DB7 are control data			
31	RESB	Hardware Reset input pin When RESB is "L", initialization is executed.			
32	CS1B	Chip select input pins Data / instruction I/O is enabled only when CS1B is "L" and CS2 is "H". when chip select is non-active, DB0 to DB7 may be high impedance.			

A	Supply voltage for backlight LED+
K	Supply voltage for backlight LED-

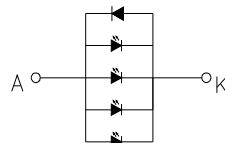


6. BACKLIGHT CHARACTERISTICS

Item	Symbol	min.	typ.	max.	Unit	Condition
Forward Voltage	V <sub>f</sub>	2.9	3.1	3.3	V	I <sub>f</sub> = 60 mA T=25° C
Power Dissipation	P <sub>d</sub>	174	186	198	mW	
Luminous Uniformity	ΔL <sub>v</sub>	70			%	
Luminance	L <sub>v</sub>	420	500		cd/m <sup>2</sup>	
Color Coordinate	X	0.260		0.30		
	Y	0.270		0.31		
Lifetime		50000h			Hours	



Circuit Diagram  
COLOR: WHITE



Remarks:  
1. Unmarked tolerance is ±0.3  
2. All materials comply with RoHs  
3. [ ]...: critical dimension.

**7. ABSOLUTE MAXIMUM RATINGS**

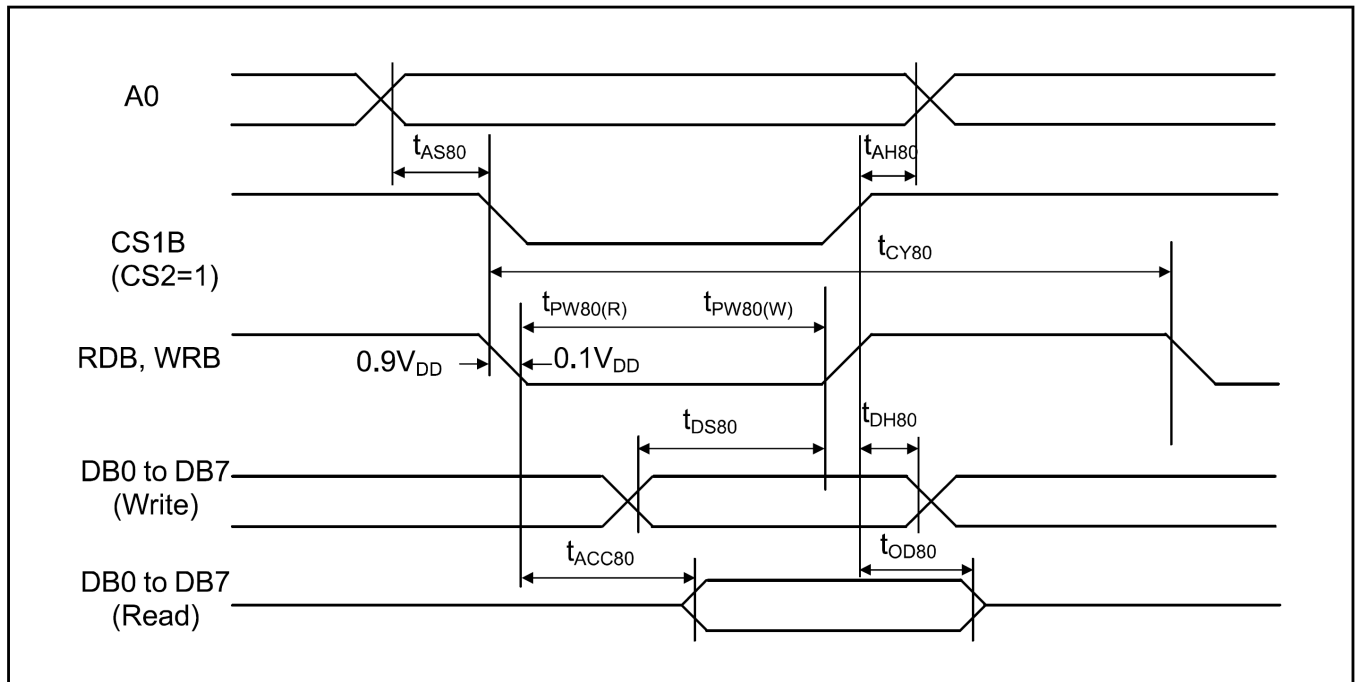
Parameter	Symbol	Rating	Unit
Supply Voltage Range	V <sub>DD</sub>	-0.3 ~ 7.0	V
	V <sub>0</sub> ,V <sub>OUT</sub>	-0.3 ~ 15.0	V
Supply Voltage Range	V <sub>1</sub> /V <sub>2</sub> /V <sub>3</sub> /V <sub>4</sub>	-0.3 ~ V <sub>0</sub>	V
Operating Temperature	T <sub>opr</sub>	-20~+70	°C
Storage Temperature	T <sub>stg</sub>	-30~+80	°C

**8. ELECTRICAL CHARACTERISTICS****8.1. DC CHARACTERISTICS**

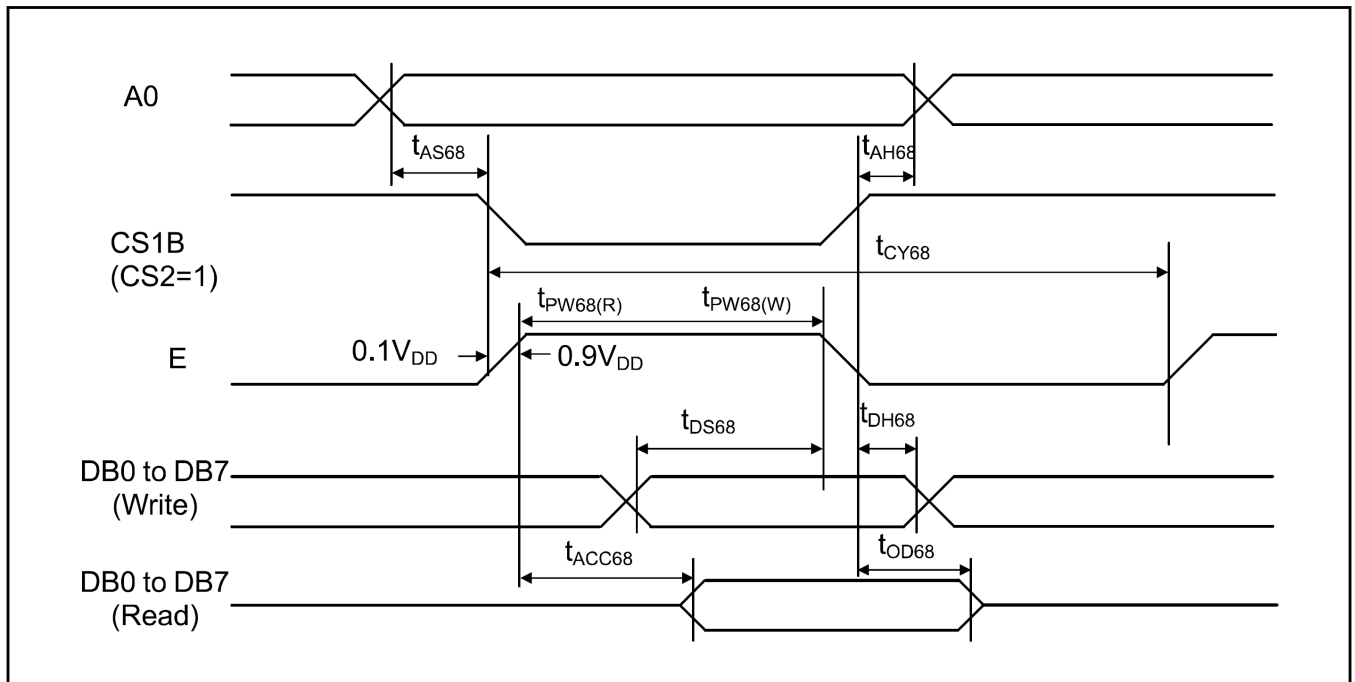
ITEM	symbol	Condition	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Supply Voltage For Logic	V <sub>DD</sub>		3.0	3.3	3.6	V
Supply Voltage For LCD	V <sub>LCD</sub>		8.7	9.0	9.3	V
Current Consumption	I <sub>DD</sub>			TBD		mA
Input Voltage	High	V <sub>IH</sub>	0.8xV <sub>DD</sub>	-	V <sub>DD</sub>	V
	Low	V <sub>IL</sub>	V <sub>SS</sub>	-	0.2xV <sub>DD</sub>	
Output Voltage	High	V <sub>OH</sub>	I <sub>OH</sub> = -0.5mA	0.8xV <sub>DD</sub>	-	V <sub>DD</sub>
	Low	V <sub>OL</sub>	I <sub>OL</sub> = 0.5mA	V <sub>SS</sub>	-	0.2xV <sub>SS</sub>

8.2. AC CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

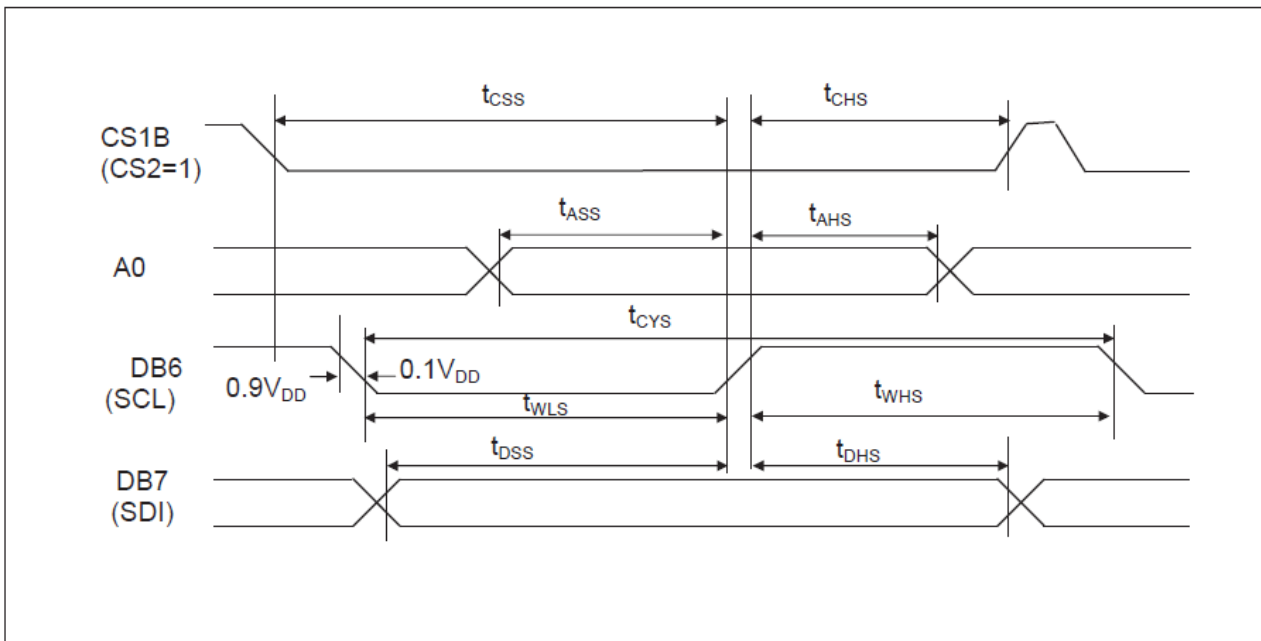


Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time	A0	tAS80	0	-	-	ns	
Address hold time		tAH80	0	-	-	ns	
System cycle time		tCY80	300	-	-	ns	
Pulse width (WRB)	RW_WRB	tPW80(W)	150	-	-	ns	
Pulse width (RDB)	E_RDB	tPW80(R)	150	-	-	ns	
Data setup time	DB7 to DB0	tDS80	60	-	-	ns	
Data hold time		tDH80	0	-	-	ns	
Read access time	DB7 to DB0	tACC80	140	-	-	ns	(No load)
Output disable time		tOD80	-	-	10	ns	



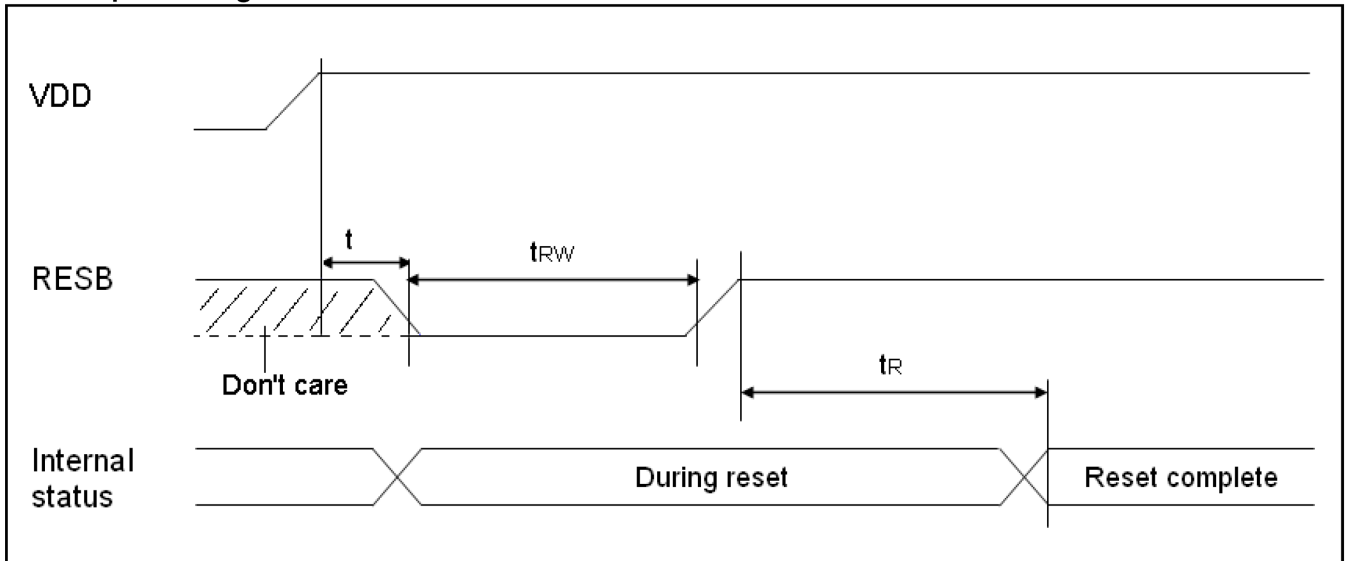
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	A0	tAS68 tAH68	0 0	- -	- -	ns	
System cycle time		tCY68	300	-	-	ns	
Pulse width (E)	RW_WRB	tPW68(W)	150	-	-	ns	
Pulse width (E)	E_RDB	tPW68(R)	150	-	-	ns	
Data setup time Data hold time	DB7 to DB0	tDS68 tDH68	60 0	- -	- -	ns	
Read access time Output disable time		tACC68 tOD68	140 -	- -	- 10	ns	(No load)

Serial Interface



Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle	DB6 (SCL)	tcYS	200	-	-	ns	
SCL high pulse width	DB6 (SCL)	tWHS	90	-	-	ns	
SCL low pulse width	DB6 (SCL)	tWLS	90	-	-	ns	
Address setup time	A0	tASS	45	-	-	ns	
Address hold time	A0	tAHS	45	-	-	ns	
Data setup time	DB7 (SDI)	tDSS	45	-	-	ns	
Data hold time	DB7 (SDI)	tDHS	45	-	-	ns	
CS1B setup time	CS1B	tCSS	90	-	-	ns	
CS1B hold time	CS1B	tCHS	90	-	-	ns	

Reset Input Timing



Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESB	$t_{RW}$	2	-	-	us	*1
Reset time	-	$t_R$	-	-	2	us	
Reset time	RESB	$t$	0	-	-	us	

NOTE

\*1.  $t_R$  (reset time) represents the period from rising edge of reset input to end of internal circuit reset. The IST3004-TX can operate normally after  $t_R$

## 9. COMMAND TABLE

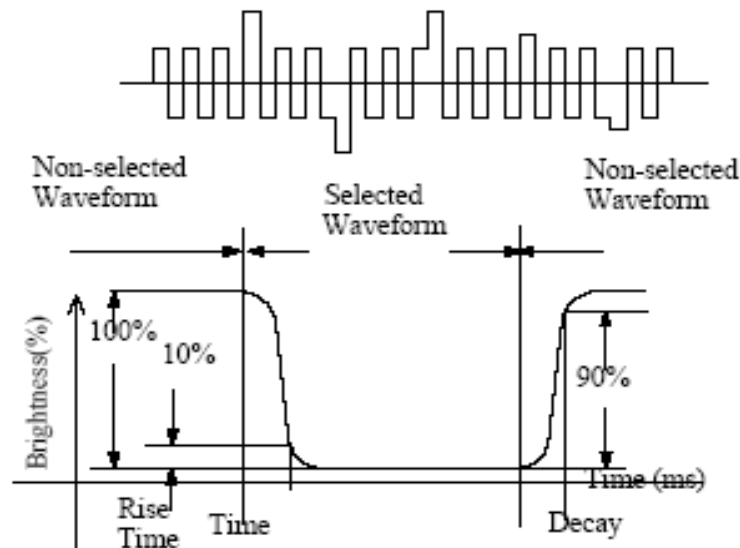
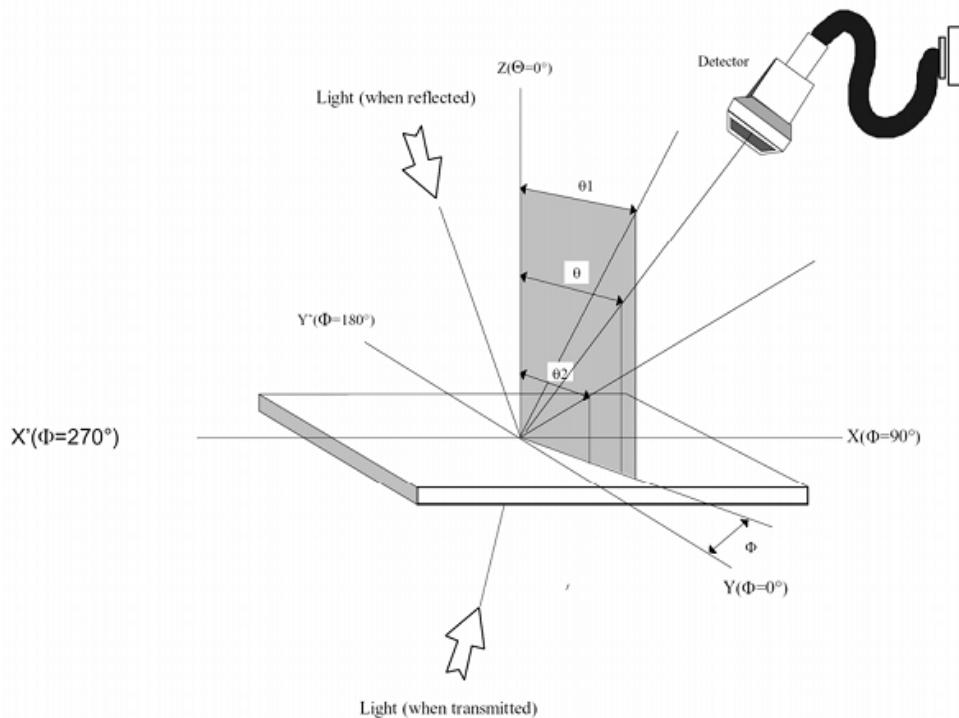
× : Don't care

INSTRUCTION	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	LCD display On/Off control DON = 0 : display OFF DON = 1 : display On
Display starting line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify the line address for the first COM output
page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
Read status	0	1	BUSY	ADC	ON/OFF	RESB	0	0	0	0	Read the internal status
Write display data	1	0	Write data								Write data into Display RAM
Read display data	1	1	Read data								Read data from Display RAM
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG output direction select ADC = 0 : SEG0 → SEG131 ADC = 1 : SEG131 → SEG0
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Normal / Reverse display select REV = 0 : Reverse display off REV = 1 : Reverse display on
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Entire display On/Off control EON = 0 : Entire display off EON = 1 : Entire display on
LCD bias select	0	0	1	0	1	0	0	0	1	BS	Select LCD bias
Set Read-modify-write (RMW)	0	0	1	1	1	0	0	0	0	0	Set Read-modify-write mode
Clear RMW	0	0	1	1	1	0	1	1	1	0	Clear Read-modify-write mode
S/W Reset	0	0	1	1	1	0	0	0	1	0	S/W Reset
SHL select	0	0	1	1	0	0	SHL	×	×	×	COM output direction select SHL = 0 : COM0 → COM63 SHL = 1 : COM63 → COM0
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode (double byte command)
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode (double byte command)
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power save	-	-	-	-	-	-	-	-	-	-	Compound Instruction of display OFF and entire display ON
NOP	0	0	1	1	1	0	0	0	1	1	No operation (dummy command)
Set Booster Ratio select mode	0	0	1	1	1	1	1	0	0	0	Set Booster ration select mode (double byte command)
Set Booster Ratio register	0	0	×	×	×	×	×	×	BT1	BT0	Set Booster ration BT[1:0] = 00 : x2, x3, x4 BT[1:0] = 01 : x5 BT[1:0] = 11 : x6 BT[1:0] = 10 : (don't use)
Test Instruction	0	0	1	0	0	0	1	0	0	0	Test command (don't use)

10.ELECTRO-OPTICAL DEFINITION

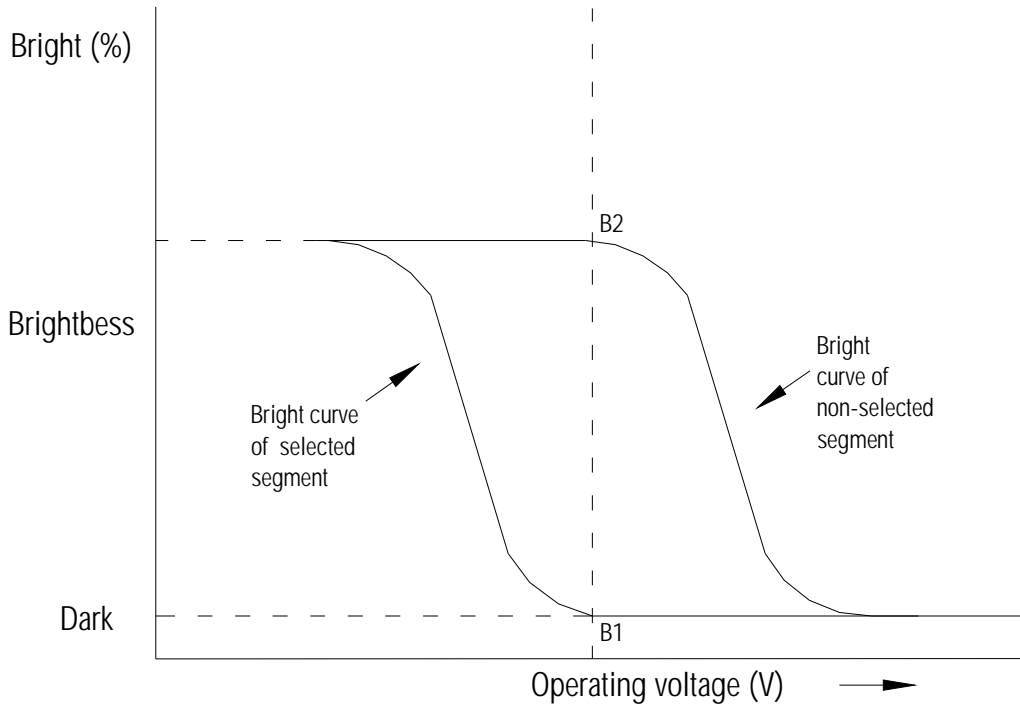
Optical Characteristics

Item	Symbol	Description	Condition	Min	Typ	Max	Unt
Operating Voltage of LCD	V <sub>LCD</sub>	---	Ta=-20°C	9.3	9.6	9.8	V
		---	Ta=25°C	8.7	9.0	9.3	
		---	Ta=70°C	8.3	8.6	8.9	
Response Time	Tr	Rise	25°C	---	200	400	ms
	Tf	Fall	25°C	---	250	500	ms
Contrast	Cr		VDD=3.3V 25°C	---	4	---	
Viewing Angle	$\theta$	6 o'clock axis	Cr $\geq$ 2.0 VDD=3.3V 25°C	---	40	---	deg
		12 o'clock axis	VDD=3.3V 25°C	---	40	---	deg
		3 o'clock axis	VDD=3.3V 25°C	---	40	---	deg
		9 o'clock axis	VDD=3.3V 25°C	---	40	---	deg

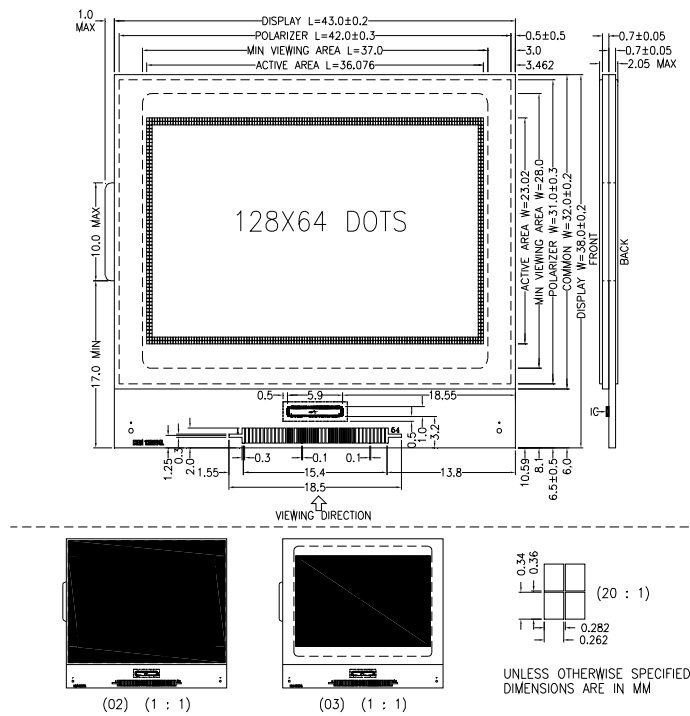




Definition of contrast  $Cr. = \frac{B2}{B1} = \frac{\text{Bright curve of not selected segment}}{\text{Bright curve of selected segment}}$

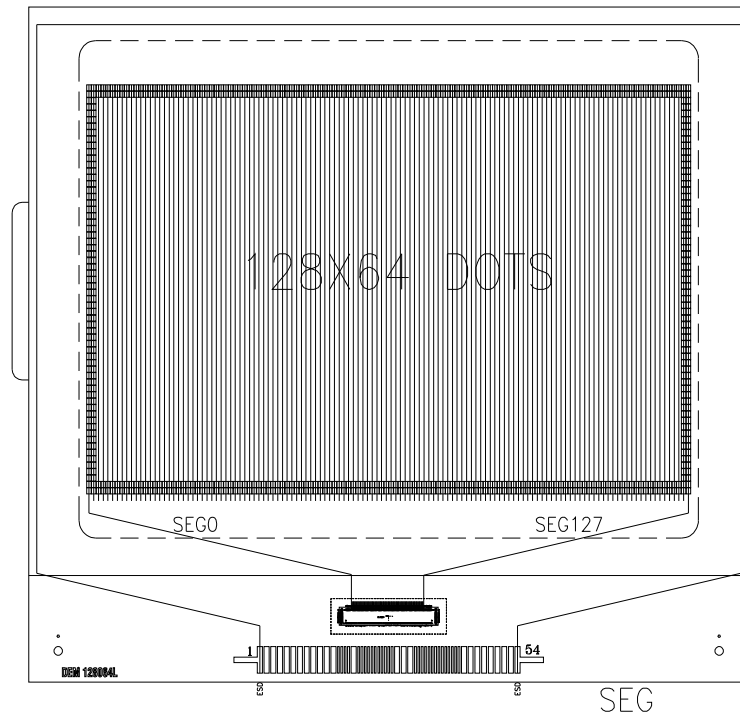


11. LCD ARTWORK

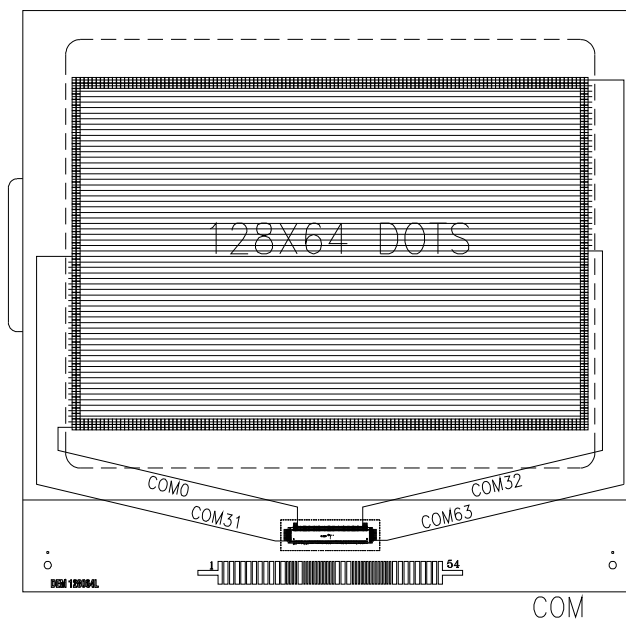


UNLESS OTHERWISE SPECIFIED  
DIMENSIONS ARE IN MM  
TOLERANCES:±0.2MM

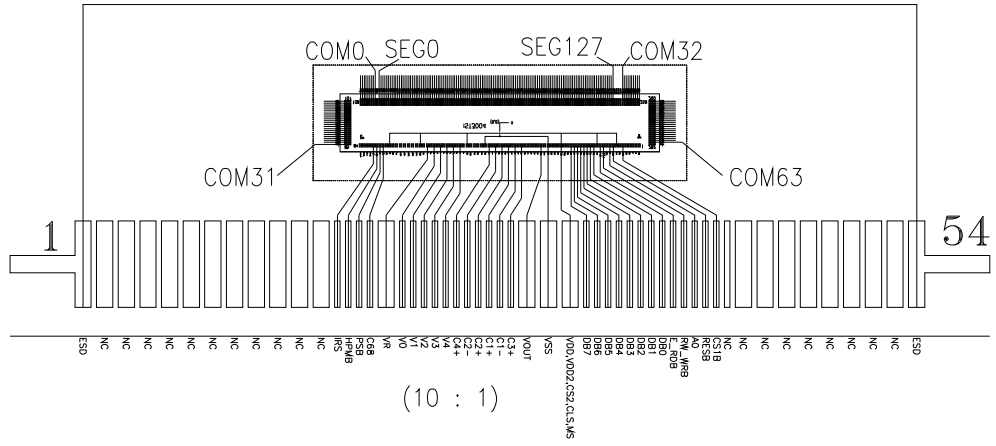
12. SEG LAYOUT



13. COM LAYOUT



14. IC LAYOUT



**15. QUALITY DESCRIPTION**

**DEFECT SPECIFICATION:**

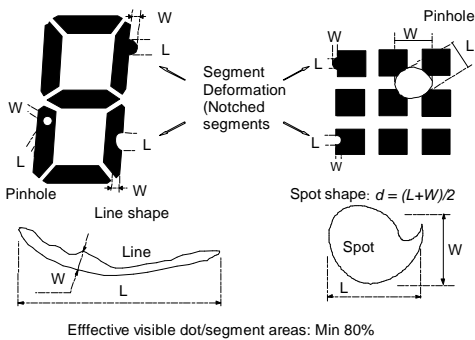
Specific type-related items are covered in this sheet.

a: Table for Cosmetic defects

(Note: nc = not counted).

Sizes and number of defects

(Max. Qty)



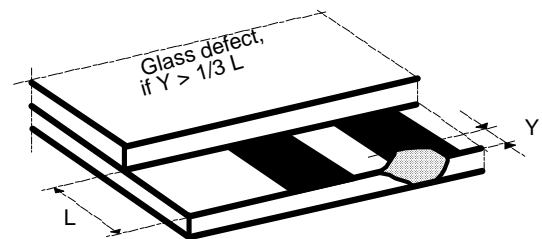
Examples/ Shapes

b: Glass defects

b1: Glass defects at contact ledge

b2: Glass chipping in other areas shall not be in conflict with the product's function.

Defect Type	Max. defect size [ $\mu\text{m}$ ] d or L	W	Max. Quantity.
Black or White Spots	$d \leq 150$		nc
	$150 < d \leq 300$		5
Black or White Lines	--	$W \leq 10$	nc
	$L \leq 5000$	$W \leq 30$	3
	$L \leq 2000$	$W \leq 50$	2
Pinhole	$d \leq 150$		nc
	$150 < d \leq 300$		1/segment
(Total defects)			(5)
Segment Deformation	$W \leq 100$		nc
Bubble (e.g. under pola)	$d \leq 150$		nc
	$200 < d \leq 400$		3
	$400 < d \leq 600$		1



**16. RELIABILITY TEST**

Operating life time: Longer than 50000 hours (at room temperature without direct irradiation of sunlight)

Reliability characteristics shall meet following requirements.

<b>TEMPERATURE TESTS</b>	<b>NORMAL GRADE</b>
High Temperature Storage	+80°C * 96HR
Low Temperature Storage	-30°C * 96HR
High Temperature Operation	+70°C * 96HR
Low Temperature Operation	-20°C * 96HR
High Temperature, High Humidity	+60°C 90%RH 96HR
Thermal Shock	-20°C * 30 min ← 10s ↓ 5Cycles 70°C * 30 min —
Vibration Test	Frequency * Swing * Time 40Hz * 4mm * 4hrs
Drop Test	Drop height * Times 1.0m * 6 times

**17. LCD MODULES HANDLING PRECAUTIONS**

- n The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- n If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.
- n Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- n The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.
- n To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  - Be sure to ground the body when handling the LCD module.
  - Tools required for assembly, such as soldering irons, must be properly grounded.
  - To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  - The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.
- n Storage precautions  
When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

**18. OTHERS**

- n Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.
- n If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.
- n To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:
  - Exposed area of the printed circuit board
  - Terminal electrode sections

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