



TFT LCD Module Product Specification

DT022CTFT
2.2" (240(RGB) x 320 PIXELS) TFT Module

November 4, 2019

Remark:

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Revision Record

| REV | CHANGES | DATE |
|------------|--|-------------|
| 1.0 | First release | Jan 9, 2018 |
| 1.1 | Corrected VSYNC & HSYNC pin location on section 4. Outline Drawing and section 5. Interface Signals. | Nov 4, 2019 |
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1. Scope

This data sheet is to introduce the specification of DT022CTFT active matrix TFT module. It is composed of a color TFT-LCD panel, driver ICs, FPC and a backlight unit. The 2.2" display area contains 240 (RGB) x 320 pixels.

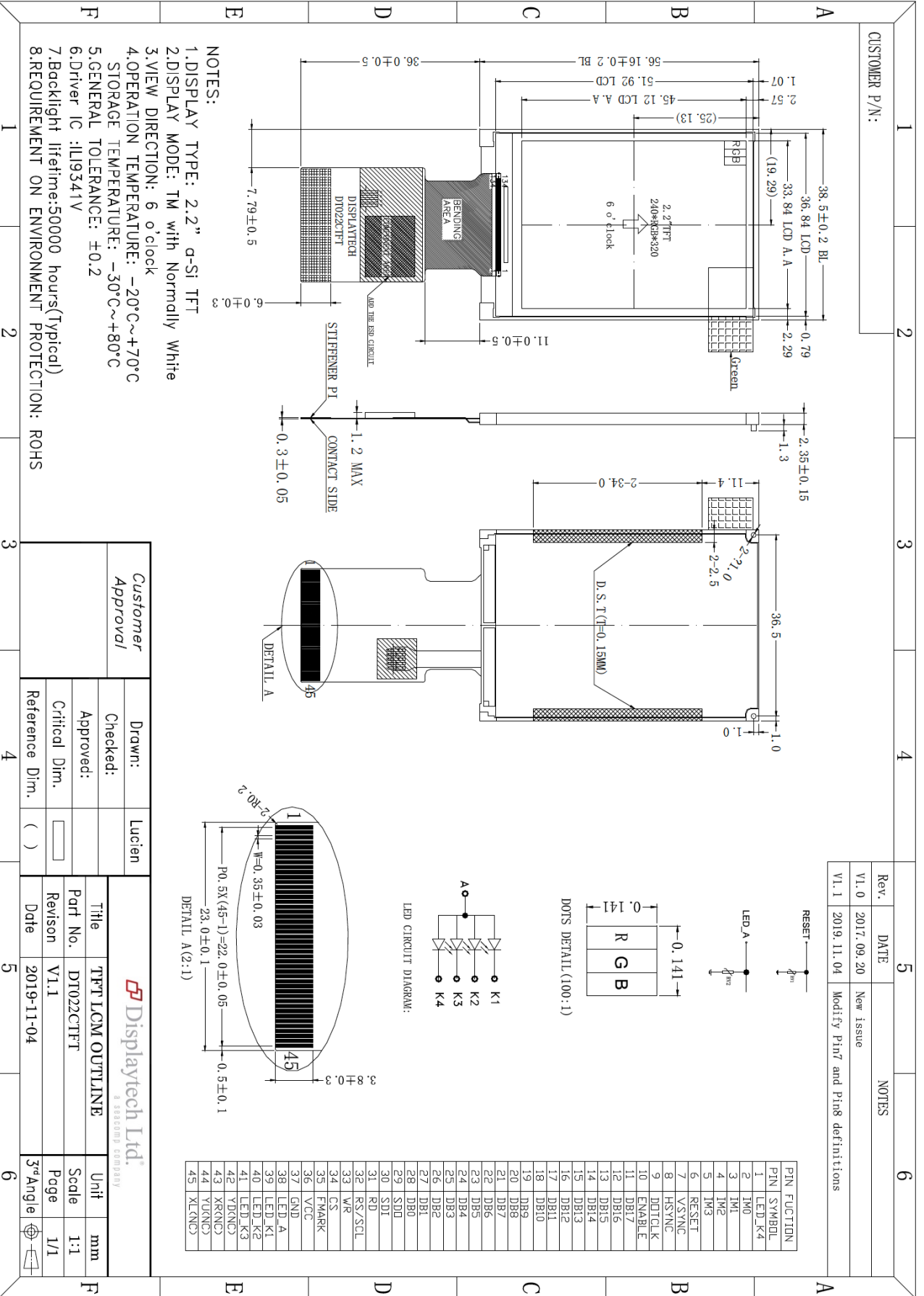
2. Application

Digital equipment which need color display, mobile navigator/video systems.

3. General Information

| Item | Contents | Unit |
|-------------------------------|------------------------------|------|
| Size | 2.2 | inch |
| Resolution | 240(RGB) x 320 | / |
| Interface | RGB/MCU | / |
| Technology Type | a-Si | / |
| Pixel Pitch | 0.141 x 0.141 | mm |
| Pixel Configuration | R.G.B. Vertical Stripe | / |
| Outline Dimension (W x H x D) | 38.50 x 56.16 x 2.35 | mm |
| Active Area | 33.84 x 45.12 | mm |
| Display Mode | Normally white, Transmissive | / |
| Viewing Direction | 6 o'clock | / |
| Backlight Type | LED | / |
| Driver IC | ILI9341V | / |

4. Outline Drawing



5. Interface Signals

| No | Symbol | Description | Remarks |
|---------|------------|--|---------|
| 1 | LED-K4 | LED backlight (Cathode) | |
| 2 | IM0 | System interface select | Note |
| 3 | IM1 | System interface select | |
| 4 | IM2 | System interface select | |
| 5 | IM3 | System interface select | |
| 6 | RESET | Reset signal, Active low | |
| 7 | VSYNC | Frame sync signal for RGB interface operation | |
| 8 | HSYNC | Line sync signal for RGB interface operation | |
| 9 | DOTCLK | Dot clock signal for RGB interface operation | |
| 10 | ENABLE | Data enable signal for RGB interface operation | |
| 11 ~ 28 | DB17 ~ DB0 | Data bus | |
| 29 | SDO | Serial data output in serial bus system interface | |
| 30 | SDI | Serial data Input in serial bus system interface | |
| 31 | RD | Read enable pin I80 parallel bus system interface | |
| 32 | RS/SCL | RS: Data or Command select pin in parallel interface When RS="1", data is selected When RS="0", command is selected SCL: Serial data clock in serial bus system | |
| 33 | WR | Write enable pin in I80 parallel bus system interface | |
| 34 | CS | Chip select signal | |
| 35 | FMARK | Tearing effect output pin to synchronize MPU to frame writing | |
| 36 | VCC | Power supply | |
| 37 | GND | Ground | |
| 38 | LED-A | LED backlight (Anode) | |
| 39 | LED-K1 | LED backlight (Cathode) | |
| 40 | LED-K2 | LED backlight (Cathode) | |
| 41 | LED-K3 | LED backlight (Cathode) | |
| 42 | YD (NC) | Touch panel pin (No connection) | |
| 43 | XR (NC) | Touch panel pin (No connection) | |
| 44 | YU (NC) | Touch panel pin (No connection) | |
| 45 | XL (NC) | Touch panel pin (No connection) | |

Note:

| IM3 | IM2 | IM1 | IM0 | Interface | DB Pin in use | |
|-----|-----|-----|-----|---------------------------------------|-------------------|-------------------|
| | | | | | Register/Content | GRAM |
| 0 | 0 | 0 | 0 | 80 MCU 8-bit bus interface I | DB[7:0] | DB[7:0] |
| 0 | 0 | 0 | 1 | 80 MCU 16-bit bus interface I | DB[7:0] | DB[15:0] |
| 0 | 0 | 1 | 0 | 80 MCU 9-bit bus interface I | DB[7:0] | DB[8:0] |
| 0 | 0 | 1 | 1 | 80 MCU 18-bit bus interface I | DB[7:0] | DB[17:0] |
| 0 | 1 | 0 | 1 | 3-line 9-bit data serial interface I | SDA: In/Out | |
| 0 | 1 | 1 | 0 | 4-line 8-bit data serial interface I | SDA: In/Out | |
| 1 | 0 | 0 | 0 | 80 MCU 16-bit bus interface II | DB[8:1] | DB[17:10] DB[8:1] |
| 1 | 0 | 0 | 1 | 80 MCU 8-bit bus interface II | DB[17:10] | DB[17:10] |
| 1 | 0 | 1 | 0 | 80 MCU 18-bit bus interface II | DB[8:1] | DB[17:0] |
| 1 | 0 | 1 | 1 | 80 MCU 9-bit bus interface II | DB[17:10] | DB[17:9] |
| 1 | 1 | 0 | 1 | 3-line 9-bit data serial interface II | SDI: In, SDO: Out | |
| 1 | 1 | 1 | 0 | 4-line 8-bit data serial interface II | SDI: In, SDO: Out | |

6. Absolute Maximum Ratings

6.1 Electrical absolute maximum ratings

| Parameter | Symbol | MIN | MAX | Unit | Remark |
|----------------------|--------|------|-----|------|--------|
| Power Supply Voltage | VCC | -0.3 | 3.6 | V | |

Notes:

- If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.
- VCC > VSS must be maintained.

6.2 Environment conditions

| Parameter | Symbol | MIN | MAX | Unit | Remark |
|-----------------------|--------|-----|-----|------|--------|
| Operating Temperature | TOPR | -20 | +70 | °C | |
| Storage Temperature | TSTG | -30 | +80 | °C | |

Note:

- The response time will become lower when operated at low temperature.
- Background color changes slightly depending on ambient temperature. The phenomenon is reversible.
- Ta ≤ 40°C: 85%RH MAX.
Ta > 40°C: Absolute humidity must be lower than the humidity of 85%RH at 40°C.

7. Electrical Specifications

7.1 Electrical characteristics

GND=0V, Ta=25°C

| Item | Symbol | MIN | TYP | MAX | Unit | Remark | |
|----------------------|------------|-----|--------|-----|--------|-------------|----------|
| Power Supply | VCC | 2.6 | 2.8 | 3.3 | V | Ta=25°C | |
| Input Signal Voltage | Low Level | VIL | 0 | - | 0.2VCC | V | VCC=2.8V |
| | High Level | VIH | 0.8VCC | - | VCC | V | VCC=2.8V |
| Current Consumption | ICC1 | - | 5 | 10 | mA | Normal mode | |
| | ICC2 | - | 0.05 | 0.1 | mA | Sleep mode | |

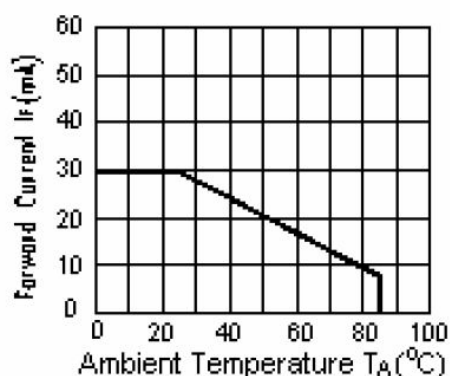
Note: Tested in 1×1 chessboard pattern.

7.2 LED backlight

Ta=25°C

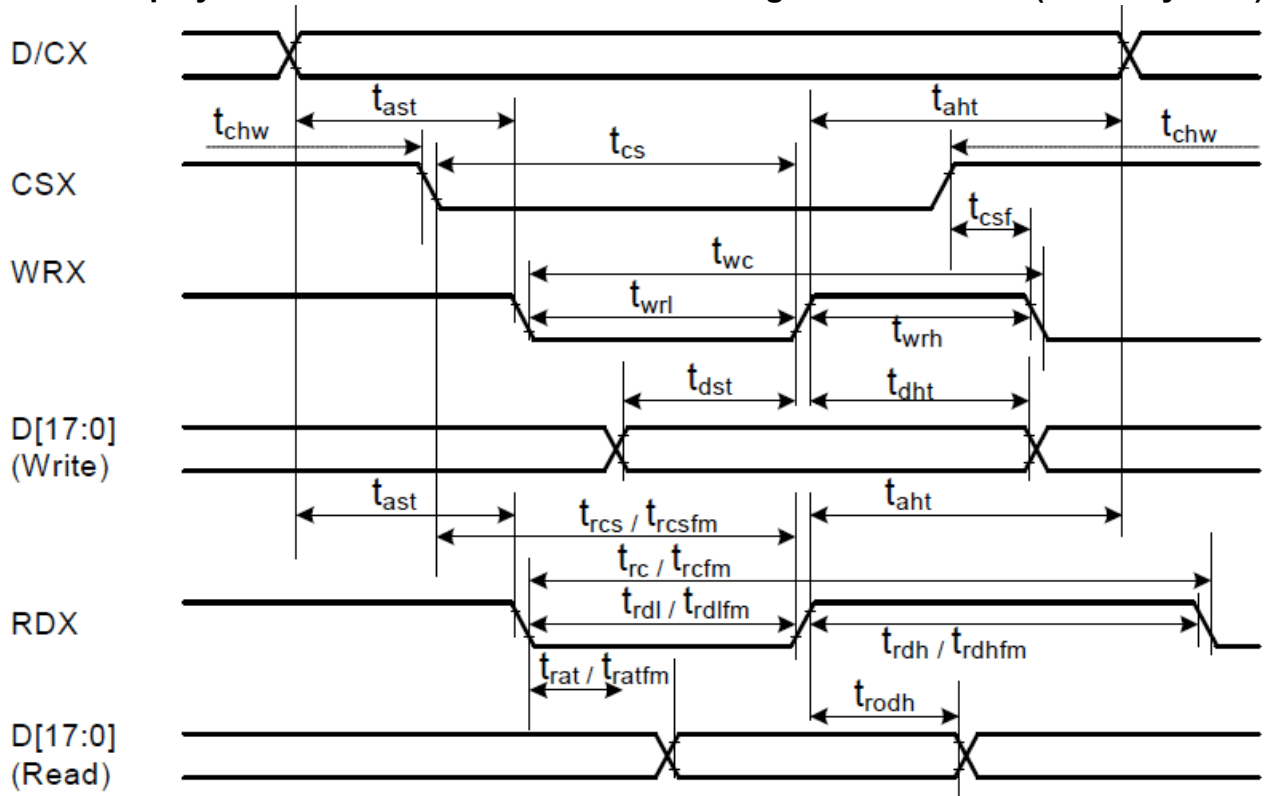
| Item | Symbol | MIN | TYP | MAX | Unit | Remark |
|-----------------|--------|-----|--------|-----|------|--------|
| Forward current | IF | - | 60 | - | mA | |
| Forward voltage | VF | - | 3.0 | - | V | |
| LED life time | - | - | 50,000 | - | Hrs | Note |

Note : The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL =60mA. The LED lifetime could be decreased if operating IL is larger than 60mA.



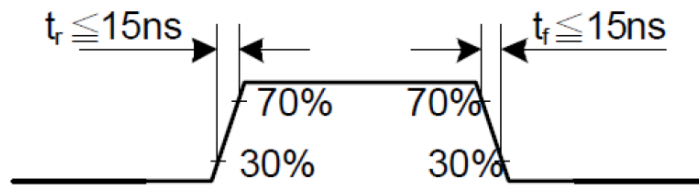
8. Command/AC Timing

8.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-I system)

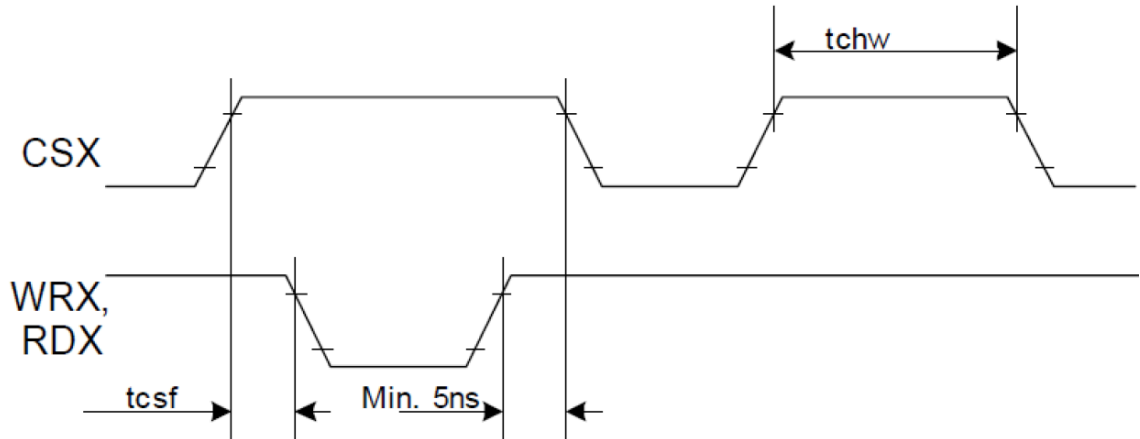


| Signal | Symbol | Parameter | Min. | Max. | Unit | Description |
|--|--------|------------------------------------|------|------|------|---|
| DCX | tast | Address setup time | 0 | - | ns | |
| | taht | Address hold time (Write/Read) | 0 | - | ns | |
| CSX | tchw | CSX "H" pulse width | 0 | - | ns | |
| | tcs | Chip Select setup time (Write) | 15 | - | ns | |
| | trcs | Chip Select setup time (Read ID) | 45 | - | ns | |
| | trcsfm | Chip Select setup time (Read FM) | 355 | - | ns | |
| | tcsf | Chip Select Wait time (Write/Read) | 10 | - | ns | |
| WRX | twc | Write cycle | 66 | - | ns | |
| | twrh | Write Control pulse H duration | 15 | - | ns | |
| | twrl | Write Control pulse L duration | 15 | - | ns | |
| RDX(FM) | trcfm | Read Cycle (FM) | 450 | - | ns | |
| | trdhfm | Read Control H duration (FM) | 90 | - | ns | |
| | trdlfm | Read Control L duration (FM) | 355 | - | ns | |
| RDX(ID) | trc | Read cycle (ID) | 160 | - | ns | |
| | trdh | Read Control pulse H duration | 90 | - | ns | |
| | trdl | Read Control pulse L duration | 45 | - | ns | |
| D[17:0] D[15:0] D[8:0] D[7:0] | tdst | Write data setup time | 10 | - | ns | For maximum CL=30pF For minimum CL=8pF |
| | tdht | Write data hold time | 10 | - | ns | |
| | trat | Read access time | - | 40 | ns | |
| | tratfm | Read access time | - | 340 | ns | |
| | trod | Read output disable time | 20 | 80 | ns | |

Note 1: Ta= -30 to 70°C, VDDI=1.65 to 3.3V, VCI=2.5 to 3.3V, VSS=0V.

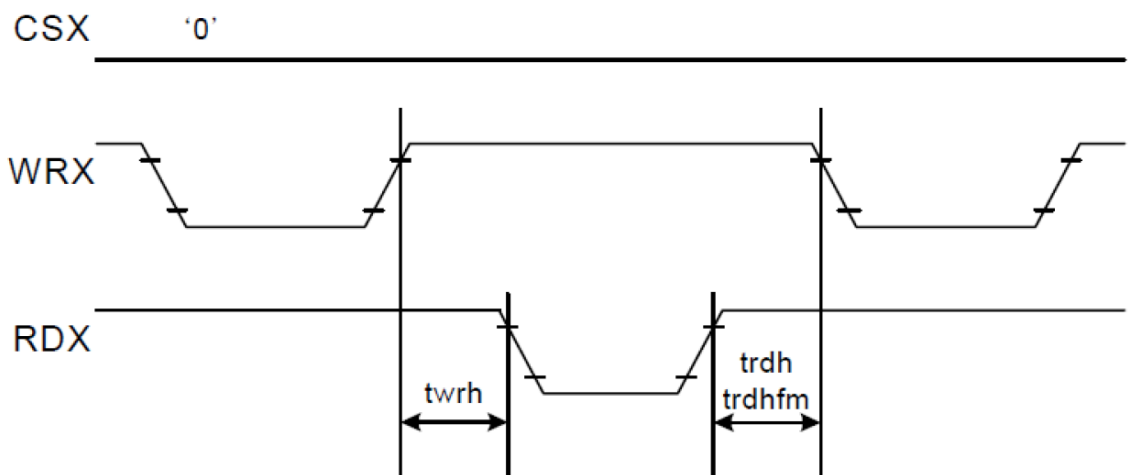


CSX timings:



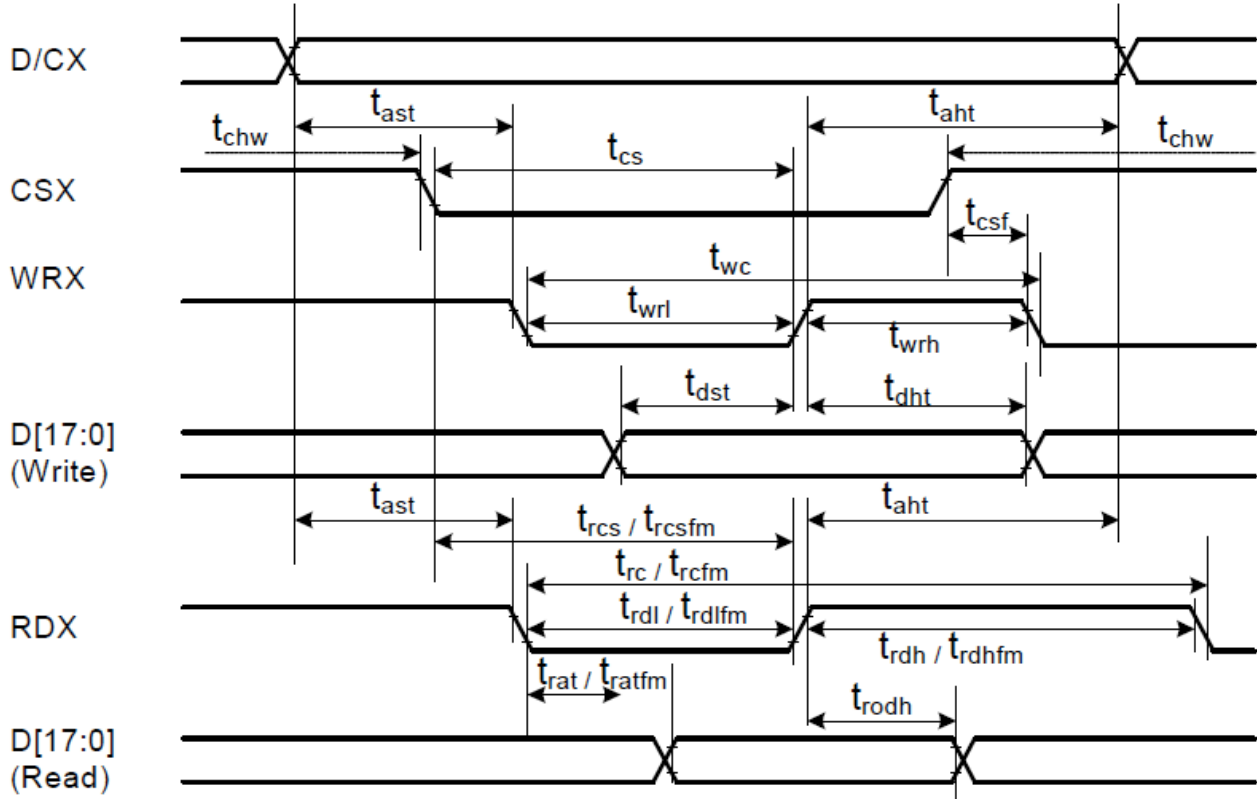
Note: Logic high and low levels are specified as 30% and 70% of VDDI for input signals.

Write to read or read to write timings:



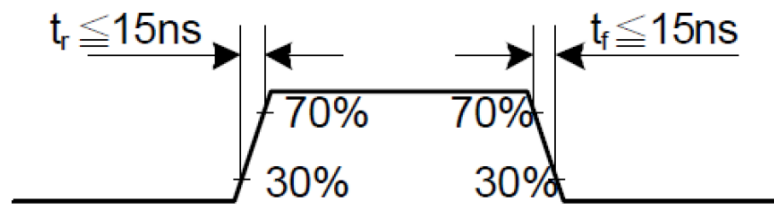
Note: Logic high and low levels are specified as 30% and 70% of VDDI for input signals.

8.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-II system)

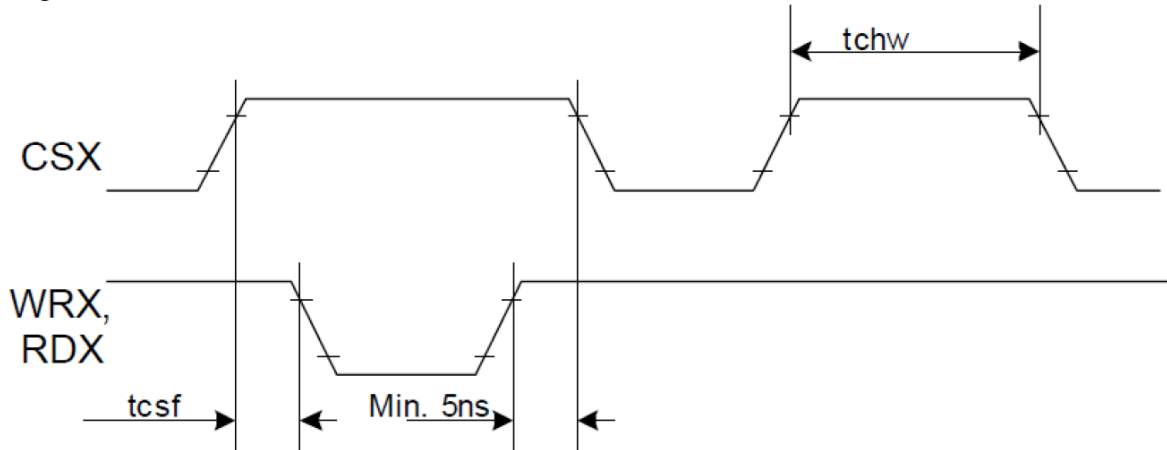


| Signal | Symbol | Parameter | Min. | Max. | Unit | Description |
|--|--------|------------------------------------|------|------|------|---|
| DCX | tast | Address setup time | 0 | - | ns | |
| | taht | Address hold time (Write/Read) | 0 | - | ns | |
| CSX | tchw | CSX "H" pulse width | 0 | - | ns | |
| | tcs | Chip Select setup time (Write) | 15 | - | ns | |
| | trcs | Chip Select setup time (Read ID) | 45 | - | ns | |
| | trcsfm | Chip Select setup time (Read FM) | 355 | - | ns | |
| | tcsf | Chip Select Wait time (Write/Read) | 10 | - | ns | |
| WRX | twc | Write cycle | 66 | - | ns | |
| | twrh | Write Control pulse H duration | 15 | - | ns | |
| | twrl | Write Control pulse L duration | 15 | - | ns | |
| RDX(FM) | trcfm | Read Cycle (FM) | 450 | - | ns | |
| | trdhfm | Read Control H duration (FM) | 90 | - | ns | |
| | trdlfm | Read Control L duration (FM) | 355 | - | ns | |
| RDX(ID) | trc | Read cycle (ID) | 160 | - | ns | |
| | trdh | Read Control pulse H duration | 90 | - | ns | |
| | trdl | Read Control pulse L duration | 45 | - | ns | |
| D[17:0] D[17:0]&D[8:1] D[17:10] D[17:9] | tdst | Write data setup time | 10 | - | ns | For maximum CL=30pF For minimum CL=8pF |
| | tdht | Write data hold time | 10 | - | ns | |
| | trat | Read access time | - | 40 | ns | |
| | tratfm | Read access time | - | 340 | ns | |
| | trod | Read output disable time | 20 | 80 | ns | |

Note 1: Ta= -30 to 70°C, VDDI=1.65 to 3.3V, VCI=2.5 to 3.3V, VSS=0V.

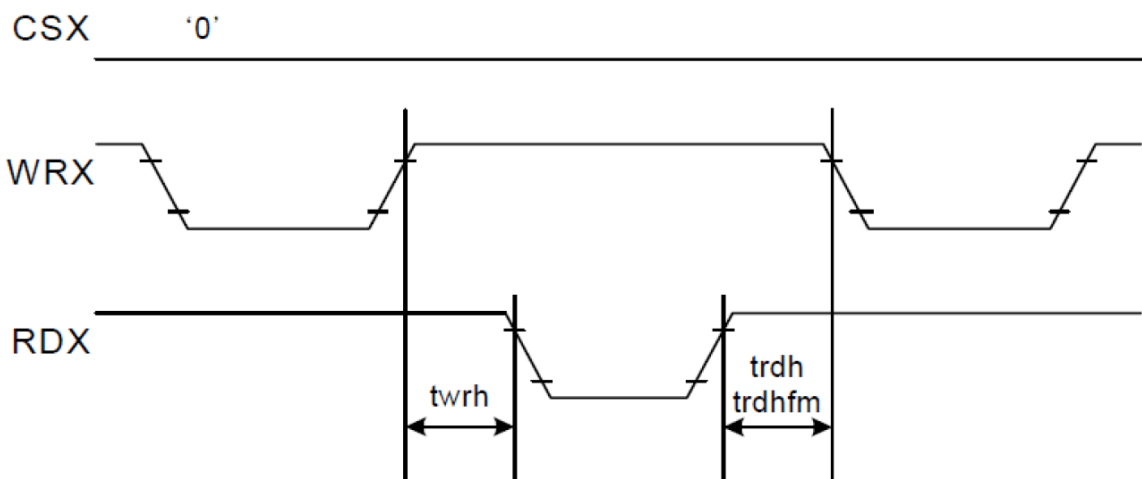


CSX timings:



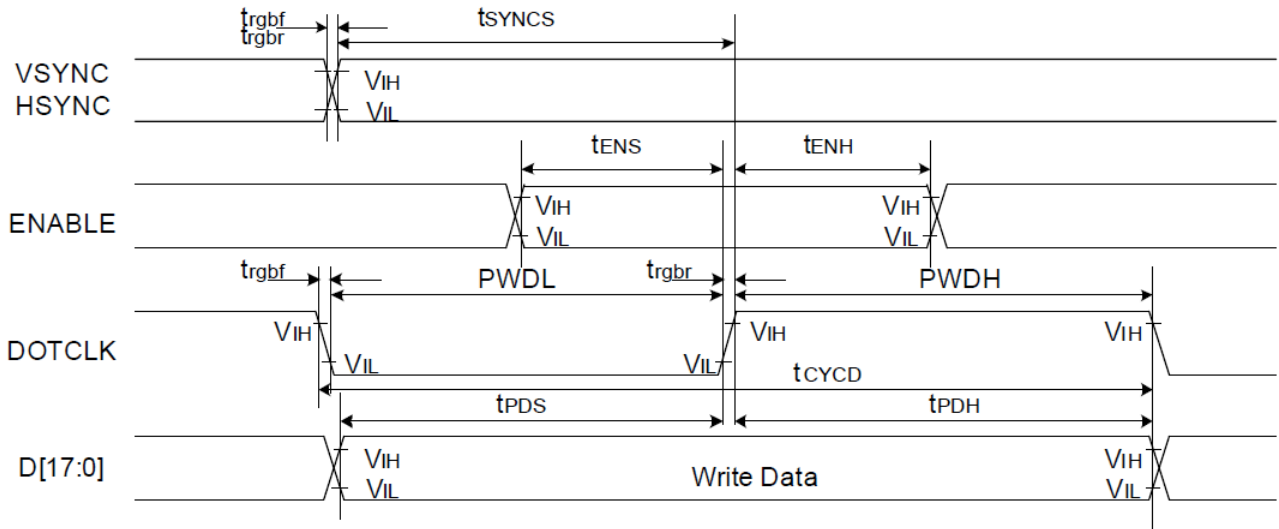
Note: Logic high and low levels are specified as 30% and 70% of VDDI for input signals.

Write to read to read to write timings:



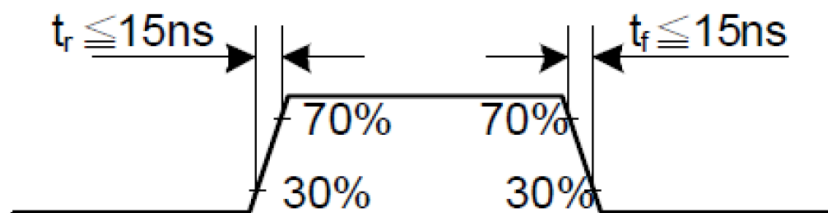
Note: Logic high and low levels are specified as 30% and 70% of VDDI for input signals.

8.3 Parallel 18/16/6-bit RGB Interface Timing Characteristics



| Signal | Symbol | Parameter | Min. | Max. | Unit | Description | |
|-----------------|--------------|-------------------------------------|------|------|------|----------------------------------|------------------------------|
| VSYNC/ HSYNC | tsynCS | VSYNC/HSYNC setup time | 15 | - | ns | 18/16-bit bus RGB interface mode | |
| | tsynCH | VSYNC/HSYNC hold time | 15 | - | ns | | |
| DE | tENS | DE setup time | 15 | - | ns | | |
| | tENH | DE hold time | 15 | - | ns | | |
| D[17:0] | tPOS | Data setup time | 15 | - | ns | | |
| | tPDH | Data hold time | 15 | - | ns | | |
| DOTCLK | PWDH | DOTCLK high-level period | 15 | - | ns | | |
| | PWDL | DOTCLK low-level period | 15 | - | ns | | |
| | tcycD | DOTCLK cycle time | 100 | - | ns | | |
| | trgbr, trgbf | DOTCLK, HSYNC, VSYNC rise/fall time | - | 15 | ns | | |
| VSYNC/ HSYNC | tsynCS | VSYNC/HSYNC setup time | 15 | - | ns | | 6-bit bus RGB interface mode |
| | tsynCH | VSYNC/HSYNC hold time | 15 | - | ns | | |
| DE | tENS | DE setup time | 15 | - | ns | | |
| | tENH | DE hold time | 15 | - | ns | | |
| D[17:0] | tPOS | Data setup time | 15 | - | ns | | |
| | tPDH | Data hold time | 15 | - | ns | | |
| DOTCLK | PWDH | DOTCLK high-level period | 15 | - | ns | | |
| | PWDL | DOTCLK low-level period | 15 | - | ns | | |
| | tcycD | DOTCLK cycle time | 50 | - | ns | | |
| | trgbr, trgbf | DOTCLK, HSYNC, VSYNC rise/fall time | - | 15 | ns | | |

Note 1: Ta= -30 to 70°C, VDDI=1.65 to 3.3V, VCI=2.5 to 3.3V, AGND=VSS=0V.



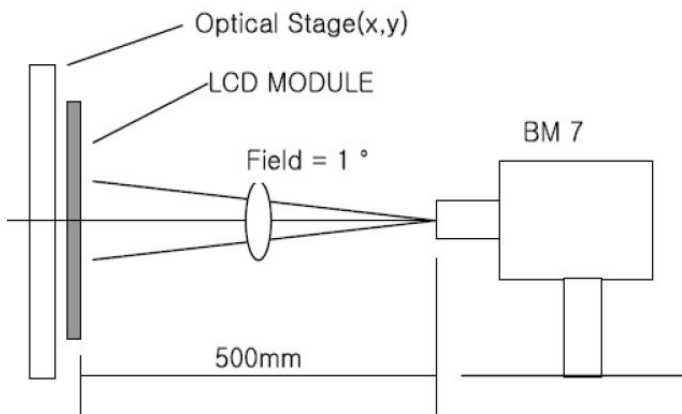
9. Optical Specification

| Item | Symbol | Condition | MIN | TYP | MAX | Unit | Remark |
|----------------|------------|------------------|------|------|-----|-------------------|-----------|
| Contrast ratio | CR | $\theta=0^\circ$ | 300 | 500 | - | | Note 1, 2 |
| Response time | Tr | 25°C | - | 10 | - | ms | Note 1, 3 |
| | Tf | | - | 10 | - | | |
| View angles | ΘT | CR ≥ 10 | - | 55 | - | Degree | Note 4 |
| | ΘB | | - | 65 | - | | |
| | ΘL | | - | 65 | - | | |
| | ΘR | | - | 65 | - | | |
| Chromaticity | White | x | - | 0.28 | - | Note 1, 5 | |
| | | y | - | 0.33 | - | | |
| | Red | x | - | 0.51 | - | | |
| | | y | - | 0.34 | - | | |
| | Green | x | - | 0.31 | - | | |
| | | y | - | 0.56 | - | | |
| Blue | x | - | 0.15 | - | | | |
| | y | - | 0.14 | - | | | |
| NTSC Ratio | S | | 50 | 60 | | % | Note 1, 5 |
| Luminance | L | | 250 | 330 | - | cd/m ² | Note 1, 6 |
| Uniformity | U | | - | 80 | - | % | Note 1, 7 |

Note 1: Definition of optical measurement system.

Temperature = 25°C (±3°C)

LED back-light: ON, Environment brightness < 150 lx

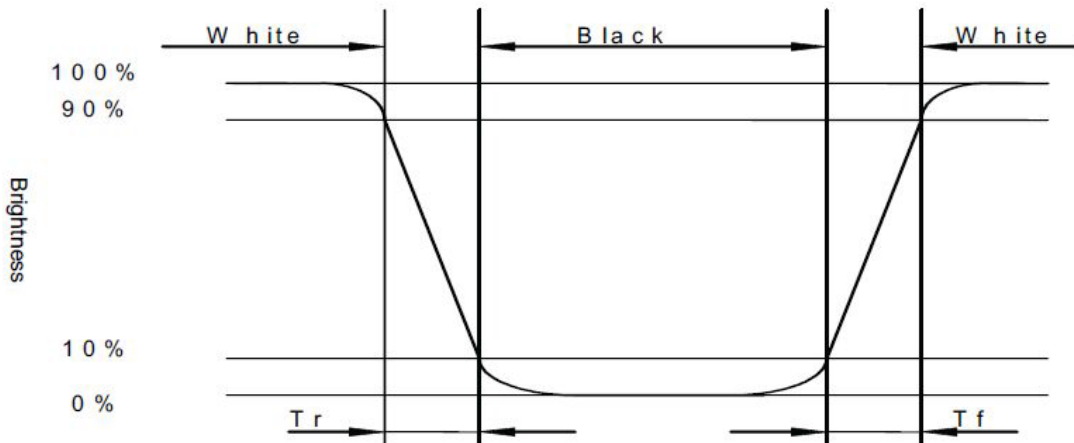


Note 2: Contrast ratio is defined as follow:

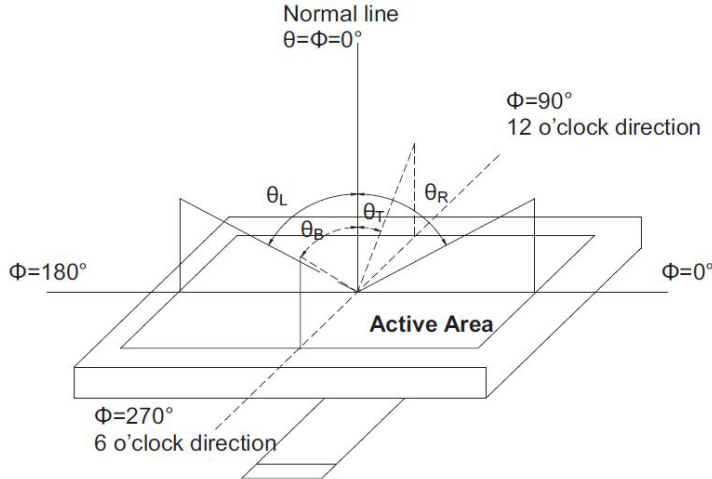
$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

Note 3: Response time is defined as follow:

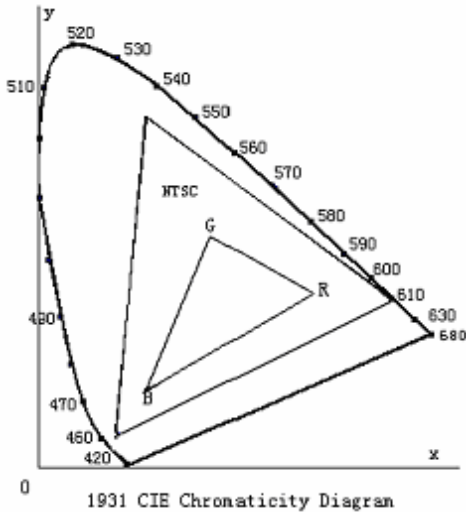
Response time is the time required for the display to transition from black to white (Rise time, Tr) and from white to black (Decay Time, Tf).



Note 4: Viewing angle range is defined as follow:
Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow (CIE1931)
Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels “White” at the center of display area on optimum contrast.

Note 7: Luminance Uniformity is defined as follow:

Active area is divided into 9 measuring areas (Refer Fig.2). Every measuring point is placed at the center of each measuring area.

$$\text{Uniformity (U)} = \frac{\text{Minimum Luminance(brightness) in 9 points}}{\text{Maximum Luminance(brightness) in 9 points}}$$

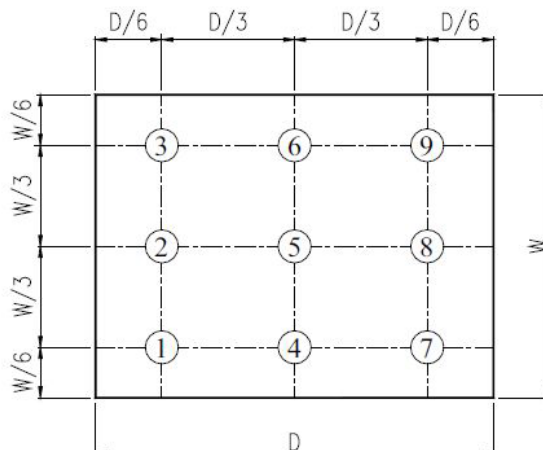


Fig. 2 Definition of uniformity

10. Environmental / Reliability Tests

| No | Test Item | Condition | Judgment Criteria |
|----|-----------------------------------|---|---|
| 1 | High Temp Operation | Ta=+70°C, 96hrs | Per table below |
| 2 | Low Temp Operation | Ta=-20°C, 96hrs | Per table below |
| 3 | High Temp Storage | Ta=+80°C, 96hrs | Per table below |
| 4 | Low Temp Storage | Ta=-30°C, 96hrs | Per table below |
| 5 | High Temp & High Humidity Storage | Ta=+60°C, 90% RH, 96hrs | Per table below (polarizer discoloration is excluded) |
| 6 | Thermal Shock (Non-operation) | -30°C 30 min~+70°C 30 min, Change time: 5min, 10 Cycles | Per table below |
| 7 | ESD (Operation) | C=150pF, R=330Ω, 5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times; | Per table below |
| 8 | Vibration (Non-operation) | Frequency range: 10~55Hz, Stroke: 1.5mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. | Per table below |
| 9 | Shock (Non-operation) | 60G 6ms, ±X,±Y,±Z 3times, for each direction | Per table below |
| 10 | Package Drop Test | Height: 80cm, 1 corner, 3 edges, 6 surfaces | Per table below |

| Inspection | Criterion (after test) |
|------------------------|---|
| Appearance | No crack on the FPC, on the LCD panel |
| Alignment of LCD panel | No bubbles in the LCD panel No other defects of alignment in active area |
| Electrical current | Within device specifications |
| Function / Display | No broken circuit, no short circuit or no black line No other defects of display |

11. Precautions for Use of LCD Modules

11.1 Safety

The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

- The LCD and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
- Do not handle the product by holding the flexible pattern portion in order to assure the reliability.
- Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
- Provide a space so that the panel does not come into contact with other components.
- To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
- Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
- Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.

- h. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static electricity

- a. Ground soldering iron tips, tools and testers when they are in operation.
- b. Ground your body when handling the products.
- c. Power on the LCD module before applying the voltage to the input terminals.
- d. Do not apply voltage which exceeds the absolute maximum rating.
- e. Store the products in an anti-electrostatic bag or container.

11.4 Storage

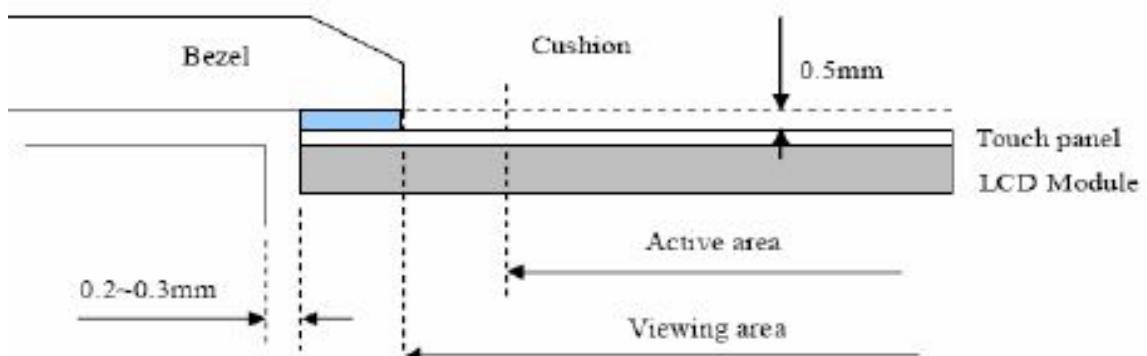
- a. Store the products in a dark place at $+25^{\circ}\text{C}\pm 10^{\circ}\text{C}$ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
- b. Storage in a clean environment, free from dust, active gas, and solvent.

10.5 Cleaning

- a. Do not wipe the touch panel with dry cloth, as it may cause scratch.
- b. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

- a. Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.
- b. In order to make the display assembly stable and firm, Displaytech recommends to design some supporting at the display backside, especially for the display with tape-attached touch panel, such supporting is important and essential, or else, the display may drop-off from front after some period of time.
- c. Do not display the fixed pattern for a long time because it may develop image sticking due to the LCD structure. If the screen is displayed with fixed pattern, use a screen saver.



X-ON Electronics

Largest Supplier of Electrical and Electronic Components

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