

# DP2101W

## DP2101W P-Channel Enhancement Mode Field Effect Transistor

### General description

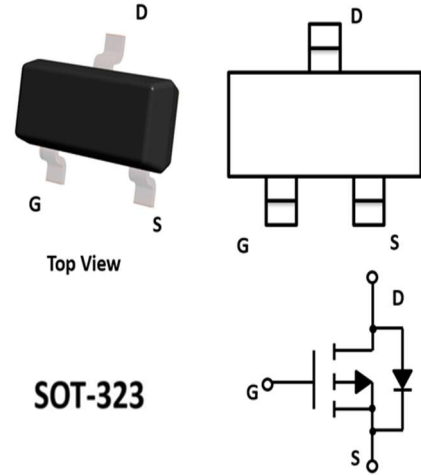
P-Channel Enhancement Mode Field Effect Transistor

#### Features:

- $V_{DS} : -20V$
- $I_D : -2.0A$
- $R_{DS(ON)}$ ( at  $V_{GS}=-4.5V$ )  $< 120$  mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=-2.5V$ )  $< 150$  mohm
- Trench Power LV MOSFET technology
- Low  $R_{DS(ON)}$
- Low Gate Charge

#### Applications

- Video monitor
- Power management



SOT-323

#### Device Marking Code:

Device Type	Device Marking
DP2101W	TS1

### Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	$V_{DS}$	-20	V
Gate-source Voltage	$V_{GS}$	$\pm 10$	V
Drain Current	$I_D$	$T_A=25^\circ\text{C}$ @ Steady State	-2
		$T_A=70^\circ\text{C}$ @ Steady State	-1.6
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	-8	A
Total Power Dissipation @ $T_A=25^\circ\text{C}$	$P_D$	0.7	W
Thermal Resistance Junction-to-Ambient <sup>B</sup>	$R_{\theta JA}$	178	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

## Electrical Characteristics ( $T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-20V, V_{GS}=0V, T_C=25^\circ\text{C}$			-1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 10V, V_{DS}=0V$			$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4	-0.62	-1.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-1.5A$		90	120	m $\Omega$
		$V_{GS}=-2.5V, I_D=-1.5A$		115	150	
Diode Forward Voltage	$V_{SD}$	$I_S=-2A, V_{GS}=0V$		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	$I_S$				-2	A
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=-10V, V_{GS}=0V, f=1\text{MHz}$		290		pF
Output Capacitance	$C_{oss}$			47		
Reverse Transfer Capacitance	$C_{rss}$			29		
<b>Switching Parameters</b>						
Total Gate Charge	$Q_g$	$V_{GS}=-4.5V, V_{DS}=-10V, I_D=-2A$		3.9		nC
Gate Source Charge	$Q_{gs}$			0.7		
Gate Drain Charge	$Q_{gd}$			0.9		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=-4.5V, V_{DD}=-10V, I_D=-1A, R_{GEN}=2.5\Omega$		12		ns
Turn-on Rise Time	$t_r$			54		
Turn-off Delay Time	$t_{D(off)}$			15		
Turn-off Fall Time	$t_f$			9		

A. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ .

B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

## Typical Performance Characteristics

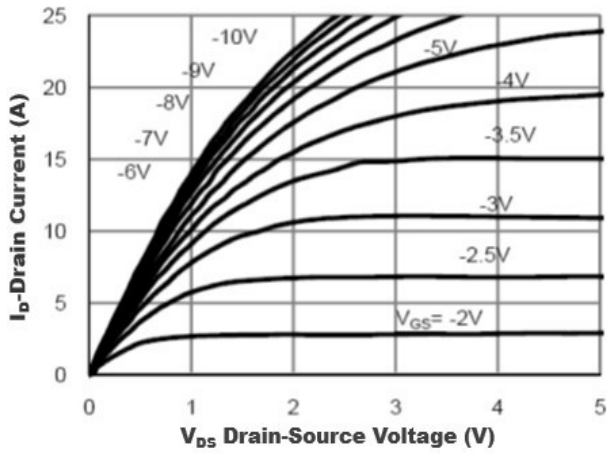


Figure1. Output Characteristics

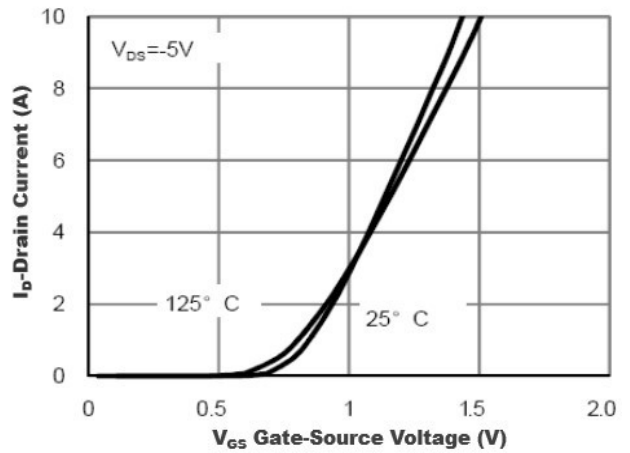


Figure2. Transfer Characteristics

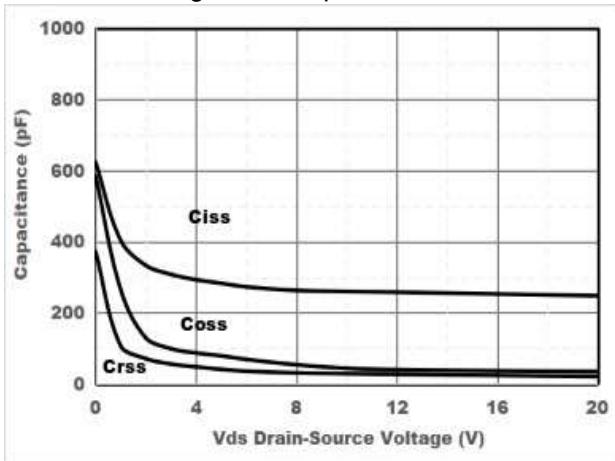


Figure3. Capacitance Characteristics

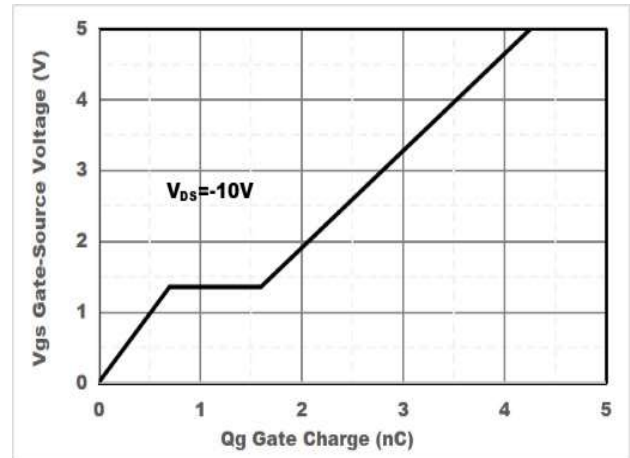


Figure4. Gate Charge

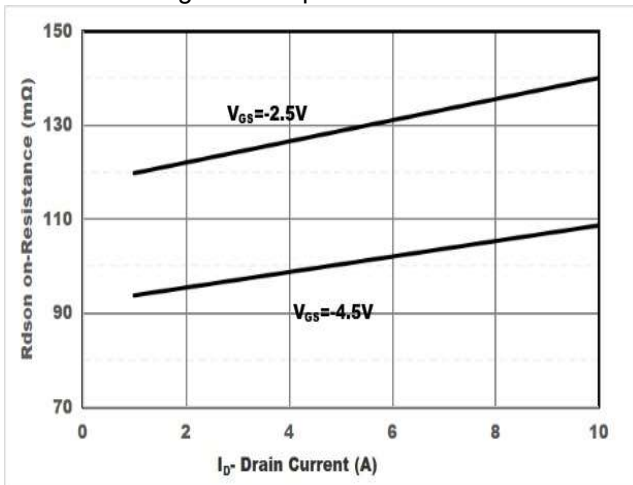


Figure5. Drain-Source on Resistance

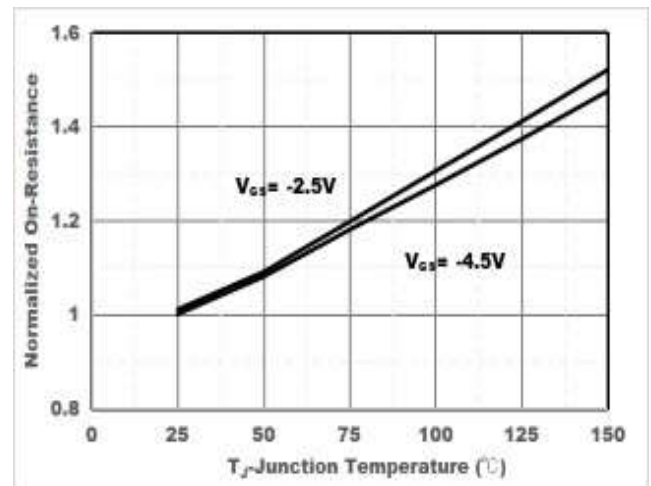
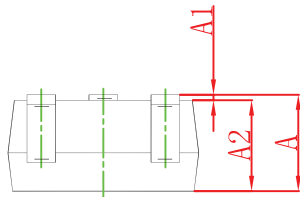
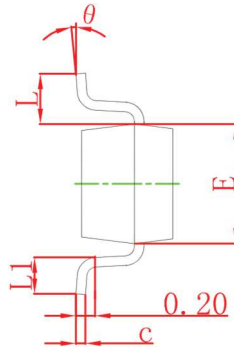
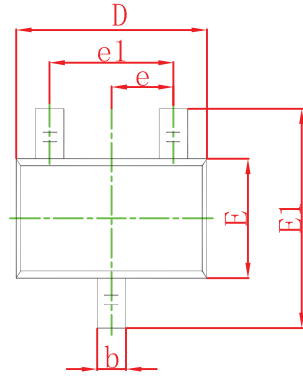
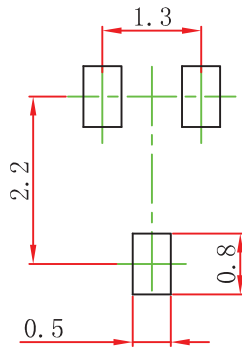


Figure6. Drain-Source on Resistance

## SOT-323 Package Outline



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.200	0.400	0.008	0.016
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0.055
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
	0°	8°	0°	8°



**Note:**

1. Controlling dimension: in millimeters.
2. General tolerance: ±0.05mm.
3. The pad layout is for reference purposes only.

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