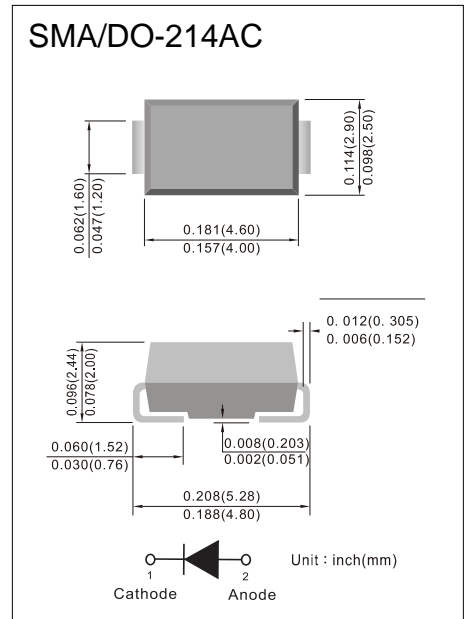


■ Features

- Glass passivated junction chip
- Ideal for automated placement
- Fast switching for high efficiency
- Comply with RoHS standard, halogen-free

■ Mechanical Data

- package:SMA/DO-214AC
- Polarity: Indicated by cathode band
- Epoxy: UL 94V-0 rate flame retardant
- Mounting Position : Any



■ Maximum Ratings And Electrical Characteristics($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	RS1A	RS1B	RS1D	RS1G	RS1J	RS1K	RS1M	UNIT
Maximum repetitive peak reverse voltage	V_{RRM}	50	100	200	400	600	800	1000	V
Maximum RMS voltage	V_{RMS}	35	70	140	280	420	560	700	V
Maximum DC blocking voltage	V_{DC}	50	100	200	400	600	800	1000	V
Maximum average forward rectified current	$I_{F(AV)}$	1							A
Peak forward surge current, 8.3 ms single half sine-wave superimposed on rated load	I_{FSM}	30							A
Maximum instantaneous forward voltage (Note 1) @ 1 A	V_F	1.3							V
Maximum reverse current @ rated V_R $T_J=25^{\circ}\text{C}$ $T_J=125^{\circ}\text{C}$	I_R	5 50							μA
Maximum reverse recovery time (Note 2)	t_{rr}	150			250	500		ns	
Typical junction capacitance (Note 3)	C_J	10							pF
Typical thermal resistance	$R_{\theta JC}$ $R_{\theta JA}$	32 105							$^{\circ}\text{C/W}$
Operating junction temperature range	T_J	- 55 to +150							$^{\circ}\text{C}$
Storage temperature range	T_{STG}	- 55 to +150							$^{\circ}\text{C}$

Note 1: Pulse test with $PW=300\mu\text{s}$, 1% duty cycle

Note 2: Reverse Recovery Test Conditions: $I_F=0.5\text{A}$, $I_R=1.0\text{A}$, $I_{RR}=0.25\text{A}$

Note 3: Measured at 1 MHz and Applied $V_R=4.0$ Volts



■ Ratings And Characteristics Curves($T_A=25^{\circ}\text{C}$ unless otherwise noted)

FIG.1 FORWARD CURRENT DERATING CURVE

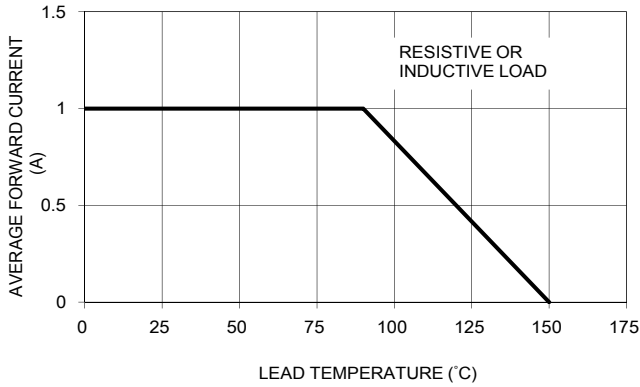


FIG. 2 TYPICAL REVERSE CHARACTERISTICS

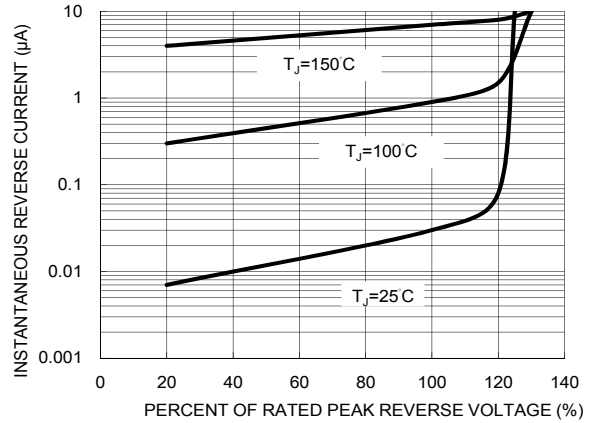


FIG. 3 MAXIMUM NON-REPETITIVE FORWARD SURGE CURRENT

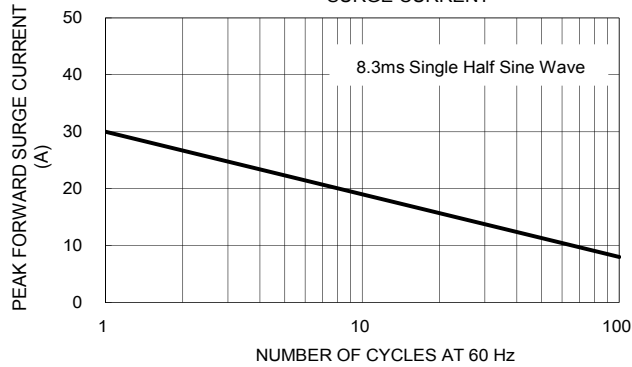


FIG. 4 TYPICAL FORWARD CHARACTERISTICS

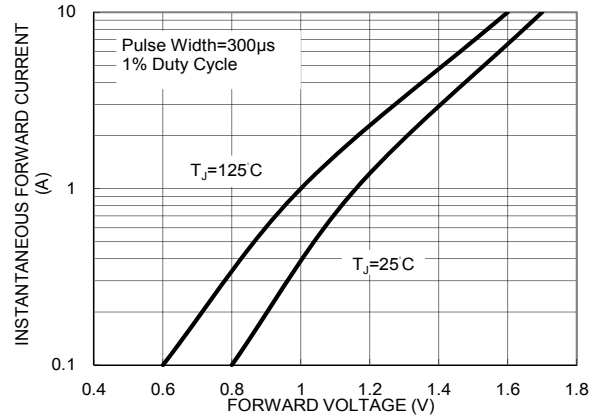


FIG. 5 TYPICAL JUNCTION CAPACITANCE

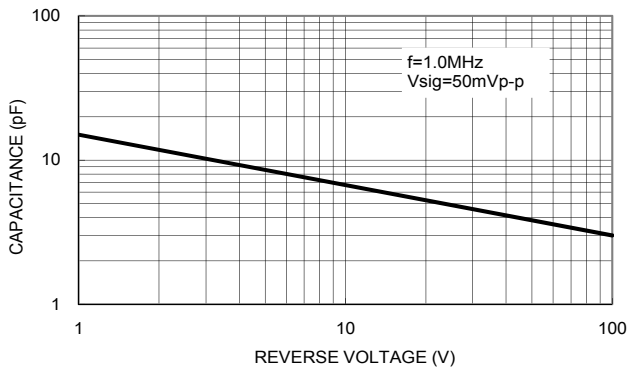
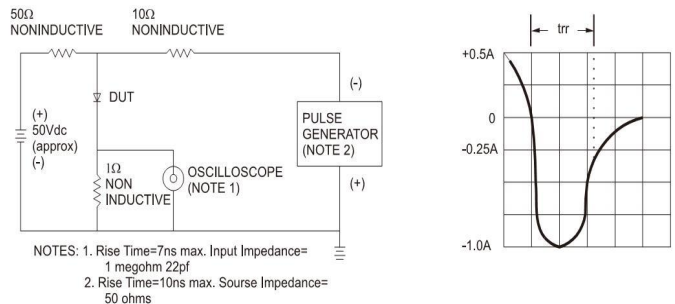


FIG.6- REVERSE RECOVERY TIME CHARACTERISTIC AND TEST CIRCUIT DIAGRAM



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