REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
E	Added changes in accordance with NOR 5962-R085-93	93-03-16	M. A. Frye
F	Added device types 45, 46, and 47. Removed CAGE code 34168 for case outline 8, and added cage code 34168 for case outline 9. Editorial changes throughout.	95-11-14	M. A. Frye
G	Added device types 48-68. ICC1 changes for device types 18, 19, 46, and 47. Updated boilerplate. glg	98-02-20	Raymond Monnin
H	Updated boilerplate paragraphs as part of a 5 year review. ksr	05-05-18	Raymond Monnin
J	Updated boilerplate paragraphs as part of a 5 year review. ksr	10-11-05	Charles F. Saffle

REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J						
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48						
REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS																	
REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
90-10-29

REVISION LEVEL
J

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME

COLUMBUS, OHIO 43218-3990

http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 8K x 8 STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON

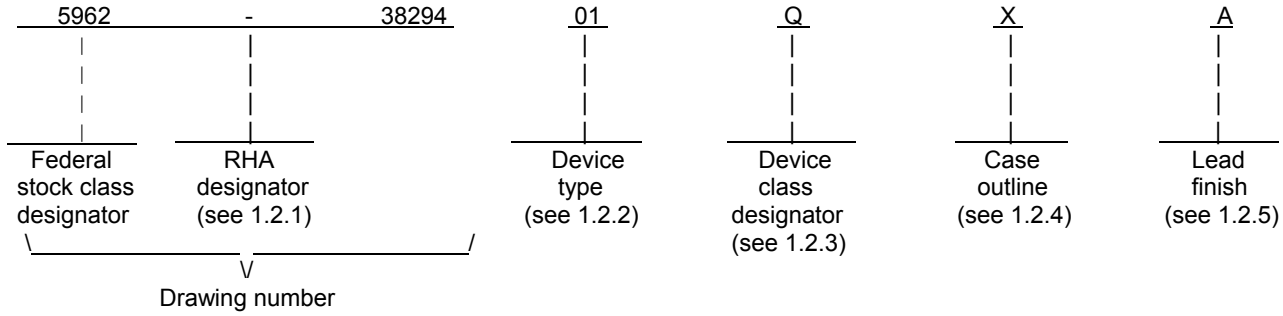
SIZE	CAGE CODE	
A	67268	**5962-38294**

SHEET 1 OF 48

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Data retention	Access time
01			No	150 ns
02			Yes	120 ns
03			No	120 ns
04			Yes	100 ns
05			No	100 ns
06			Yes	70 ns
07			No	70 ns
08			Yes	55 ns
09			No	55 ns
10		8K x 8 CMOS SRAM	Yes	45 ns
11			No	45 ns
12			Yes	35 ns
13			No	35 ns
14			Yes	25 ns
15			No	25 ns
16			Yes	20 ns
17			No	20 ns
18			Yes	15 ns
19			No	15 ns
20			Yes	70 ns
21			No	70 ns
22			Yes	55 ns
23			No	55 ns
24			Yes	45 ns
25			No	45 ns
26			Yes	35 ns
27			No	35 ns
28			Yes	25 ns
29			No	25 ns
30			No	20 ns
31			Yes	100 ns
32			Yes	70 ns
33			Yes	55 ns
34			Yes	45 ns

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 and QML-38535.

Device type	Generic number 1/	Circuit function	Data retention	Access time
35			Yes	85 ns
36			Yes	70 ns
37			Yes	55 ns
38			Yes	120 ns
39			Yes	70 ns
40		8K x 8 CMOS SRAM	Yes	120 ns
41			Yes	70 ns
42			Yes	55 ns
43			Yes	55 ns
44			No	55 ns
45			Yes	120 ns
46			Yes	12 ns
47			No	12 ns
48			No	70 ns
49			Yes	55 ns
50			No	55 ns
51			Yes	45 ns
52			No	45 ns
53			Yes	35 ns
54			No	35 ns
55			Yes	25 ns
56			No	25 ns
57			Yes	20 ns
58			No	20 ns
59			No	70 ns
60			Yes	55 ns
61			No	55 ns
62			Yes	45 ns
63			No	45 ns
64			Yes	35 ns
65			No	35 ns
66			Yes	25 ns
67			No	25 ns
68			No	20 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Y	CQCC1-N32	32	Rectangular chip carrier
Z	CDIP3-T28 or GDIP4-T28	28	Dual-in-line
U	CQCC4-N28	28	Rectangular chip carrier
T	GDFP2-F28	28	Flat pack
M	CDFP4-F28	28	Flat pack
N	See figure 1	28	Flat pack
9	See figure 1	36	Flat pack
8	See figure 1	36	Flat pack

1/ See footnote 1/, page 2.

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} +0.5 V dc 4/
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} +0.5 V dc 4/
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases X, Y, Z, U, T, and M	See MIL-STD-1835
Case N	10°C/W 5/
Case 9	2.0°C/W 5/
Case 8	3.3°C/W 5/
Output voltage applied in high-Z state	-0.5 V dc to V_{CC}+0.5 V dc
Maximum power dissipation, (P_D)	1.0 W
Maximum junction temperature (T_J)	+150°C 6/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Supply voltage (V_{SS})	0.0 V dc
High level input voltage range (V_{IH}):	
Device types 1-39,46-68,42,44 (TTL levels)	-2.2 V dc to V_{CC} + 0.5 V dc
Device types 40,41,43,45 (CMOS levels)	0.8 x V_{CC} to V_{CC} + 0.5 V dc
Low level input voltage range (V_{IL})	
Device types 1-39,46-68,42,44 (TTL levels)	-0.5 V dc to 0.8 V dc
Device types 40,41,43,45 (CMOS levels)	-0.5 V dc to 0.2 x V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ All voltages referenced to V_{SS} (V_{SS} = ground) unless otherwise specified.

4/ Negative undershoots to a minimum of -3.0 V are allowed with a maximum of 20 ns pulse width.

5/ When the thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 6 .

3.2.5 Functional tests. Various functional tests used to test this device are contained in appendix A herein. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.2.6 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in Table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime -VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

3.11 Substitution. Substitution data shall be as indicated in appendix B herein.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA V_{IL} = 0.8 V, V_{IH} = 2.2 V		1,2,3	01-39, 46-68, 42,44,	2.4		V
		V_{CC} = 4.5 V and 5.5 V, V_{IL} = 0.9 V and 1.1 V, V_{IH} = 3.6 V and 4.4 V, I_{OH} = -4.0 mA			40,41, 43,45	4.2		
			M,D,P,L,R,F, G,H	1 2/	3/	4/		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA V_{IL} = 0.8 V, V_{IH} = 2.2 V		1,2,3	01-39, 46-68, 42,44		0.4	V
		V_{CC} = 4.5 V and 5.5 V, V_{IL} = 0.9 V and 1.1 V, V_{IH} = 3.6 V and 4.4 V, I_{OL} = 8.0 mA			40,41, 43,45			
			M,D,P,L,R,F, G,H	1 2/	3/	4/		V
High level input current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V for pin being tested, all other pins not being tested at 0.0 V.		1,2,3	All		10	µA
			M,D,P,L,R,F, G,H	1 2/	3/	4/		µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.0 V for pin being tested, all other pins not being tested at 0.0 V.		1,2,3	All	-10		µA
			M,D,P,L,R,F, G,H	1 2/	3/	4/		µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
High impedance output leakage current	I_{OHZ}	V_{CC} = 5.5 V, V_O = 5.5 V V_{IL} = 0.0 V, V_{IH} = 5.0 V $V_{IH} \le \overline{OE} \le V_{CC}$		1,2,3	01-39, 46-68, 42,44,		10	µA
		V_{CC} = 4.5 V and 5.5 V, V_O = 5.5 V, V_{IL} = .5 V, $V_{IH} = V_{CC}$ - .5 V, $3.6\ V \le \overline{OE} \le 4.4\ V$			40,41, 43,45			
			M,D,P,L,R,F, G,H	1 2/	3/	4/		µA
Low impedance output leakage current	I_{OLZ}	V_{CC} = 5.5 V, V_O = 0.0 V V_{IL} = 0.0 V, V_{IH} = 5.0 V $V_{IH} \le \overline{OE} \le V_{CC}$		1,2,3	01-39, 46-68, 42,44,	-10		µA
		V_{CC} = 4.5 V and 5.5 V, V_O = 0.0 V, V_{IL} = .5 V, $V_{IH} = V_{CC}$ - .5 V, $3.6\ V \le \overline{OE} \le 4.4\ V$			40,41, 43,45			
			M,D,P,L,R,F, G,H	1 2/	3/	4/		µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA,		02,04, 31,38		60	
		$\overline{CE}_1$ = 0.8 V dc, f = $1/t_{AVAV}$,		01,03,05			
		$\overline{OE}$ = $\overline{WE}$ = CE_2 = 2.2 V dc				80	
				06,20,32		90	
				07,08,10, 21,22,24,			mA
			1,2,3	33,34		105	
				12,14,26, 28,39,42		110	
				09,11, 16,23,25		125	
				13,27		130	
				15,17, 29,30		135	
				48,49,51, 59,60,62		145	
				35,36		150	
				53,55,64, 66		155	
				50,52,56, 57,58,61, 63,67,68		160	
				18,19, 54,65		170	
				37,46,47		180	
		V_{CC} = 5.5 V, I_{OUT} = 0 mA,					
				40,45		60	
		$\overline{CE}_1$ = 1.1 V dc, f = $1/t_{AVAV}$,					
		$\overline{OE}$ = $\overline{WE}$ = CE_2 = 4.4 V dc		41,43		110	
		V_{CC} = 5.5 V, I_{OUT} = 0 mA,					
				44		200	
		$\overline{WE}$ = V_{CC}, f = 20 MHz					
		M,D,P,L,R,F, G,H	1 2/	3/	4/		mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Standby supply current TTL levels	I_{CC2}	V_{CC} = 5.5 V, f = 0, $\overline{CE}_1 = V_{IH}$, $CE_2 = V_{IL}$,		38-43, 45		500	µA
				35-37		10	
				02,04,06, 20,31,32		15	
		$\overline{OE}$ = $\overline{WE}$ = V_{IH}, all other inputs = V_{IL} or V_{IH}	1,2,3	01,03,05, 07,21,48, 59		20	mA
				08,10,12, 14,16,18, 22,24,26, 28,33,34, 46,47,49, 51,53,55, 57,60,62, 64,66		30	
				09,11,13, 15,17,19, 23,25,27, 29,30,50, 52,54,56, 58,61,63, 65,67,68		40	
		V_{CC} = 5.5 V, f = 0, $\overline{AS}$ = GND, all other inputs = 2.0 V		44		37.5	
		$\overline{CE_1}$=CE_2 = V_{CC}, all other inputs = 0.8 V				12	
		M,D,P,L,R,F,G,H	1 2/	3/		4/	mA
				35-37		15	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Standby supply current CMOS levels	I_{CC3}	V_{CC} = 5.5 V, f = 0		1,2,3	35-37		200	µA
					38-43, 45		500	
		$\overline{CE}_1 \ge V_{CC}$ - 0.5 V, all other inputs = 0.5 V or V_{CC} - 0.5 V			01,02, 04,06, 20,31, 32,46, 47		5	mA
					08,10,12, 14,16,18, 22,24,26, 28,33,34, 49,51,53, 55,57,60, 62,64,66		10	
					03,05,07, 21,48,59		15	
					09,11,13, 15,17,19, 23,25,27, 29,30,50, 52,54,56, 58,61,63, 65,67,68		20	
		V_{CC} = 5.5 V, f = 0						
		$CE_2 = \overline{AS}$ = GND all other inputs = V_{CC}			44		2	
			M,D,P,L,R,F,G,H	1 2/	3/		4/	mA
					35-37		3	
Data retention current	I_{CC4}	V_{CC} = 2.0 V, f = 0		1,2,3	31-37		75	µA
					02,04		200	
		$\overline{CE}_1 \ge V_{CC}$ - 0.2 V, all other inputs = 0.2 V or V_{CC} - 0.2 V			06,08,10, 12,14,16, 18,20,22, 24,26,28,			
					38-43, 45,46,49, 51,53,55, 57,60,62, 64,66		300	
			M,D,P,L,R,F,G,H	1 2/	3/		4/	µA
					35-37		3	mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Input capacitance 5/	C_{IN}	V_I = 0.0 V, T_A = +25°C, f = 1 MHz (see 4.4.1e)		4	All		15	pF
Output capacitance 5/	C_{OUT}	V_O = 0.0 V, T_A = +25°C, f = 1 MHz (see 4.4.1e)		4	All		20	pF
Functional tests 6/		V_{CC} = 4.5 V verify output V_O (see 4.4.1c)		7,8A,8B	All	L	H	V
			M,D,P,L,R,F, G,H	7 2/	3/	4/		V
Read cycle								
Read/Write cycle time	t_{AVAV}	See figures 4 and 5		9,10,11	01	150		ns
					02,03, 38,40, 45	120		
					04,05, 31	100		
					35	85		
					06,07,20, 21,32,36, 39,41,48, 59	70		
					08,09,22, 23,33,37, 42-44,49 50,60,61	55		
					10,11,24, 25,34,51, 52,62,63	45		
					12,13,26, 27,53,54, 64,65	35		
					14,15,28, 29,55,56, 66,67	25		
					16,17,30, 57,58,68	20		
					18,19,	15		
					46,47	12		
			M,D,P,L,R,F, G,H	9 2/	3/	4/		ns
Output hold time	t_{AVQX}			9,10,11	35-44, 45	5		ns
					01-13, 20-27, 31-34, 48-54, 59-65	3		
					46,47	2		
					14-19, 28-30, 55-58, 66-68	0		
			M,D,P,L,R,F, G,H	9 2/	3/	4/		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Read access time	t_{AVQV}	See figures 4 and 5	9,10,11	01		150	ns
				02,03		120	
				04,05,31		100	
				35		85	
				06,07,20, 21,32,36, 39,41,48, 59		70	
				08,09,22, 23,33,37, 38,40, 42-45,49 50,60,61		55	
				10,11,24, 25,34,51, 52,62,63		45	
				12,13,26, 27,53,54, 64,65		35	
				14,15,28, 29,55,56, 66,67		25	
				16,17,30, 57,58,68		20	
				18,19		15	
				46,47		12	
			M,D,P,L,R,F, G,H	9 2/	3/	4/	ns
$\overline{OE}$ controlled output enabled time 5/ 7/	t_{OLQX}		9,10,11	01-05, 31,44	5		ns
				06-30, 32-43, 45,46,47, 48-68	0		
			M,D,P,L,R,F, G,H	9 2/	3/	4/	ns
$\overline{OE}$ controlled output three-state time 5/ 7/	t_{OHQZ}		9,10,11	01		50	ns
				02-11, 20-25, 31-34, 48-52, 59-63		40	
				12,13,26, 27,53,54, 64,65		30	
				44		20	
				14-17, 28-30, 35-43,45 55-58, 66-68		15	
				18,19		10	
				46,47		7	
			M,D,P,L,R,F, G,H	9 2/	3/	4/	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device types	Limits Min	Limits Max	Unit
					01		70	
$\overline{OE}$ controlled output enabled time (read cycle 3)	t_{OLQV}	See figures 4 and 5		9,10,11	02,03		55	ns
					04,05, 31		45	
					06,07,20, 21,32,35, 48,59		30	
					08,09,22, 23,33,49, 50,60,61		25	
					10,11,24, 25,34,44, 51,52,62, 62,63,		20	
					12-17, 26-30, 36-43,45 53-58, 64-68		15	
					18,19		12	
					46,47		8	
			M,D,P,L,R,F, G,H	9 2/	3/		4/	ns
$\overline{CE}$ controlled output enable time	t_{ELQX}			9,10,11	01-43,45	0		ns
					48-68			
					44	5		
					46,47	2		
5/ 7/			M,D,P,L,R,F, G,H	9 2/	3/	4/		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
$\overline{CE}$ controlled output access time	t_{ELQV}	See figures 4 and 5	9,10,11	01		150	ns
				02,03		120	
				04,05 31		100	
				35		85	
				06,07,20, 21,32,36, 39,41,48, 59		70	
				08,09,22, 23,33,37, 38,40, 42-45, 49,50,60, 61		55	
				10,11,24, 25,34,51, 52,62,63		45	
				12,13,26, 27,53,54, 64,65		35	
				14,15,28, 29,55,56, 66,67		25	
				16,17,30 57,58,68		20	
				18,19		15	
				46,47		12	
		M,D,P,L,R,F, G,H	9 2/	3/		4/	ns
$\overline{CE}$ high to high Z 5/ 7/	t_{EHQZ}		9,10,11	01		50	ns
				02,03		40	
				04-07,20 21,31,32 48,59		35	
				08-11, 22-25, 33-35,44 49-52, 60-63		25	
				36-43, 45		20	
				12-17, 26-30, 53-58, 64-68		15	
				18,19		10	
				46,47		7	
		M,D,P,L,R,F, G,H	9 2/	3/		4/	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device types	Limits Min	Limits Max	Unit
Address setup time for write control	t_{AVWL} t_{AVEL}	See figures 4 and 5		9,10,11	01-43, 48-68, 45,46,47	0		ns
					44	10		
			M,D,P,L,R,F, G,H	9 2/	3/	4/		ns
$\overline{CE}$ low to write end	t_{ELWH}				38,40, 45	105		
					01	100		
					02,03	85		
					04,05, 31	80		
					35	65		
					06,07,20, 21,32,36, 39,41,48, 59	60		
				9,10,11	08,09,22, 23,33,37, 49,50,60, 61	50		ns
					42-44	45		
					10,11,24, 25,34,51, 52,62,63	40		
					12,13,26, 27,53,54, 64,65	30		
					14,15,28, 29,55,56, 66,67	20		
					16,17,30, 57,58,68	15		
					18,19	13		
					46,47	10		
			M,D,P,L,R,F, G,H	9 2/	3/	4/		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Address valid to end of write	t_{AVWH}	See figures 4 and 5		9,10,11	38,40,45	105		ns
					01	100		
					02,03	85		
					04,05,31	80		
					35	65		
					06,07,20,21,32,36,39,41,48,59	60		
					08,09,22,23,33,37,49,50,60,61	50		
					42-44	45		
					10,11,24,25,34,51,52,62,63	40		
					12,13,26,27,53,54,64,65	30		
					14,15,28,29,55,56,66,67	20		
					16,17,30,57,58,68	15		
					18,19	13		
					46,47	10		
			M,D,P,L,R,F,G,H	9 2/	3/	4/		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Write pulse width	t_{WLWH}	See figures 4 and 5		9,10,11	38,40,45	105		ns
					01	90		
					02,03	70		
					04-07,20,21,31,32,39,41,48,59	60		
					08,09,22,23,33,35,49,50,60,61	50		
					42,43	45		
					10,11,24,25,34,36,37,51,52,62,63	40		
					44	35		
					12,13,26,27,53,54,64,65	30		
					14,15,28,29,55,56,66,67	20		
					16,17,30,57,58,68	15		
					18,19	13		
					46,47	10		
			M,D,P,L,R,F,G,H	9 2/	3/	4/		ns
Write recovery time	t_{WHAV}			9,10,11	01-43,45,46,47,48-68	0		ns
					44	10		
			M,D,P,L,R,F,G,H	9 2/	3/	4/		ns
Chip disable to address change	t_{EHAX}			9,10,11	01-43,45,46,47,48-68	0		ns
					44	5		
			M,D,P,L,R,F,G,H	9 2/	3/	4/		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
$\overline{WE}$ high to low Z 5/ 7/	t_{WHQX}	See figures 4 and 5		9,10,11	01-45, 48-68	0		ns
					46,47	2		
			M,D,P,L,R,F, G,H	9 2/	3/	4/		ns
$\overline{WE}$ low to high Z	t_{WLQZ}			9,10,11	01		50	ns
					02,03		40	
					04-07,20		35	
					21,31,32, 48,59			
					08,09,22, 23,33,49, 50,60,61		30	
					10,11,24, 25,34,51, 52,62,63		25	
					44		20	
					12-15, 26-29, 35-43,45 53-56, 64,67,		15	
					16-19, 30,57,58, 68		10	
					46,47		7	
			M,D,P,L,R,F, G,H	9 2/	3/		4/	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Data setup time	t_{DVWH}	See figures 4 and 5		9,10,11	38,40, 45	105		ns
					01,39, 41	60		
					02-05, 31,35	50		
					42,43	45		
					36,37	40		
					06,07,20, 21,32,48, 59	35		
					08,09,22, 23,33,44, 49,50,60, 61	25		
					10,11,24, 25,34,51, 52,62,63	20		
					12-15, 26-29, 53-56, 64-67	15		
					16,17,30, 57,58,68	12		
					18,19	10		
					46,47	7		
			M,D,P,L,R,F, G,H	9 2/	3/	4/		ns
Data hold time	t_{WHDX}			9,10,11	01-13, 20-27, 31-34, 44, 48-54, 59-65,	5		ns
					14-19, 28-30, 35-43, 45,46,47 55-58, 66-68	0		
			M,D,P,L,R,F, G,H	9 2/	3/	4/		ns
Chip deselect to data retention time 5/	t_{CDR}			7,8A,8B	02,04,06, 08,10,12, 14,16,18, 20,22,24, 26,28, 31-43, 45,46,49, 51,53,55, 57,60,62, 64,66	0		ns
			M,D,P,L,R,F, G,H	7 2/	3/	4/		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Operation recovery time 5/	t_R	See figures 4 and 5		7,8A,8B	02,04,06, 08,10,12, 14,16,18, 20,22,24, 26,28, 31-43, 45,46,49, 51,53,55, 57,60,62, 64,66	t_{AVAV}		ns
			M,D,P,L,R,F, G,H	7 2/	3/	4/		ns
AC parameters only for device type 44 and 45 only								
$\overline{AS}$ address latch control access time	t_{LLQV}	See figures 4 and 5		9,10,11	44,45		65	ns
			M,D,P,L,R,F, G,H	9 2/	3/		4/	ns
Address valid to end of write	t_{LLWH}			9,10,11	44		45	ns
			M,D,P,L,R,F, G,H	9 2/	3/		4/	ns
$\overline{AS}$ address latch control setup to start of write	t_{LLWL}			9,10,11	44,45	10		ns
			M,D,P,L,R,F, G,H	9 2/	3/	4/		ns
$\overline{AS}$ address latch control hold after end of write	t_{WHLL}			9,10,11	44,45		0	ns
			M,D,P,L,R,F, G,H	9 2/	3/		4/	ns
$\overline{AS}$ address latch control setup to end of write	t_{LLEH}			9,10,11	44		45	ns
			M,D,P,L,R,F, G,H	9 2/	3/		4/	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ GND = 0 V $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{AS}$ address latch control setup to start of write	t_{LLEL}	See figures 4 and 5	9,10,11	44		5	ns
		M,D,P,L,R,F, G,H	9 2/	3/		4/	ns
$\overline{AS}$ address latch control hold after end of write	t_{EHLL}		9,10,11	44	5		ns
		M,D,P,L,R,F, G,H	9 2/	3/	4/		ns
Address setup to address latch	t_{AVLH}		9,10,11	44,45	15		ns
		M,D,P,L,R,F, G,H	9 2/	3/	4/		ns
Address hold after address latch	t_{LHAX}		9,10,11	44,45	10		ns
		M,D,P,L,R,F, G,H	9 2/	3/	4/		ns
Address latch width	t_{LLLH}		9,10,11	44,45	20		ns
		M,D,P,L,R,F, G,H	9 2/	3/	4/		ns
Chip enable hold after address latch	t_{LHEL}		9,10,11	44	0		ns
		M,D,P,L,R,F, G,H	9 2/	3/	4/		ns

1/ AC measurements assume transition time ≤ 5 ns, input levels are from ground to 3.0 V, and output load $C_L \ge 30$ pF except as noted on figure 5. Timing reference levels are 1.5 V. For devices 40, 41, and 43, input levels are $V_{IL} = 0.5$ V, $V_{IH} = V_{CC} - 0.5$ V.

2/ When performing postirradiation electrical measurements for any RHA level $T_A = +25°C$. Limits shown are guaranteed at $T_A = +25°C \pm 5°C$. The M, D, P, L, R, F, G, and H in the test condition column are the postirradiation limits for the device types specified in the device types column.

3/ Devices listed in 1.2.2 herein, that are to be marked with an RHA marking shall apply to all RHA levels unless otherwise specified.

4/ Preirradiation values for RHA marked devices shall also be the postirradiation values unless otherwise specified.

5/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table IA.

6/ Functional tests shall include the test table and other test patterns used for fault detection as approved by the qualifying activity. Outputs are measured at $V_{OL} < 1.5$ V, $V_{OH} > 1.5$ V. For devices 40, 41, and 43, outputs are measured at $V_{OL} < V_{CC} / 2$, $V_{OH} > V_{CC} / 2$.

7/ This parameter measured ±500 mV from steady-state V_{OL} or V_{OH}.

TABLE IB. Single event phenomena (SEP) test limits. 1/ 2/

Device type	T_A =temperature (± 10°C) 3/	Memory pattern	V_{CC} = 4.5 V		Bias voltage for latch-up test V_{CC} = 5.5 V (minimum); no latch-up; LET = 100 3/
			Effective threshold LET no upsets (Mev/(mg/cm^2)	Maximum device cross section (μm^2)	(minimum)
35	+125°C	All 1s	≥ 46	11.5	119
36	+125°C	All 1s	≥ 46	11.5	119
37	+125°C	All 1s	≥ 46	11.5	119
38	+125°C	Parity	≥ 35	48	119
39	+125°C	Parity	≥ 22	48	119
40	+125°C	Parity	≥ 35	48	119
41	+125°C	Parity	≥ 22	48	119
42	+125°C	Parity	≥ 22	48	119
43	+125°C	Parity	≥ 22	48	119
44	+125°C	4/	≥ 50	≤ 50	120
45	+125°C	Parity	≥ 35	45	119

1/ For SEP test conditions, see 4.4.4.2 herein.

2/ For QML product, technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Worst case temperature T_A = +125°C

4/ Testing shall be performed using checkerboard and checkerboard bar test patterns.

Case N

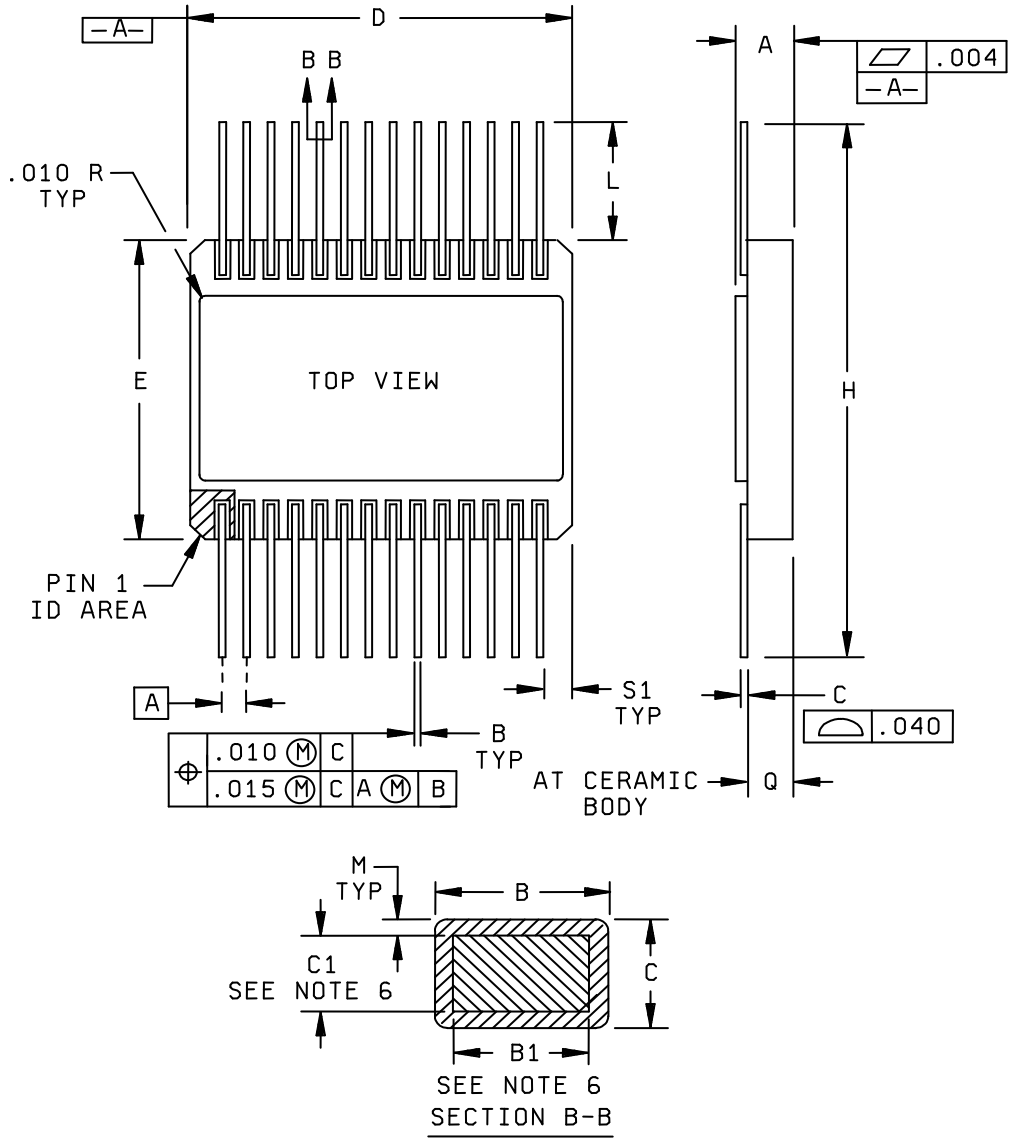


FIGURE 1. Case outlines.

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.110	---	2.79
B	.014	.021	0.36	0.53
B1	.014	.018	0.36	0.46
C	.006	.012	0.15	0.30
C1	.006	.009	0.15	0.23
D	.735	.765	18.67	19.43
E	.685	.715	17.40	18.16
e	.050 BSC		1.27 BSC	
H	---	1.480	---	37.59
L	.330	.400	8.38	---
M	---	.0015	---	0.038
Q	.070	.090	1.78	2.29
S1	.005	---	0.13	---

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Vendor option for pin one identifier. No alpha or numeric symbols allowed.
4. Dimension letters refer to MIL-STD-1835.
5. Leads must not overhang braze pads.
6. Dimensions B1 and C1 apply to base metal only. Dimension M applies to plating thickness.

FIGURE 1. Case outlines - Continued.

Case 9

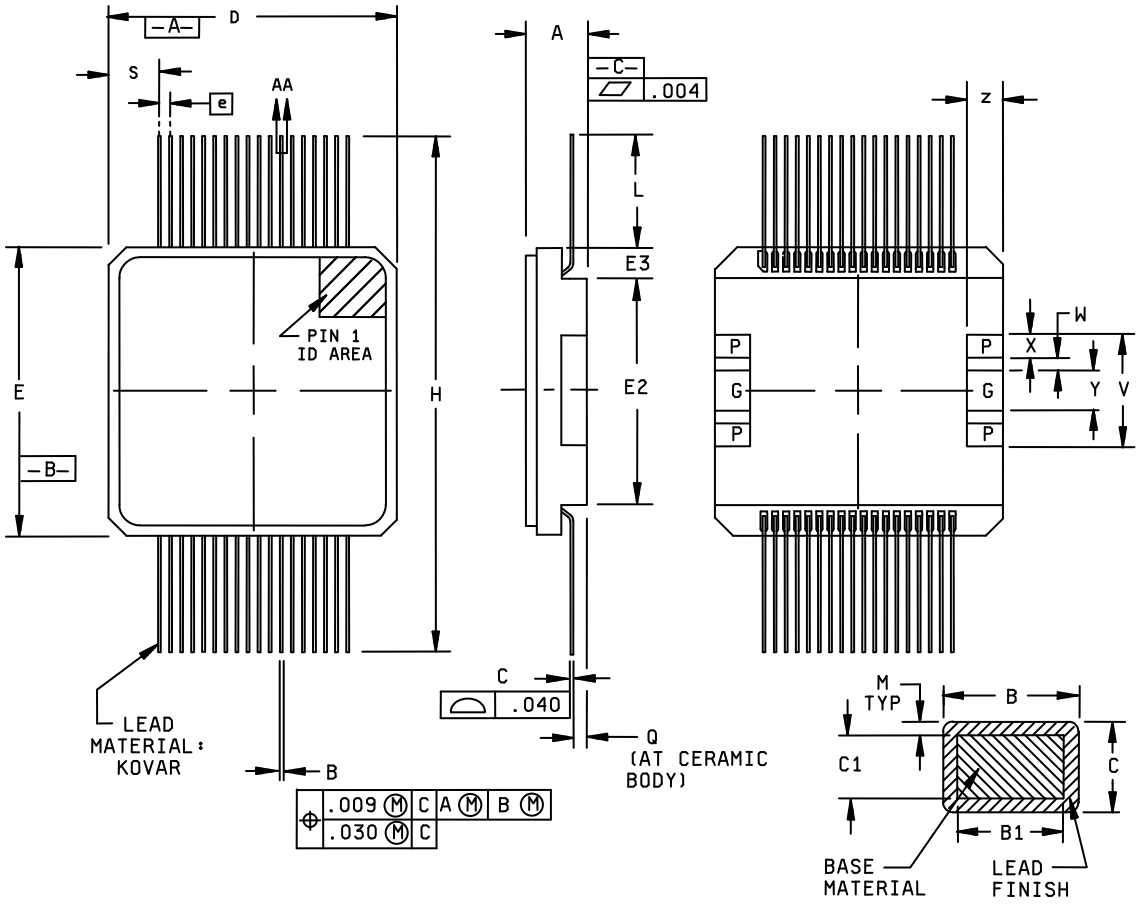


FIGURE 1. Case outlines - Continued.

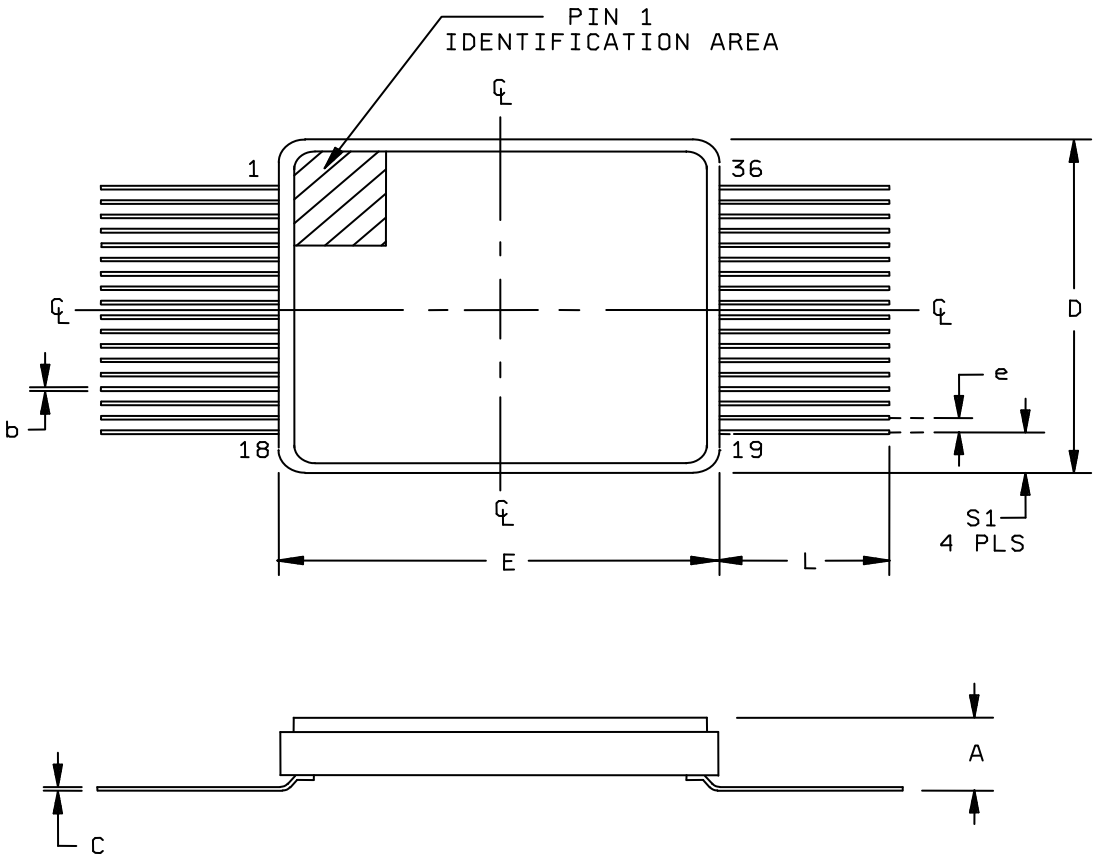
Case 9 – Continued.

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.150	---	3.810
B	.006	.013	1.52	.330
B1	.006	.010	1.52	.254
C	.0045	.0105	.114	.266
C1	.0045	.0075	.114	.190
D	.620	.640	15.75	16.26
e	.025 BSC		.635 BSC	
E	.620	.640	15.750	16.26
E2	.470	.490	11.940	12.450
E3	.075 REF		1.910 REF	
H	---	1.20	---	30.48
L	.270	---	6.858	---
M	.0015 TYP		.038 TYP	
Q	.026	---	.660	---
S	.1025 REF		2.604	
V	.260 REF		6.600	
W	.030 REF		.762	
X	.050 REF		1.270	
Y	.100 REF		2.540	
Z	.080 REF		2.030	

NOTES:
1. Package material: Opaque ceramic.
2. All exposed metallized areas pre gold plated over nickel plating in accordance with MIL-STD-1835.
3. Lead finish is in accordance with MIL-PRF-38535.
4. Capacitor pads P are electrically connected to V_{DD}. Capacitor pads G are electrically connected to V_{SS}.
5. Leads must not overhang braze pads.
6. Capacitors are optional at user level only. This document does not cover devices with capacitors installed.

FIGURE 1. Case outlines - Continued.

Case 8



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.075	.095	1.91	2.41
b	.007	.010	.18	.25
S1	.103	.123	2.62	3.12
c	.004	.006	.11	.15
D	.640	.660	16.26	16.76
E	.623	.637	15.82	16.18
e	.025 BSC		.635 BSC	
L	.235	.285	5.96	7.24

FIGURE 1. Case outlines - Continued.

Device types	01–19, 31–38, 40, 42, 43, 46, 47, 48–58	20 – 30, 59 – 68	01 – 19, 31 – 37, 48 – 58	35 – 43	44	45
Case outlines	X, Z, U, T, M, and N	U	Y	9	8, 9	9
Terminal number	Terminal symbol					
1	NC	A_4	NC	V_{SS}	GND	V_{SS}
2	A_{12}	A_5	NC	V_{CC}	V_{CC}	V_{CC}
3	A_7	A_6	A_{12}	NC	NC	NC
4	A_6	NC	A_7	A_{12}	A_{12}	A_{12}
5	A_5	A_7	A_6	A_7	A_7	A_7
6	A_4	A_8	A_5	A_6	A_6	A_6
7	A_3	A_9	A_4	A_5	A_5	A_5
8	A_2	A_{10}	A_3	A_4	A_4	A_4
9	A_1	A_{11}	A_2	A_3	A_3	A_3
10	A_0	A_{12}	A_1	A_2	A_2	A_2
11	I/O	I/O	A_0	A_1	A_1	A_1
12	I/O	I/O	NC	A_0	A_0	A_0
13	I/O	I/O	I/O	I/O	I/O	I/O
14	V_{SS}	V_{SS}	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O	I/O	I/O
16	I/O	I/O	V_{SS}	NC	NC	NC
17	I/O	I/O	NC	V_{CC}	V_{CC}	V_{CC}
18	I/O	I/O	I/O	V_{SS}	GND	V_{SS}
19	I/O	I/O	I/O	V_{SS}	GND	V_{SS}
20	$\overline{CE}_1$	$\overline{CE}_1$	I/O	V_{CC}	V_{CC}	V_{CC}
21	A_{10}	A_0	I/O	I/O	I/O	I/O
22	$\overline{OE}$	$\overline{OE}$	I/O	I/O	I/O	I/O
23	A_{11}	A_1	$\overline{CE}_1$	I/O	I/O	I/O
24	A_9	A_2	A_{10}	I/O	I/O	I/O
25	A_8	A_3	$\overline{OE}$	I/O	I/O	I/O
26	CE_2	CE_2	NC	$\overline{CE}_1$	$\overline{CE}_1$	$\overline{CE}_1$
27	$\overline{WE}$	$\overline{WE}$	A_{11}	A_{10}	A_{10}	A_{10}
28	V_{CC}	V_{CC}	A_9	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
29	- - -	- - -	A_8	A_{11}	A_{11}	A_{11}
30	- - -	- - -	CE_2	A_9	A_9	A_9
31	- - -	- - -	$\overline{WE}$	A_8	A_8	A_8
32	- - -	- - -	V_{CC}	CE_2	$\overline{AS}$	CE_2
33	- - -	- - -	- - -	$\overline{WE}$	CE_2	$\overline{WE}$
34	- - -	- - -	- - -	NC	$\overline{WE}$	$\overline{AS}$
35	- - -	- - -	- - -	V_{CC}	V_{CC}	V_{CC}
36	- - -	- - -	- - -	V_{SS}	GND	V_{SS}

FIGURE 2. Terminal connections.

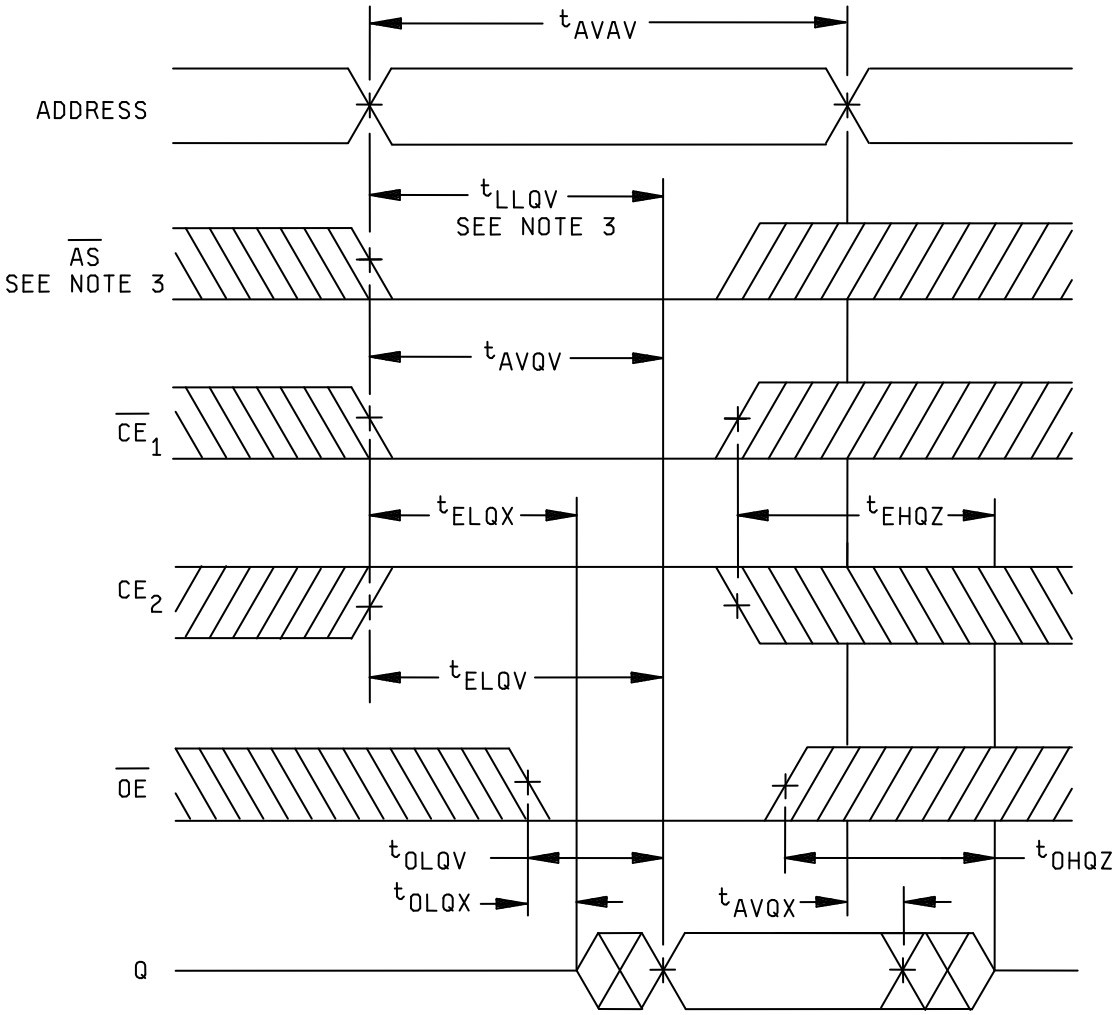
Device types 01-43, 46-68					
Mode	$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	I/O
Standby	H	X	X	X	High Z
Standby	X	L	X	X	High Z
Read	L	H	H	L	D_{OUT}
Write	L	H	L	X	D_{IN}
Read	L	H	H	H	High Z

Device type 44,45							
Mode	CE_2	$\overline{CE}_1$	$\overline{WE}$	$\overline{OE}$	$\overline{AS}$	I/O	Power
Write	H	L	L	X	X	D_{IN}	Active
Read	H	L	H	L	X	D_{OUT}	Active
Deselected	H	H	X	X	H	High Z	Deselected
Deselected, address load	H	H	X	X	L	High Z	Deselected
Standby	L	X	X	X	X	High Z	Standby

NOTE: H = logic "1" state, L = logic "0" state. X = logic "don't care state, and Z = high impedance state.

FIGURE 3. Truth table.

Read cycle



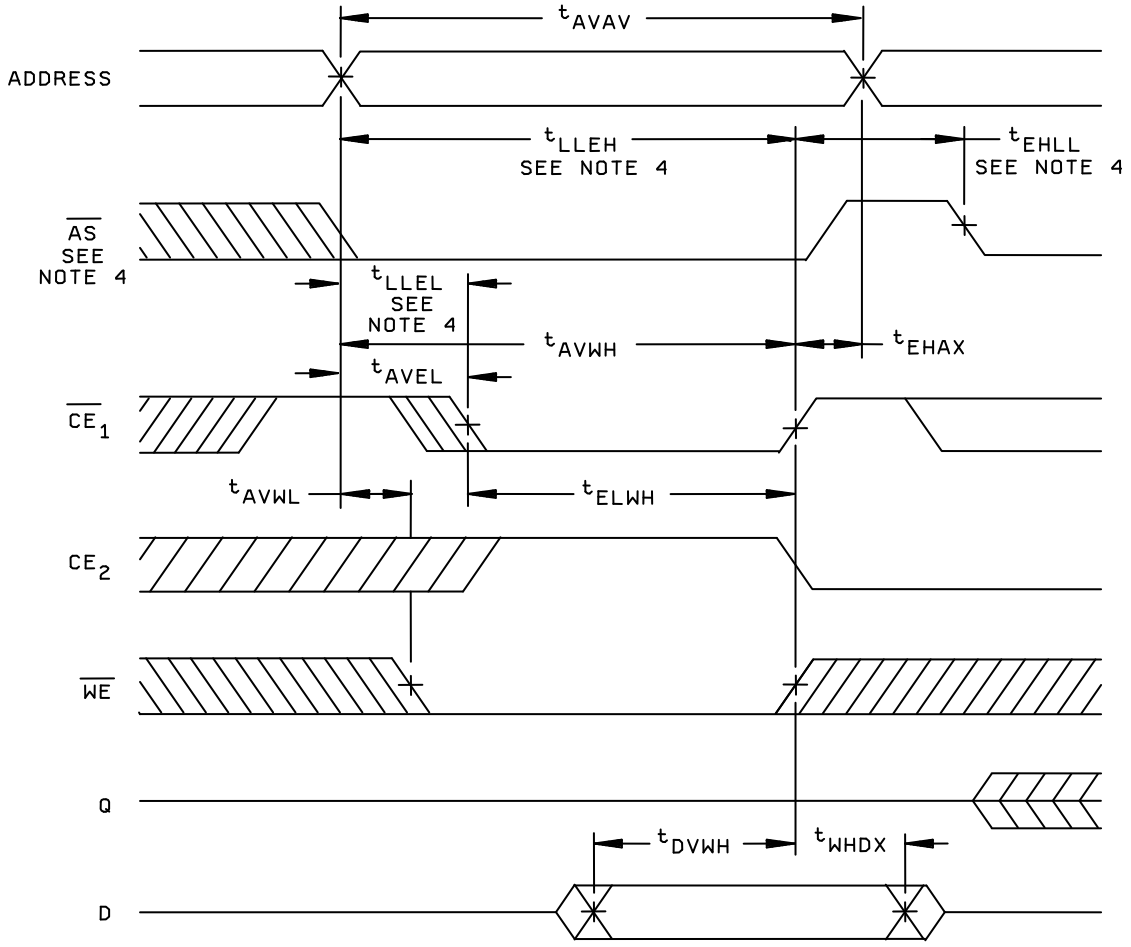
NOTES:

1. $\overline{WE}$ is held high during the read cycle.
2. Timing measurement reference level is 1.5 V.
3. Device type 44 and 45 only.

FIGURE 4. Timing waveforms.

Write cycle 1

(CE_1 or CE_2 controlled)

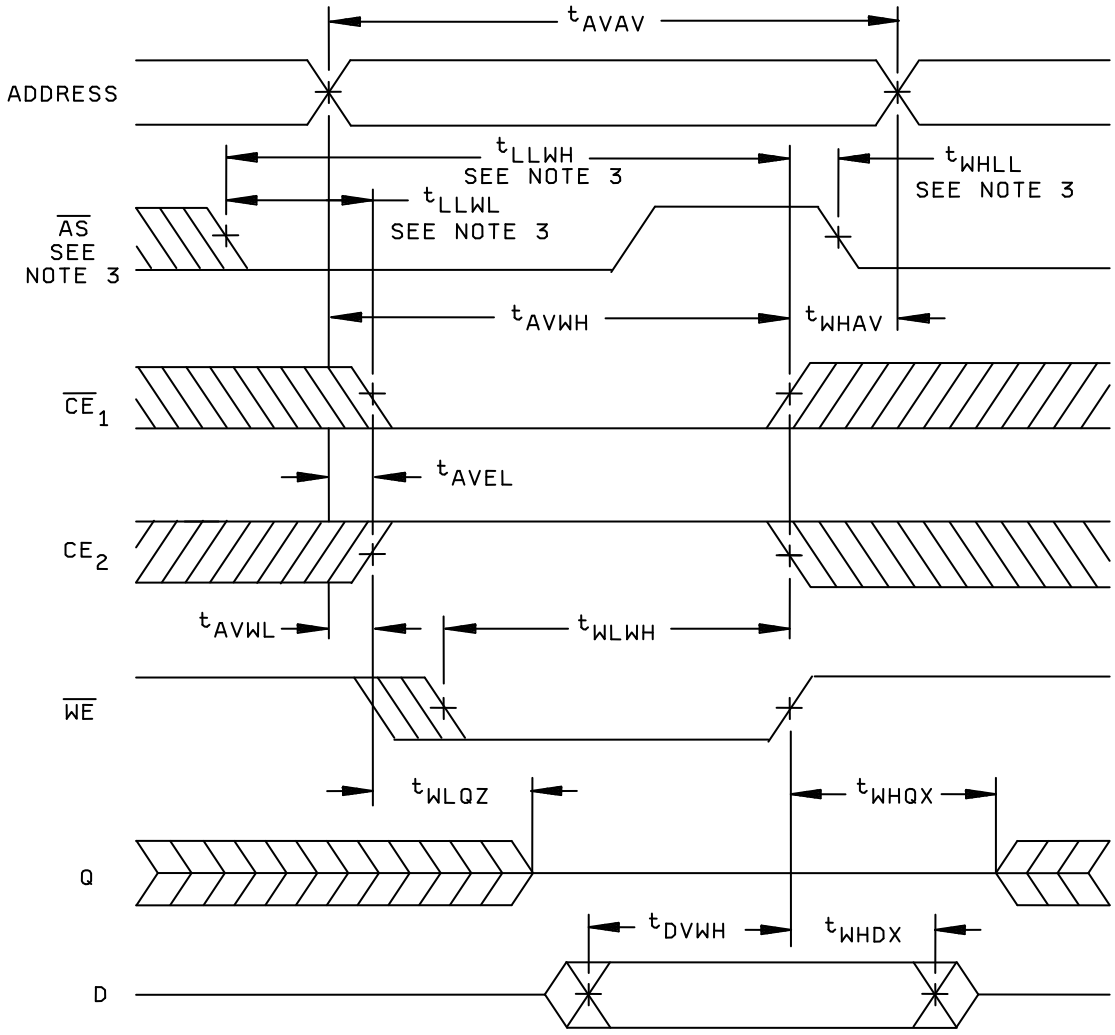


NOTES:

1. Either $\overline{CE}_1$ or CE_2 may be used to control the write cycle. If $\overline{CE}_1$ is used, CE_2 should be high when $\overline{WE}$ is low. If CE_2 is used, $\overline{CE}_1$ should be low when $\overline{WE}$ is low.
2. In a $\overline{CE}_1$ or CE_2 controlled write cycle, the outputs assume a high impedance state, whether $\overline{OE}$ is high or low, as long as $\overline{WE}$ is low.
3. Timing measurement reference is 1.5 V.
4. Device type 44 and 45 only.

FIGURE 4. Timing waveforms - Continued.

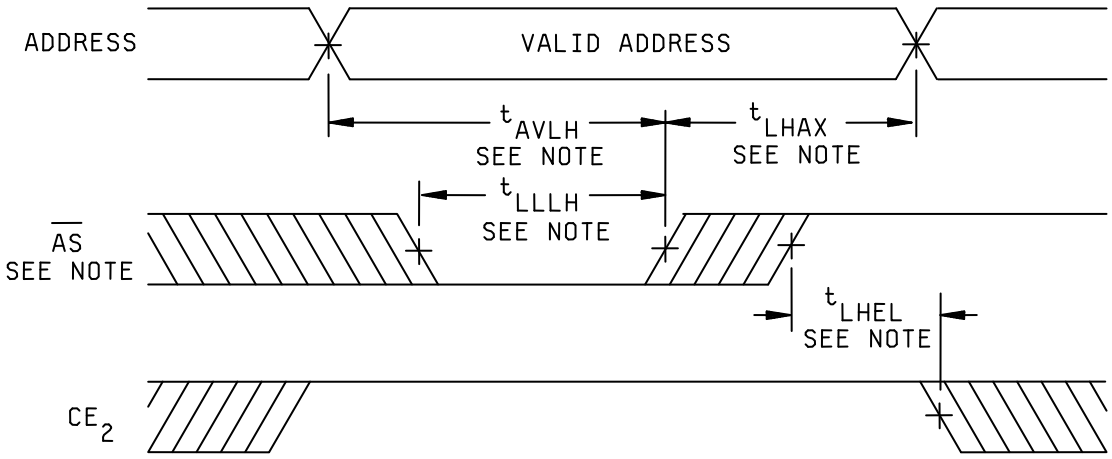
Write cycle 2
($\overline{WE}$ controlled)



NOTES:

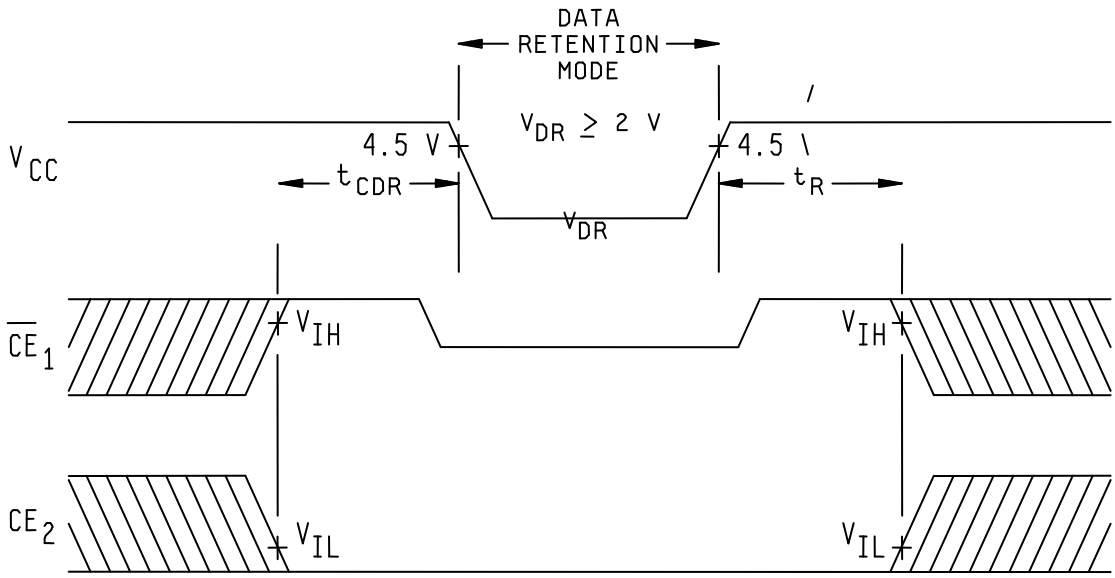
1. In the $\overline{WE}$ controlled write cycle, while $\overline{WE}$ is low, it will force the outputs into a high impedance state, whether $\overline{OE}$ is high or low.
2. Timing measurement reference is 1.5 V.
3. Device type 44 and 45 only.

FIGURE 4. Timing waveforms - Continued.



NOTE: Device types 44 and 45 only.

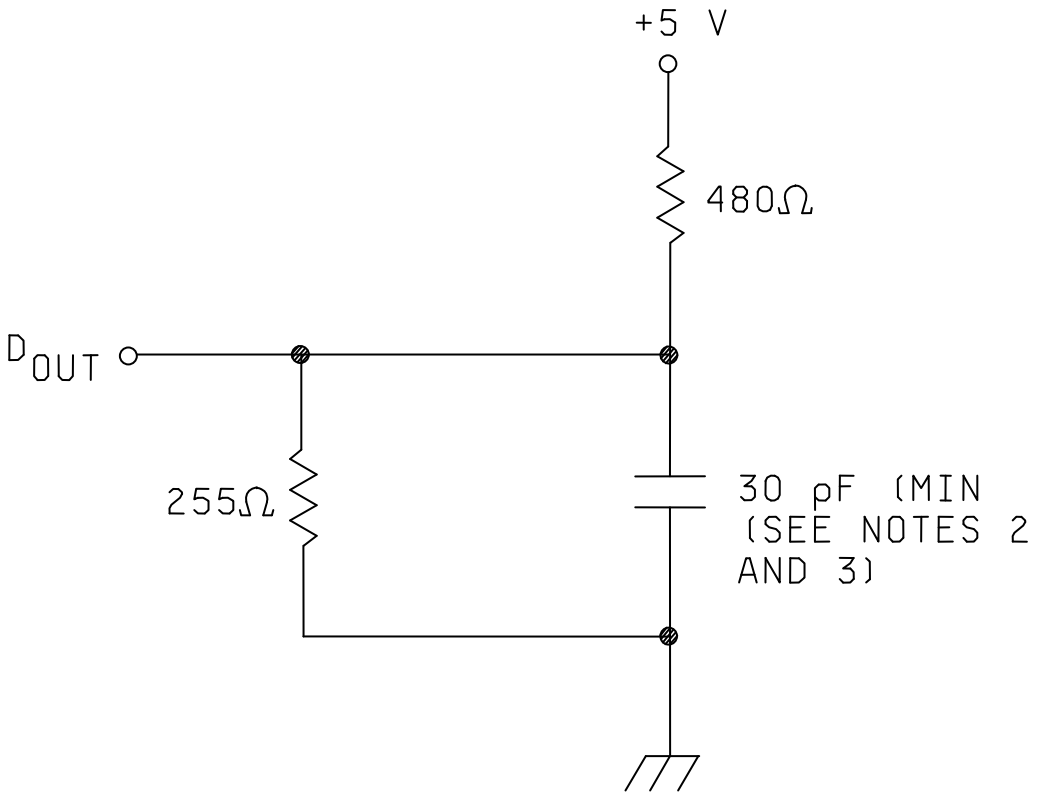
FIGURE 4. Timing waveforms - Continued.



NOTES:

1. Either $\overline{CE}_1$ or CE_2 may be used to begin data retention mode.
2. For t_{CDR} and t_R: $\overline{CE}_1 \geq V_{CC}$ -0.2 V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC}$ -2.0 V or $V_{IN} \leq 0.2$ V

FIGURE 4. Timing waveforms - Continued.



NOTES:
1. .Use this output load circuit or equivalent for testing.
2. Including scope and jig.
3. Minimum of 5 pF for t_{EHQZ}, t_{OHQZ}, t_{ELQX}, t_{OLQX}, and t_{WHQX}.

FIGURE 5. Output load circuit.

Case 9

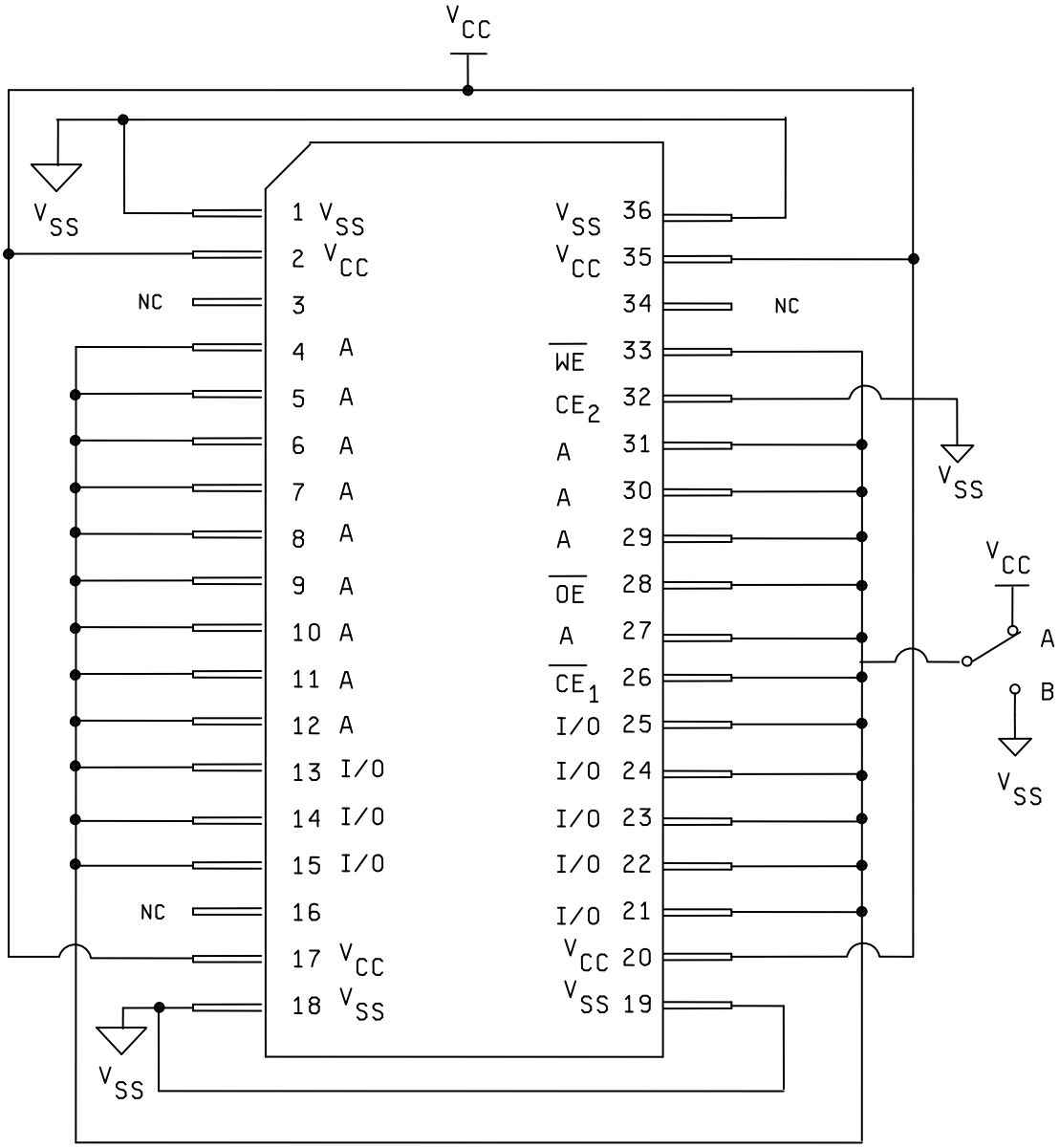
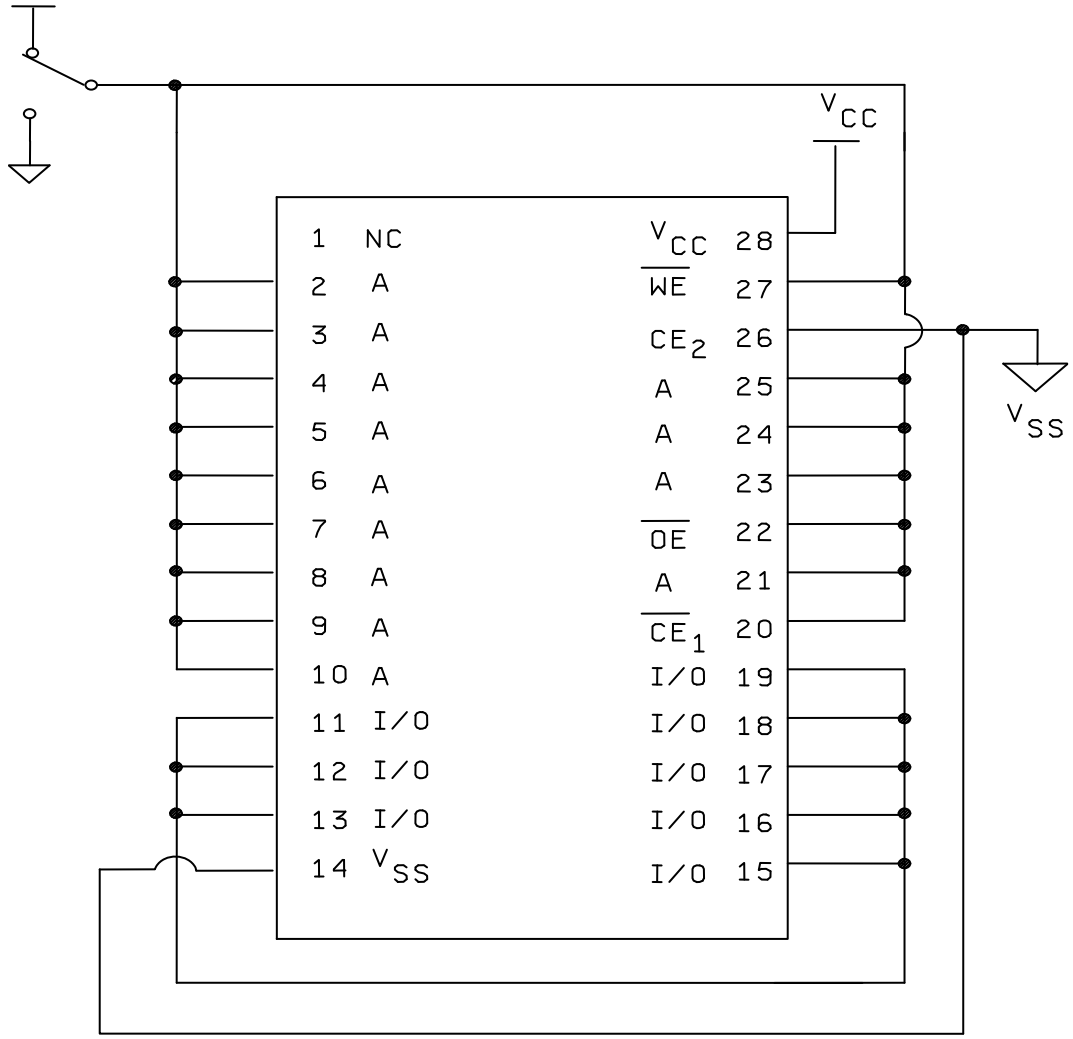


FIGURE 6. Radiation exposure circuit.

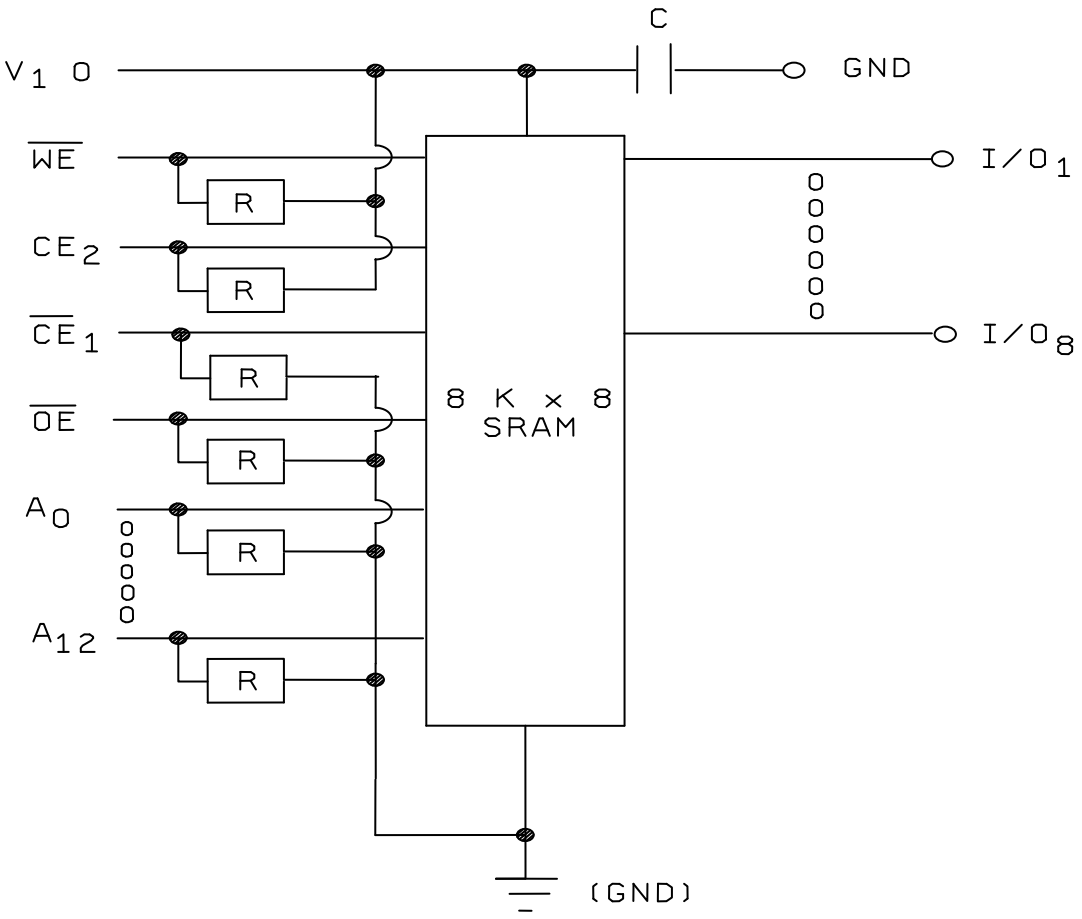
Case X



NOTES:
1. V_{CC} = 5.5 V dc (±10%).
2. Inputs = V_{CC}.
3. Outputs are open.
4. CE_2 = V_{SS} = 0 V dc.
5. Memory background shall be solid ones.

FIGURE 6. Radiation exposure circuit – Continued.

Case 8



NOTES:
1. Power pins connected to V_1.
2. The absolute voltage ratings of 1.3 shall not be exceeded.
3. ESD precautions shall be followed.
4. The pattern in the memory array will be checkerboard for irradiation and accelerated aging tests.
5. Pin conditions: During irradiation and accelerator aging tests.

$\overline{CE}_1$ = GND	$\overline{WE}$ = V_{CC}	I/O_1 - I/O_8 = FLOATING
CE_2 = V_{CC}	A_0 - A_{12} = GND	C = 0.1 µF ±10 percent
V_1 = V_{CC}	R = 10 kΩ ±10 percent	
V_{CC} = 5.0 V	$\overline{OE}$ = V_{CC}	

FIGURE 6. Radiation exposure circuit - Continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9 or 1,2,8A,10	1, 7, 9 or 1,2,8A,10
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall verify the truth table.

4/ * indicates PDA applies to subgroup 1 and 7.

5/ ** see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing.. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

Table IIB. Delta limits at +25°C.

Test 1/	All device types
I_{CC3} standby	± 10% of specified value in table IA
I_{IH}, I_{IL}	± 10% of specified value in table IA
I_{OHZ}, I_{OLZ}	± 10% of specified value in table IA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25ºC ±5ºC, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging shall be performed on all devices requiring a RHA level greater than 5K rads(Si). The post-anneal end point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may effect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). SEP testing shall be required on class V devices. SEP testing shall be performed on the SEC or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be normal to the die surface and 60° to the normal, inclusive (i.e., 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be greater than 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} = 5.5 V dc for the latch-up measurements.

g. For SEP test limits, see table IB herein.

4.4.4.3 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latch-up (SEP).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

C_{IN} C_{OUT} ---------- Input and bidirectional output, terminal-to-GND capacitance.
GND ---------- Ground zero voltage potential.
I_{CC} ---------- Supply current.
I_{IL} ---------- Input current low
I ---------- Input current high
T_C ---------- Case temperature.
T_A ---------- Ambient temperature
V_{CC} ---------- Positive supply voltage.
V_{IC} ---------- Positive input clamp voltage
O/V ---------- Latch-up over-voltage
O/I ---------- Latch-up over-current

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

t X X X X

Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

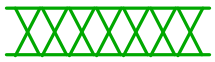
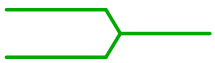
a. Signal definitions:

A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable
O = Output enable
L = Address latch (device 44 and 45 only)

b. Transition definitions:

H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

APPENDIX A

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3. ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum

APPENDIX B

SUBSTITUTION DATA

B.1 SCOPE

B.1.1 Scope. This appendix contains the PIN substitution information to support the one part-one part number system. SMD 5962-38294 supersedes SMDs 5962-85525 and 5962-89691. For new designs, after the date of this document the new PIN shall be used in lieu of the old PIN. For existing designs prior to the date of this document the new PIN can be used in lieu of the old PIN. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. The PIN substitution data shall be as follows:

B.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

B.3 SUBSTITUTION DATA

New PIN	Old PIN	New PIN	Old PIN
5962-3829401MXX	5962-8552501XX	5962-3829413MXX	5962-8552507XX
5962-3829401MYX	5962-8552501YX	5962-3829413MYX	5962-8552507YX
5962-3829402MXX	5962-8552513XX	5962-3829413MZX	5962-8552507ZX
5962-3829402MYX	5962-8552513YX	5962-3829413MTX	5962-8552507TX
5962-3829403MXX	5962-8552502XX	5962-3829414MXX	5962-8969101XX
5962-3829403MYX	5962-8552502YX	5962-3829414MZX	5962-8969101ZX
5962-3829404MXX	5962-8552512XX	5962-3829414MTX	5962-8969101TX
5962-3829404MYX	5962-8552512YX	5962-3829415MXX	5962-8969102XX
5962-3829405MXX	5962-8552503XX	5962-3829415MYX	5962-8969102YX
5962-3829405MYX	5962-8552503YX	5962-3829415MZX	5962-8969102ZX
5962-3829406MXX	5962-8552511XX	5962-3829415MUX	5962-8969102NX
5962-3829406MYX	5962-8552511YX	5962-3829415MTX	5962-8969102TX
5962-3829407MXX	5962-8552504XX	5962-3829417MXX	5962-8969104XX
5962-3829407MYX	5962-8552504YX	5962-3829417MYX	5962-8969104YX
5962-3829408MXX	5962-8552510XX	5962-3829417MZX	5962-8969104ZX
5962-3829408MYX	5962-8552510YX	5962-3829417MUX	5962-8969104NX
5962-3829408MZX	5962-8552510ZX	5962-3829417MTX	5962-8969104TX
5962-3829408MTX	5962-8552510TX	5962-3829419MXX	5962-8969106XX
5962-3829409MXX	5962-8552505XX	5962-3829419MYX	5962-8969106YX
5962-3829409MYX	5962-8552505YX	5962-3829419MZX	5962-8969106ZX
5962-3829409MZX	5962-8552505ZX	5962-3829419MUX	5962-8969106NX
5962-3829409MTX	5962-8552505TX	5962-3829419MTX	5962-8969106TX
5962-3829410MXX	5962-8552509XX	5962-3829422MUX	5962-8552510UX
5962-3829410MYX	5962-8552509YX	5962-3829423MUX	5962-8552505UX
5962-3829410MZX	5962-8552509ZX	5962-3829424MUX	5962-8552509UX
5962-3829410MTX	5962-8552509TX	5962-3829425MUX	5962-8552506UX
5962-3829411MXX	5962-8552506XX	5962-3829426MUX	5962-8552508UX
5962-3829411MYX	5962-8552506YX	5962-3829427MUX	5962-8552507UX
5962-3829411MZX	5962-8552506ZX	5962-3829428MUX	5962-8969101UX
5962-3829411MTX	5962-8552506TX	5962-3829429MUX	5962-8969102UX
5962-3829412MXX	5962-8552508XX	5962-3829430MUX	5962-8969104UX
5962-3829412MYX	5962-8552508YX	1/	5962-8969106UX
5962-3829412MZX	5962-8552508ZX		
5962-3829412MTX	5962-8552508TX		

1/ Due to erroneous data received for document 5962-89691, there is no substitution part.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-11-05

Approved sources of supply for SMD 5962-38294 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829401MXA	3DTT2 3/ 3/ 3/	P4C164-150CWMB IDT7164S150DB EDI8810H150DB AM99C88-15/BXC
5962-3829401MYA	3/ 3/ 3/	IDT7164S150L32B EDI8810H150LB AM99C88-15/BUC
5962-3829401MZA	3/	IDT7164S150TCB
5962-3829401MTA	3/	IDT7164S150XEB
5962-3829402MXA	3DTT2 3/ 3/	P4C164L-120CWMB IDT7164L120DB EDI8810H120DB
5962-3829402MYA	3/ 3/	IDT7164L120L32B EDI8810H120LB
5962-3829402MZA	3/	IDT7164L120TCB
5962-3829402MTA	3/	IDT7164L120XEB
5962-3829403MXA	3DTT2 3/ 3/ 3/ 3/	P4C164-120CWMB IDT7164S120DB EDI8810H120DB P4C164L-120DWMB AM99C88-12/BXC
5962-3829403MYA	3/ 3/ 3/	IDT7164S120L32B EDI8810H120LB AM99C88-12/BUC
5962-3829403MZA	3/	IDT7164S120TCB
5962-3829403MTA	3/	IDT7164S120XEB
5962-3829404MXA	3DTT2 3/ 3/ 3/	P4C164L-100CWMB IDT7164L100DB EDI8810H100DB P4C164L-100DWMB

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829404MYA	3/ 3/	IDT7164L100L32B EDI8810H100LB
5962-3829404MZA	3/	IDT7164L100TCB
5962-3829404MTA	3/	IDT7164L100XEB
5962-3829405MXA	3DTT2 3/ 3/ 3/ 3/	P4C164-100CWMB IDT7164S100DB EDI8810H100DB P4C164-100DWMB AM99C88-10/BXC
5962-3829405MYA	3/ 3/ 3/	IDT7164S100L32B EDI8810H100LB AM99C88-10/BUC
5962-3829405MZA	3/	IDT7164S100TCB
5962-3829405MTA	3/	IDT7164S100XEB
5962-3829406MXA	3DTT2 61772 3/ 3/	P4C164L-70CWMB IDT7164L70DB L7C185IMB70 EDI8810H70DB
5962-3829406MYA	3/ 3/ 3/ 3/ 3/ 3/	P4C164L-70DWMB IDT7164L70L32B EDI8810H-70LB L7C185TMB70 IMS1630W-70LM MT5C6408ECW-70L
5962-3829406MZA	61772 3/ 3/	IDT7164L70TDB MT5C6408C-70L L7C185CMB70
5962-3829406MUA	3/ 3/	L7C185KMB70 MT5C6408EC-70L
5962-3829406MTA	3/ 3/	IDT7164L70XEB L7C185MMB70
5962-3829406MMA	3/	MT5C6408F-70L
5962-3829407MXA	3/ 61772 3/ 3DTT2 3/ 3/ 3/ 3/ 0C7V7	6164-70/BXAJC IDT7164S70DB EDI8810H70DB P4C164-70DWMB MC5164-70/B AM99C88-70/BXC 6264-70/BXAJC L7C185IMB70 QP7C186A-70DMB

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829407MYA	3/	MR5164-70/B
	3/	6164-70M/BUAJC
	3/	IDT7164S70L32B
	3/	EDI8810H70LB
	3/	MT5C6408ECW-70
	3/	AM99C88-70/BUC
	3/	L7C185TMB70
	3DTT2	P4C164-70L32MB
	0C7V7	QP7C186A-70LMB
5962-3829407MZA	3/	MT5C6408C-70
	3/	L7C185CMB700
	3DTT2	P4C164-70DMB
	0C7V7	QP7C185A-70DMB
	61772	IDT7164S70TDB
5962-3829407MTA	3DTT2	P4C164-70FMB
	3/	IDT7164S70XEB
	3/	L7C185MMB70
5962-3829407MUA	3DTT2	P4C164-70LSMB
	3/	MT5C6408EC-70
	3/	L7C185KMB70
5962-3829407MMA	3DTT2	P4C164-70FSMB
	3/	MT5C6408F-70
	3/	MF5164-70/B
5962-3829408MXA	3/	EDI8810H55DB
	61772	IDT7164L55DB
	3DTT2	P4C164L-55DWMB
	3/	L7C185IMB55
5962-3829408MYA	3DTT2	P4C164L-55L32MB
	3/	EDI8810H55LB
	3/	IDT7164L55L32B
	3/	MT5C6408ECW-55L
	3/	L7C185TMB55
5962-3829408MZA	3/	P4C164L-55DMB
	3DTT2	P4C164L-55DMB
	3/	MT5C6408C-55L
	61772	IDT7164L55TDB
	3/	L7C185CMB55
5962-3829408MUA	3DTT2	P4C164L-55LSMB
	3/	MT5C6408EC-55L
	3/	L7C185KMB55
5962-3829408MMA	3DTT2	P4C164L-55FSMB
	3/	MT5C6408F-55L
5962-3829408MTA	3DTT2	P4C164L-55FMB
	3/	IDT7164L55XEB
	3/	P4C164L-55FMB
	3/	CY7C185L-55KMB
	3/	L7C185MMB55

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829409MXA	61772 3/ 3/ 3/ 3DTT2 3/ 3/ 3/ 0C7V7	IDT7164S55DB 6164-55/BXAJC EDI8810H55DB CY7C186A-55DMB P4C164-55DWMB HM1E-65764N/883 6264-55/BXAJC L7C185IMB55 QP7C186A-55DMB
5962-3829409MYA	3/ 3/ 3/ 3/ 3DTT2 3/ 0C7V7 3/	IDT7164S55L32B 6164-55M/BUAJC EDI8810H55LB CY7C186A-55LMB P4C164-55L32MB L7C185TMB55 QP7C186A-55LMB MT5C6408ECW-55
5962-3829409MYC	3/	HM4-65764N/883
5962-3829409MZA	3/ 3/ 3DTT2 61772 3/ 3/ 3/ 0C7V7	CY7C185A-55DMB MT5C6408C-55 P4C164-55DMB IDT7164S55TDB HM1-65764N/883 EDI8808CB55QB L7C185CMB55 QP7C185A-55DMB
5962-3829409MUA	3DTT2 3/ 3/	P4C164-55LSMB MT5C6408EC-55 L7C185KMB55
5962-3829409MMA	3DTT2 3/	P4C164-55FSMB MT5C6408F-55
5962-3829409MTA	3DTT2 3/ 3/ 3/ 3/	P4C164-55FMB CY7C185A-55KMB IDT7164S55XEB L7C185MMB55 P4C164-55FMB
5962-3829410MXA	3/ 61772 3/ 3DTT2 3/ 3/	62L64-45BXAJC IDT7164L45DB MC5164L-45/B P4C164L-45DWMB CY7C186L-45DMB L7C185IMB45
5962-3829410MYA	3/ 3/ 3/ 3/	MR5164L-45/B IDT7164L45L32B MT5C6408ECW-45L L7C185TMB45

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829410MZA	3/ 3DTT2 61772 3/ 3/	MT5C6408C-45L P4C164L-45DMB IDT7164L45TDB CY7C185L-45DMB L7C185CMB45
5962-3829410MUA	3DTT2 3/ 3/	P4C164L-45LSMB MT5C6408EC-45L L7C185KMB45
5962-3829410MMA	3/ 3/ 3DTT2	MT5C6408F-45L MF5164L-45/B P4C164L-45FSMB
5962-3829410MTA	3/ 3DTT2 3/ 3/	IDT7164L45XEB P4C164L-45FMB CY7C185L-45KMB L7C185MMB45
5962-3829411MXA	3/ 3/ 61772 3/ 3DTT2 3/ 3/ 0C7V7	MC5164-45/B 6264-45/BXAJC IDT7164S45DB CY7C186A-45DMB P4C164-45DWMB HM1E-65764M/883 L7C185IMB45 QP7C186A-45DMB
5962-3829411MYA	0C7V7 3/ 3/ 3/ 3/ 3/ 3DTT2	QP7C186A-45LMB MR5164-45/B IDT7164S45L32B MT5C6408ECW-45 CY7C186A-45LMB L7C185TMB45 P4C164-45L32MB
5962-3829411MYC	3/	HM4-65764M/883
5962-3829411MZA	3/ 3/ 3DTT2 61772 3/ 3/ 0C7V7 3/	CY7C185A-45DMB MT5C6408C-45 P4C164-45DMB IDT7164S45TDB HM1-65764M/883 EDI8808CB45QB QP7C185A-45DMB L7C185CMB45
5962-3829411MUA	3/ 3/ 3DTT2	MT5C6408EC-45 L7C185KMB45 P4C164-45LSMB
5962-3829411MMA	3/ 3/ 3DTT2	MT5C6408F-45 MF5164-45/B P4C164-45FSMB

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829411MTA	3/ 3/ 3/ 3/ 3DTT2	CY7C185A-45KMB MT5C6408F-45 L7C185MMB45 IDT7164S45XEB P4C164-45FMB
5962-3829412MXA	61772 3/ 3DTT2 3/ 3/ 3/	IDT7164L35DB MC5164L-35/B P4C164L-35DWMB 62L64-35/BXAJC CY7C186L-35DMB L7C185IMB35
5962-3829412MYA	3/ 3/ 3/ 3/ 3DTT2	MR5164L-35/B IDT7164L35L32B MT5C6408ECW-35L L7C185TMB35 P4C164L-35L32MB
5962-3829412MZA	61772 3/ 3/ 3DTT2	IDT7164L35TDB MT5C6408C-35L L7C185CMB35 P4C164L-35DMB
5962-3829412MUA	3DTT2 3/ 3/ 3/	P4C164L-35LSMB MT5C6408EC-35L L7C185KMB35 CY7C185L-35DMB
5962-3829412MMA	3/ 3/ 3DTT2	MT5C6408F-35L MF5164L-35/B P4C164L-35FSMB
5962-3829412MTA	3/ 3DTT2 3/ 3/	IDT7164L35XEB P4C164L-35FMB CY7C185L-35KMB L7C185MMB35
5962-3829413MXA	3/ 3/ 61772 3/ 3DTT2 3/ 3/ 0C7V7	MC5164-35/B 6264-35/BXAJC IDT7164S35DB CY7C186A-35DMB P4C164-35DWMB HM1E-65764K/883 L7C185IMB35 QP7C186A-35DMB
5962-3829413MYA	3/ 3/ 3/ 3/ 3/ 3DTT2 0C7V7	MR5164-35/B IDT7164S35L32B CY7C186A-35LMB MT5C6408ECW-35 L7C185TMB35 P4C164-35L32MB QP7C186A-35LMB
5962-3829413MYC	3/	HM4-65764K/883

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829413MZA	3/	CY7C185A-35DMB
	3/	MT5C6408C-35
	3DTT2	P4C164-35DMB
	61772	IDT7164S35TDB
	3/	HM1-65764K/883
	3/	L7C185CMB35
	3/	EDI8808CB35QB
	0C7V7	QP7C185A-35DMB
5962-3829413MUA	3/	MT5C6408EC-35
	3/	L7C185KMB35
	3DTT2	P4C164-35LSMB
5962-3829413MMA	3/	MT5C6408F-35
	3/	MF5164-35/B
	3DTT2	P4C164-35FSMB
5962-3829413MTA	3/	CY7C185A-35KMB
	3/	IDT7164S35XEB
	3DTT2	P4C164-35FMB
	3/	L7C185MMB35
5962-3829414MXA	3/	MC5164L-25/B
	61772	IDT7164L25DB
	3DTT2	P4C164L-25DWMB
	3/	L7C185HMB or IMB25
5962-3829414MYA	3/	MR5164L-25/B
	3/	IDT7164L25L32B
	3/	MT5C6408ECW-25L
	3/	L7C185TMB25
	3DTT2	P4C164L-25L32MB
5962-3829414MZA	3DTT2	P4C164L-25DMB
	61772	IDT7164L25TDB
	3/	MT5C6408C-25L
	3/	L7C185DMB CMB25
5962-3829414MUA	3/	MT5C6408EC-25L
	3/	L7C185KMB25
	3DTT2	P4C164-25LSMB
5962-3829414MMA	3/	MF5164L-25/B
	3/	MT5C6408F-25L
	3/	L7C185FMB25
	3DTT2	P4C164L-25FSMB
5962-3829414MTA	3/	P4C164L-25FMB
	3/	IDT7164L25XEB
	3/	L7C185MMB25
	3DTT2	P4C164-25FMB

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829415MXA	3DTT2 3/ 3/ 61772 3/ 3/ 0C7V7	P4C164-25DWMB CY7C186A-25DMB MC5164-25/B IDT7164S25DB HM1E-65764H/883 L7C185HMB or IMB25 QP7C186A-25DMB
5962-3829415MYA	3/ 3/ 3/ 3/ 3DTT2 0C7V7 3/	MR5164-25/B MT5C6408ECW-25 CY7C186A-25LMB IDT7164S25L32B P4C164-25L32MB QP7C186A-25LMB L7C185TMB25
5962-3829415MYC	3/	HM4-65764H/883
5962-3829415MZA	3DTT2 3/ 3/ 61772 3/ 3/ 3/ 0C7V7	P4C164-25DMB MT5C6408C-25 CY7C185A-25DMB IDT7164S25TDB HM1-65764H/883 L7C185DMB or CMB25 EDI8808CB25QB QP7C185A-25DMB
5962-3829415MUA	3/ 3/ 3DTT2	MT5C6408EC-25 L7C185KMB25 P4C164-25LSMB
5962-3829415MMA	3/ 3/ 3/ 3DTT2	MT5C6408F-25 MF5164-25/B L7C185FMB25 P4C164-25FSMB
5962-3829415MTA	3/ 3DTT2 3/ 3/	CY7C185A-25KMB P4C164-25FMB IDT7164S25XEB L7C185MMB25
5962-3829416MXA	61772 3/ 3DTT2	IDT7164L20DB L7C185HMB or IMB25 P4C164L-20DWMB
5962-3829416MYA	61772 3/ 3/ 3DTT2	IDT7164L20L32B MT5C6408ECW-20L L7C185TMB20 P4C164L-20L32MB
5962-3829416MZA	61772 3/ 3/ 3DTT2	IDT7164L20TDB MT5C6408C-20L L7C185DMB or CMB20 P4C164L-20DMB

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829416MUA	3/ 3/ 3DTT2	MT5C6408EC-20L L7C185KMB20 P4C164L-20LSMB
5962-3829416MMA	3/ 3/ 3DTT2	MT5C6408F-20L L7C185FMB20 P4C164L-20FSMB
5962-3829416MTA	3DTT2 3/ 3/	P4C164L-20FMB IDT7164L20XEB L7C185MMB20
5962-3829417MXA	3/ 3DTT2 61772 3/ 3/ 0C7V7	CY7C186A-20DMB P4C164-20DWMB IDT7164S20DB HM1E-65764F/883 L7C185HMB or IMB20 QP7C186A-20DMB
5962-3829417MYA	3/ 3/ 3/ 0C7V7 3DTT2 3/	MT5C6408ECW-20 CY7C186A-20LMB IDT7164S20L32B QP7C186A-20LMB P4C164-20L32MB L7C185TMB20
5962-3829417MYC	3/	HM4-65764F/883
5962-3829417MZA	3DTT2 3/ 3/ 61772 3/ 3/ 0C7V7	P4C164-20DMB MT5C6408C-20 CY7C185A-20DMB IDT7164S20TDB HM1-65764F/883 L7C185DMB or CMB20 QP7C185A-20DMB
5962-3829417MUA	3/ 3/ 3DTT2	MT5C6408EC-20 L7C185KMB20 P4C164-20LSMB
5962-3829417MMA	3/ 3/ 3DTT2	MT5C6408F-20 L7C185FMB20 P4C164-20FSMB
5962-3829417MTA	3DTT2 3/ 3/ 3/	P4C164-20FMB CY7C185A-20KMB IDT7164S20XEB L7C185MMB20
5962-3829418MXA	3/ 3DTT2	L7C185HMB or IMB15 P4C164L-15DWMB

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829418MYA	3/ 3/ 3DTT2	MT5C6408ECW-15L L7C185TMB15 P4C164L-15L32MB
5962-3829418MZA	3/ 3/ 3DTT2	MT5C6408C-15L L7C185DMB or CMB15 P4C164L-15DMB
5962-3829418MUA	3/ 3/ 3DTT2	MT5C6408EC-15L L7C185KMB15 P4C164L-15LMB
5962-3829418MMA	3/ 3/ 3DTT2	MT5C6408F-15L L7C185FMB15 P4C164L-15FSMB
5962-3829418MTA	3/ 3DTT2	L7C185MMB15 P4C164L-15FMB
5962-3829419MXA	3DTT2 3/ 3/	P4C164-15DWMB L7C185HMB or IMB15 CY7C186-15DMB
5962-3829419MYA	3/ 3/ 3DTT2	MT5C6408ECW-15 L7C185TMB15 P4C164-15L32MB
5962-3829419MZA	3/ 3/ 3DTT2	MT5C6408C-15 L7C185DMB or CMB15 P4C164-15DMB
5962-3829419MUA	3/ 3/ 3DTT2	MT5C6408EC-15 L7C185KMB15 P4C164-15LSMB
5962-3829419MMA	3/ 3/ 3DTT2	MT5C6408F-15 L7C185FMB15 P4C164-15FSMB
5962-3829419MTA	3DTT2 3/ 3/	P4C164-15FMB L7C185MMB15 CY7C186-15KMB
5962-3829420MXA	3/	L7C185IMB70
5962-3829420MYA	3/ 3/	L7C185TMB70 MT5C6408ECW -70L
5962-3829420MZA	3/ 3/	L7C185CMB70 MT5C6408C -70L

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829420MUA	3/ 3/ 3/	P4C164L-70LMB MT5C6408EC -70L L7C185KMB70
5962-3829420MMA	3/	MT5C6408F-70L
5962-3829420MTA	3/	L7C185MMB70
5962-3829421MXA	3/ 3/	L7C185IMB70 P4C164-70DWMB
5962-3829421MYA	3/ 3/	L7C185TMB70 MT5C6408ECW -70
5962-3829421MZA	3/ 3/	L7C185CMB70 MT5C6408C -70
5962-3829421MUA	3DTT2 3/ 3/ 0C7V7	P4C164-70LMB MT5C6408EC-70 L7C185KMB70 QP7C185A-70LMB
5962-3829421MTA	3/	L7C185MMB70
5962-3829421MMA	3/	MT5C6408F-70
5962-3829422MXA	3/ 3/	L7C185IMB55 P4C164L-55DWMB
5962-3829422MYA	3/ 3/	L7C185TMB55 MT5C6408ECW -55L
5962-3829422MZA	3/ 3/	L7C185CMB55 MT5C6408C -55L
5962-3829422MUA	3DTT2 3/ 3/	P4C164L-55LMB MT5C6408EC-55L L7C185KMB55
5962-3829422MTA	3/	L7C185MMB55
5962-3829422MMA	3/	MT5C6408F-55L
5962-3829423MXA	3/ 3/	L7C185IMB55 P4C164-55DWMB
5962-3829423MYA	3/ 3/	L7C185TMB55 MT5C6408ECW-55

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829423MZA	3/ 3/	L7C185CMB55 MT5C6408C-55
5962-3829423MUA	3DTT2 3/ 3/ 3/ 0C7V7	P4C164-55LMB MT5C6408EC-55 L7C185KMB55 CY7C185A-55LMB QP7C185A-55LMB
5962-3829423MTA	3/	L7C185MMB55
5962-3829423MMA	3/	MT5C6408F-55
5962-3829424MXA	3/ 3/	L7C185IMB45 P4C164L-45DWMB
5962-3829424MYA	3/ 3/	L7C185TMB45 MT5C6408ECW-45L
5962-3829424MZA	3/ 3/	L7C185CMB45 MT5C6408C-45L
5962-3829424MUA	3DTT2 3/ 3/ 3/	P4C164L-45LMB CY7C185L-45LMB MT5C6408EC-45L L7C185KMB45
5962-3829424MTA	3/	L7C185MMB45
5962-3829424MMA	3/	MT5C6408F-45L
5962-3829425MXA	3/ 3/	L7C185IMB45 P4C164-45DWMB
5962-3829425MYA	3/ 3/	L7C185TMB45 MT5C6408ECW-45
5962-3829425MZA	3/ 3/ 3/	EDI8808CB45QB L7C185CMB45 MT5C6408C-45
5962-3829425MUA	3DTT2 3/ 3/ 3/ 0C7V7	P4C164-45LMB CY7C185A-45LMB L7C185KMB45 MT5C6408EC-45 QP7C185A-45LMB
5962-3829425MTA	3/	L7C185MMB45

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829425MMA	3/	MT5C6408F-45
5962-3829426MXA	3/ 3/	L7C185IMB35 P4C164L-35DWMB
5962-3829426MYA	3/ 3/	L7C185TMB35 MT5C6408ECW-35L
5962-3829426MZA	3/ 3/	L7C185CMB35 MT5C6408C-35L
5962-3829426MUA	3DTT2 3/ 3/ 3/	P4C164L-35LMB CY7C185L-35LMB L7C185KMB35 MT5C6408EC-35L
5962-3829426MTA	3/	L7C185MMB35
5962-3829426MMA	3/	MT5C6408F-35L
5962-3829427MXA	3/ 3/	L7C185IMB35 P4C164-35DWMB
5962-3829427MYA	3/ 3/	L7C185TMB35 MT5C6408ECW-35
5962-3829427MZA	3/ 3/ 3/	EDI8808CB35QB L7C185CMB35 MT5C6408C-35
5962-3829427MUA	3/ 3DTT2 3/ 3/ 0C7V7	CY7C185A-35LMB P4C164-35LMB MT5C6408EC-35 L7C185KMB35 QP7C185A-35LMB
5962-3829427MTA	3/	L7C185MMB35
5962-3829427MMA	3/	MT5C6408F-35
5962-3829428MXA	3/ 3/	L7C185HMB or IMB25 P4C164L-25DWMB
5962-3829428MYA	3/ 3/	L7C185TMB25 MT5C6408ECW-25L
5962-3829428MZA	3/ 3/	L7C185DMB or CMB25 MT5C6408C-25L

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829428MUA	3DTT2 3/ 3/	P4C164L-25LMB L7C185KMB25 MT5C6408EC-25L
5962-3829428MMA	3/ 3/	L7C185FMB25 MT5C6408F-25L
5962-3829428MTA	3/	L7C185MMB25
5962-3829429MXA	3/ 3/	L7C185HMB or IMB25 P4C164-25DWMB
5962-3829429MYA	3/ 3/	L7C185TMB25 MT5C6408ECW-25
5962-3829429MZA	3/ 3/ 3/	L7C185DMB or CMB25 EDI8808CB25QB MT5C6408C-25
5962-3829429MUA	3/ 3DTT2 3/ 3/ 0C7V7	CY7C185A-25LMB P4C164-25LMB L7C185KMB25 MT5C6408EC-25 QP7C185A-25LMB
5962-3829429MMA	3/ 3/	L7C185FMB25 MT5C6408F-25
5962-3829429MTA	3/	L7C185MMB25
5962-3829430MXA	3/ 3/	L7C185HMB or IMB20 P4C164-20DWMB
5962-3829430MYA	3/ 3/	L7C185TMB20 MT5C6408ECW-20
5962-3829430MZA	3/ 3/ 3/	L7C185DMB or CMB20 EDI8808CB25QB MT5C6408C-20
5962-3829430MUA	3/ 3DTT2 3/ 3/ 0C7V7	CY7C185A-20LMB P4C164-20LMB L7C185KMB20 MT5C6408EC-20 QP7C185A-20LMB

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829430MMA	3/ 3/	L7C185FMB20 MT5C6408F-20
5962-3829430MTA	3/	L7C185MMB20
5962-3829431MXA	3/ 3DTT2	EDI8810L100DB P4C164L-100CWMB
5962-3829431MYA	3/	EDI8810L100LB
5962-3829432MXA	3/ 3DTT2	EDI8810L70DB P4C164L-70CWMB
5962-3829432MYA	3/	EDI8810L70LB
5962-3829433MXA	3/ 3/ 3DTT2	L7C185IMB55 EDI8810L55DB P4C164L-55DWMB
5962-3829433MYA	3/ 3/ 3DTT2	L7C185TMB55 EDI8810L55LB P4C164L-55L32MB
5962-3829433MZA	3/ 3DTT2	L7C185CMB55 P4C164L-55DMB
5962-3829433MUA	3/ 3DTT2	L7C185KMB55 P4C164L-55LSMB
5962-3829433MMA	3/ 3DTT2	7C185-55 P4C164L-55FSMB
5962-3829433MTA	3/ 3DTT2	L7C185MMB55 P4C164L-55FMB
5962-3829434MXA	3/ 3DTT2	L7C185IMB45 P4C164L-45DWMB
5962-3829434MYA	3/ 3DTT2	L7C185TMB45 P4C164L-45L32MB
5962-3829434MZA	3/ 3DTT2	L7C185CMB45 P4C164L-45DMB

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829434MUA	3/ 3DTT2	L7C185KMB45 P4C164L-45LSMB
5962-3829434MMA	3/ 3DTT2	7C185-45 P4C164L-45FSMB
5962-3829434MTA	3/ 3DTT2	L7C185MMB45 P4C164L-45FMB
5962-3829435MXA	3DTT2	P4C164L-85CWMB
5962-3829435*--	3/	UT6716485
5962H3829435BNA	3/	UT6716485
5962H3829435BNC	3/	UT6716485
5962H3829435BXA	3/	UT6716485
5962H3829435BXC	3/	UT6716485
5962H3829435SNA	3/	UT6716485
5962H3829435SNC	3/	UT6716485
5962H3829435SXA	3/	UT6716485
5962H3829435SXC	3/	UT6716485
5962-3829436MXA	3DTT2	P4C164L-70CWMB
5962-3829436*--	3/	MK48H64
5962H3829436BNA	3/	UT6716470
5962H3829436BNC	3/	UT6716470
5962H3829436BXA	3/	UT6716470
5962H3829436BXC	3/	UT6716470
5962H3829436SNA	3/	UT6716470
5962H3829436SNC	3/	UT6716470
5962H3829436SXA	3/	UT6716470
5962H3829436SXC	3/	UT6716470
5962-3829437MXA	3DTT2	P4C164L-55CWMB

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829437*--	3/	UT6716455
5962H3829437BNA	3/	UT6716455
5962H3829437BNC	3/	UT6716455
5962H3829437BXA	3/	UT6716455
5962H3829437BXC	3/	UT6716455
5962H3829437SNA	3/	UT6716455
5962H3829437SXA	3/	UT6716455
5962H3829437SXC	3/	UT6716455
5962H3829438V9C	3/	HC6364/1XVHBT
5962H3829438Q9C	3/	HC6364/1XQHBT
5962H3829439*--	3/	HC6364
5962H3829440V9C	3/	HC6364/1XVHBC
5962H3829440Q9C	3/	HC6364/1XQHBC
5962H3829441*--	3/	HC6364
5962H3829442V9C	3/	HC6364/1XVHBC
5962H3829442Q9C	3/	HC6364/1XQHBC
5962H3829443V9C	3/	HC6364/1XVHBC
5962H3829443Q9C	3/	HC6364/1XQHBC
5962H3829444V8A	3/	IBM6408C-V55X
5962H3829444Q8A	3/	IBM6408C-Q55X
5962H3829444V9C	3/	LOR6408C-V55Y
5962H3829444Q9C	3/	LOR6408C-Q55Y
5962H3829445V9C	3/	HC6364/2XVHBC
5962H3829445Q9C	3/	HC6364/2XQHBC
5962-3829446MZA	3/ 3DTT2	MT5C6408C-12L P4C164L-12DMB
5962-3829446MUA	3/ 3DTT2	MT5C6408EC-12L P4C164L-12LSMB

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829446MMA	3/ 3DTT2	MT5C6408F-12L P4C164L-12FSMB
5962-3829446MTA	3DTT2	P4C164L-12FMB
5962-3829446MYA	3/	MT5C6408ECW-12L
5962-3829447MZA	3/ 3DTT2	MT5C6408C-12 P4C164-12DMB
5962-3829447MUA	3/ 3DTT2	MT5C6408EC-12 P4C164-12LSMB
5962-3829447MMA	3/ 3DTT2	MT5C6408F-12 P4C164-12FSMB
5962-3829447MTA	3DTT2	P4C164-12FMB
5962-3829447MYA	3/	MT5C6408ECW-12
5962-3829448MXA	3DTT2	P4C164-70DWMB
5962-3829448MYA	3/ 3DTT2	MT5C6408ECW-70 P4C164-70L32MB
5962-3829448MZA	3/ 3DTT2	MT5C6408C-70 P4C164-70DMB
5962-3829448MUA	3/ 3DTT2	MT5C6408EC-70 P4C164-70LSMB
5962-3829448MMA	3/ 3DTT2	MT5C6408F-70 P4C164-70FSMB
5962-3829448MTA	3DTT2	P4C164-70FMB
5962-3829449MXA	3DTT2	P4C164L-55DWMB
5962-3829449MYA	3/ 3DTT2	MT5C6408ECW-55L P4C164L-55L32MB
5962-3829449MZA	3/ 3DTT2	MT5C6408C-55L P4C164L-55DMB
5962-3829449MTA	3DTT2	P4C164L-55FMB
5962-3829449MUA	3/ 3DTT2	MT5C6408ECW-55L P4C164L-55LSMB
5962-3829449MMA	3/ 3DTT2	MT5C6408F-55L P4C164L-55FSMB

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829450MXA	3DTT2	P4C164-55DWMB
5962-3829450MYA	3/ 3DTT2	MT5C6408ECW-55 P4C164-55L32MB
5962-3829450MZA	3/ 3DTT2	MT5C6408C-55 P4C164-55DMB
5962-3829450MUA	3/ 3DTT2	MT5C6408EC-55 P4C164-55LSMB
5962-3829450MMA	3/ 3DTT2	MT5C6408F-55 P4C164-55FSMB
5962-3829450MTA	3DTT2	P4C164-55FMB
5962-3829451MXA	3DTT2	P4C164L-45DWMB
5962-3829451MYA	3/ 3DTT2	MT5C6408ECW-45 P4C164L-45L32MB
5962-3829451MZA	3/ 3DTT2	MT5C6408C-45 P4C164L-45DMB
5962-3829451MUA	3/ 3DTT2	MT5C6408EC-45 P4C164L-45LSMB
5962-3829451MMA	0EU86 3DTT2	MT5C6408F-45 P4C164L-45FSMB
5962-3829451MTA	3DTT2	P4C164L-45FMB
5962-3829452MXA	3DTT2	P4C164-45DWMB
5962-3829452MYA	3/ 3DTT2	MT5C6408ECW-45 P4C164-45L32MB
5962-3829452MZA	3/ 3DTT2	MT5C6408C-45 P4C164-45DMB
5962-3829452MUA	3/ 3DTT2	MT5C6408EC-45 P4C164-45LSMB
5962-3829452MMA	3/ 3DTT2	MT5C6408F-45 P4C164-45FSMB
5962-3829452MTA	3DTT2	P4C164-45FMB

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829453MXA	3DTT2	P4C164L-35DWMB
5962-3829453MYA	3/ 3DTT2	MT5C6408ECW-35L P4C164-35L32MB
5962-3829453MZA	3/ 3DTT2	MT5C6408C-35L P4C164L-35DMB
5962-3829453MUA	3/ 3DTT2	MT5C6408EC-35L P4C164L-35LSMB
5962-3829453MMA	3/ 3DTT2	MT5C6408F-35L P4C164L-35FSMB
5962-3829453MTA	3DTT2	P4C164L-35FMB
5962-3829454MXA	3DTT2	P4C164-35DWMB
5962-3829454MYA	3/ 3DTT2	MT5C6408ECW-35 P4C164-35L32MB
5962-3829454MZA	3/ 3DTT2	MT5C6408C-35 P4C164-35DMB
5962-3829454MUA	3/ 3DTT2	MT5C6408EC-35 P4C164-35LSMB
5962-3829454MMA	3/ 3DTT2	MT5C6408F-35 P4C164-35FSMB
5962-3829454MTA	3DTT2	P4C164-35FMB
5962-3829455MXA	3DTT2	P4C164L-25DWMB
5962-3829455MYA	3/ 3DTT2	MT5C6408ECW-25L P4C164L-25L32MB
5962-3829455MZA	3/ 3DTT2	MT5C6408C-25L P4C164L-25DMB
5962-3829455MUA	3/ 3DTT2	MT5C6408EC-25L P4C164L-25LSMB
5962-3829455MMA	3/ 3DTT2	MT5C6408F-25L P4C164L-25FSMB
5962-3829455MTA	3DTT2	P4C164L-25FMB

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829456MXA	3DTT2	P4C164-25DWMB
5962-3829456MYA	3/ 3DTT2	MT5C6408ECW-25 P4C164-25L32MB
5962-3829456MZA	3/ 3DTT2	MT5C6408C-25 P4C164-25DMB
5962-3829456MUA	3/ 3DTT2	MT5C6408EC-25 P4C164-25LSMB
5962-3829456MMA	3/ 3DTT2	MT5C6408F-25 P4C164-25FSMB
5962-3829456MTA	3DTT2	P4C164-25FMB
5962-3829457MXA	3DTT2	P4C164L-20DWMB
5962-3829457MYA	3/ 3DTT2	MT5C6408ECW-20L P4C164L-20L32MB
5962-3829457MZA	3/ 3DTT2	MT5C6408C-20L P4C164L-20DMB
5962-3829457MUA	3/ 3DTT2	MT5C6408EC-20L P4C164L-20LSMB
5962-3829457MMA	3/ 3DTT2	MT5C6408F-20L P4C164L-20FSMB
5962-3829457MTA	3DTT2	P4C164L-20FMB
5962-3829458MXA	3DTT2	P4C164-20DWMB
5962-3829458MYA	3/ 3DTT2	MT5C6408ECW-20 P4C164-20L32MB
5962-3829458MZA	3/ 3DTT2	MT5C6408C-20 P4C164-20DMB
5962-3829458MUA	3/ 3DTT2	MT5C6408EC-20 P4C164-20LSMB
5962-3829458MMA	3/ 3DTT2	MT5C6408F-20 P4C164-20FSMB
5962-3829458MTA	3DTT2	P4C164-20FMB

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3829459MUA	3DTT2	P4C164-70LMB
5962-3829460MUA	3DTT2	P4C164L-55LMB
5962-3829461MUA	3DTT2	P4C164-55LMB
5962-3829462MUA	3DTT2	P4C164L-45LMB
5962-3829463MUA	3DTT2	P4C164-45LMB
5962-3829464MUA	3DTT2	P4C164L-35LMB
5962-3829465MUA	3DTT2	P4C164-35LMB
5962-3829466MUA	3DTT2	P4C164L-25LMB
5962-3829467MUA	3DTT2	P4C164-25LMB
5962-3829468MUA	3DTT2	P4C164-20LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for the part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology, Inc. 6024 Silver Creek Valley Road San Jose, CA 95138
3DTT2	Pyramid Semiconductor Corp. 1340 Bordeaux Drive Sunnyvale, CA 94089
0C7V7QP	Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

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