REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Made technical change in table I. Added test circuit and switching waveforms. Editorial changes throughout.	89-12-07	W. Heckman
B	Change IAW NOR No. 5962-R151-93 adding footnote 2/ to table I. Editorial changes throughout. - tvn	93-05-05	Monica L. Poelking
C	Update to reflect latest changes in format and requirements. Editorial changes throughout. - les	02-03-20	Raymond Monnin
D	Update drawing to current requirements. Editorial changes throughout. - gap	09-04-14	Joseph D. Rodenbeck

The original first sheet of this drawing has been replaced.

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

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DRAWING APPROVAL DATE
87-12-14

REVISION LEVEL
D

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED SCHOTTKY, TTL, REGISTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-86074**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-86074	01	R	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54F322	8-bit serial/parallel register with sign extend and three-state outputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line package
S	GDFP2-F20 or CDFP3-F20	20	Flat package
2	CQCC1-N20	20	Square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -18 mA to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) per device 1/	495 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Setup time, high $\overline{RE}$ to CP (t_s)	8.0 ns minimum
Setup time, low $\overline{RE}$ to CP (t_s)	18.0 ns minimum
Hold time, high or low, $\overline{RE}$ to CP (t_h)	0 ns minimum
Setup time, high or low, D_0, D_1, or I/O_n to CP (t_s)	8.5 ns minimum
Hold time, high or low, D_0, D_1, or I/O_n to CP (t_h)	3.0 ns minimum

1/ Maximum power dissipation is defined as V_{CC} x I_{CC}. Must withstand the added P_D due to short circuit test (e.g. I_{OS}).

Setup time, high $\overline{SE}$ to CP (t_s)	9.0 ns minimum
Setup time, low $\overline{SE}$ to CP (t_s)	4.5 ns minimum
Hold time, high $\overline{SE}$ to CP (t_h)	2.0 ns minimum
Hold time, low $\overline{SE}$ to CP (t_h)	0 ns minimum
Setup time, high S/$\overline{P}$ to CP (t_s)	13 ns minimum
Setup time, low S/$\overline{P}$ to CP (t_s)	21 ns minimum
Setup time, high S to CP (t_s)	8.5 ns minimum
Setup time, low S to CP (t_s)	11 ns minimum
Hold time, high or low, S or S/$\overline{P}$ to CP (t_h)	0 ns minimum
Clock pulse width high (t_w)	8 ns minimum
$\overline{MR}$ pulse width low (t_w)	7.5 ns minimum
Recovery time, $\overline{MR}$ to CP	9.5 ns minimum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -3.0 mA, V_{IN} = 0.8 V or 2.0 V		1, 2, 3	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IN} = 0.8 V or 2.0 V		1, 2, 3		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IH} = -18 mA, T_C = +25°C		1		-1.2	V
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V		1, 2, 3		20	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	I/O inputs	1, 2, 3		1.0	mA
	I_{IH3}	V_{CC} = 5.5 V, V_{IN} = 7.0 V	All other inputs	1, 2, 3		100	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.5 V	$\overline{SE}$ input	1, 2, 3		-1.8	mA
			S input	1, 2, 3		-1.2	mA
			Other inputs	1, 2, 3		-0.6	mA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = GND 1/		1, 2, 3	-60	-150	mA
Off-state output current, high level voltage applied	I_{OZH}	V_{CC} = 5.5 V, V_{OUT} = 2.4 V		1, 2, 3		70	µA
Off-state output current, low level voltage applied	I_{OZL}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V		1, 2, 3		-650	µA
Supply current	I_{CC}	V_{CC} = 5.5 V Clock high output disabled		1, 2, 3		90	mA
Functional tests		See 4.3.1c		7			
Maximum clock frequency	f_{MAX} 2/	V_{CC} = 5.0 V		9	70		MHz
		R_L = 500 Ω ±5%		10, 11	50		MHz
Propagation delay time, CP to I/O_n	t_{PLH1}	C_L = 50 pF ±10%		9		8	ns
				10, 11		10	ns
	t_{PHL1}			9		8	ns
				10, 11		10	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay time, CP to Q_{0n}	t_{PLH2}	V_{CC} = 5.0 V R_L = 500 Ω ±5% C_L = 50 pF ±10%	9		9	ns
			10, 11		11	ns
	t_{PHL2}		9		8	ns
			10, 11		10	ns
Propagation delay time, $\overline{MR}$ to I/O_n	t_{PHL3}		9		13	ns
			10, 11		15	ns
Propagation delay time, $\overline{MR}$ to Q_0	t_{PHL4}		9		12	ns
			10, 11		14	ns
Output enable time, $\overline{OE}$ to I/O_n	t_{PZH1}		9		9	ns
			10, 11		13	ns
	t_{PZL1}		9		11	ns
			10, 11		15	ns
Output disable time, $\overline{OE}$ to I/O_n	t_{PHZ1}		9		6	ns
			10, 11		8	ns
	t_{PLZ1}		9		7	ns
			10, 11		10	ns
Output enable time, $S/\overline{P}$ to I/O_n	t_{PZH2}		9		11	ns
			10, 11		14	ns
	t_{PZL2}		9		14	ns
			10, 11		17	ns
Output disable time, $S/\overline{P}$ to I/O_n	t_{PHZ2}		9		12	ns
			10, 11		17	ns
	t_{PLZ2}		9		16	ns
			10, 11		20	ns

1/ Not more than one output will be tested at one time and the duration of the test condition shall not exceed 1 second.

2/ f_{MAX}, if not tested, shall be guaranteed to the specified limits.

Device type 01		
Case outlines	R and S	2
Terminal number	Terminal symbols	
1	$\overline{RE}$	$\overline{RE}$
2	S/$\overline{P}$	S/$\overline{P}$
3	D_0	D_0
4	I/O_7	I/O_7
5	I/O_5	I/O_5
6	I/O_3	I/O_3
7	I/O_1	I/O_1
8	$\overline{OE}$	$\overline{OE}$
9	$\overline{MR}$	$\overline{MR}$
10	GND	GND
11	CP	CP
12	Q_0	Q_0
13	I/O_0	I/O_0
14	I/O_2	I/O_2
15	I/O_4	I/O_4
16	I/O_6	I/O_6
17	D_1	D_1
18	$\overline{SE}$	$\overline{SE}$
19	S	S
20	V_{CC}	V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

Mode	Inputs							Outputs								
	$\overline{MR}$	$\overline{RE}$	S/$\overline{P}$	$\overline{SE}$	S	$\overline{OE}$ *	CP	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Q_0
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel load	H	L	L	X	X	X	↑	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	I_0
Shift right	H	L	H	H	L	L	↑	D_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
	H	L	H	H	H	L	↑	D_1	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Sign Extend	H	L	H	L	X	L	↑	O_7	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_1
Hold	H	H	X	X	X	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC

* When the $\overline{OE}$ input is high, all I/O_n terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

NOTES:
1. I_7-I_0 = The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the I/O terminal.
2. D_0, D_1 = The level of the steady-state inputs to the serial multiplexer input.
3. O_7-O_0 = The level of the respective Q_n flip-flop prior to the last clock low-to-high transition.
4. NC = no change; Z = high-impedance output state; H = high voltage level; L = low voltage level; ↑ = low-to-high clock transition.

FIGURE 2. Truth table.

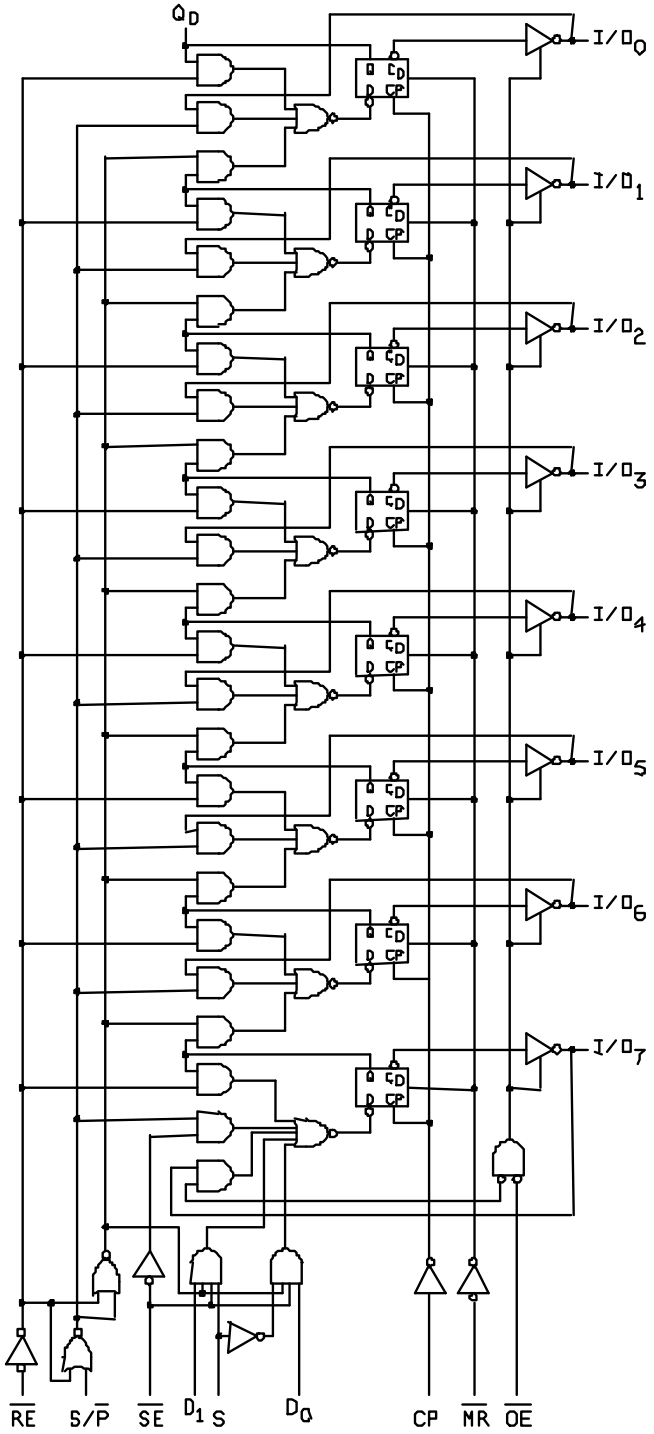
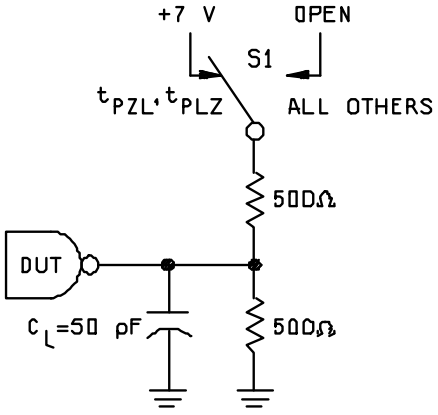
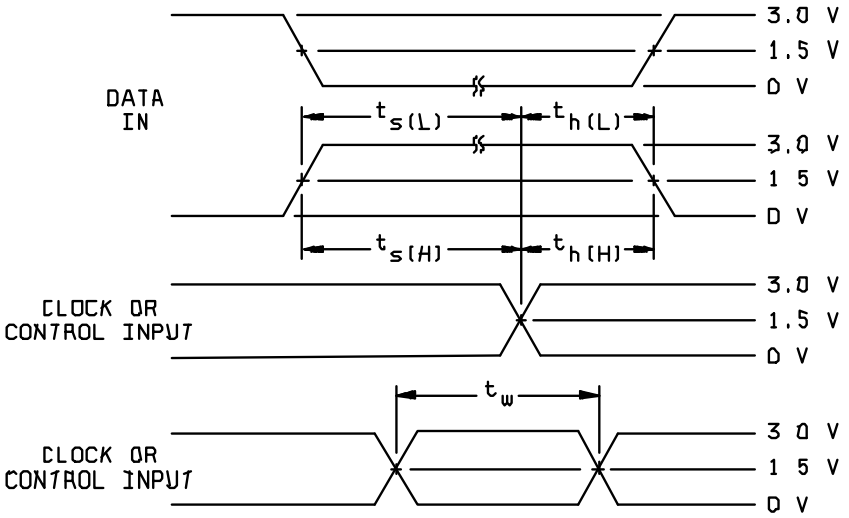


FIGURE 3. Logic diagram.

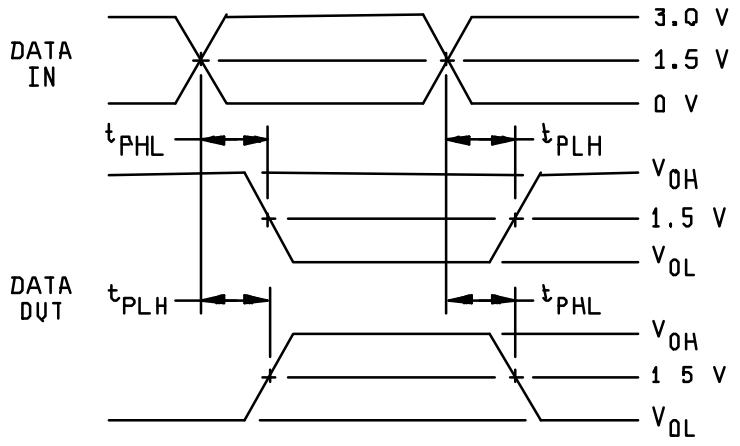




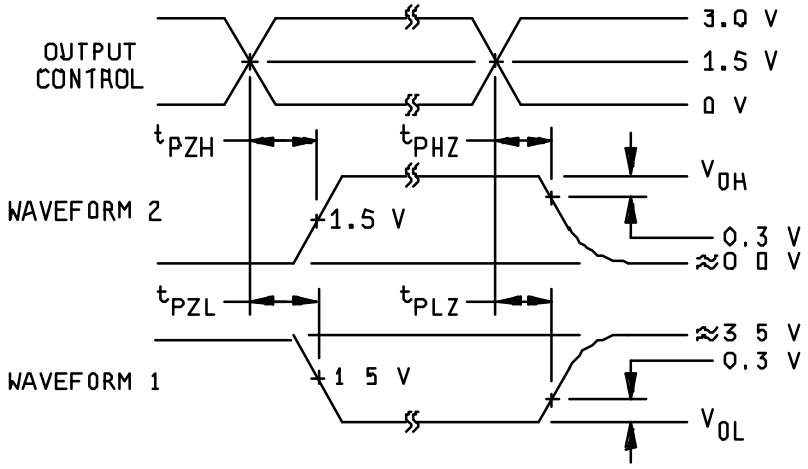
SETUP TIME, HOLD TIME
AND PULSE WIDTHS

See notes at end of next page.

FIGURE 5. Test circuit and switching waveforms.



PROPAGATION DELAY TIME



THREE-STATE OUTPUT HIGH AND LOW ENABLE AND DISABLE TIMES

Notes:
1. C_L = Includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses have the following characteristics: PRR = 1 MHz, $t_r = t_f$ = 2.5 ns, duty cycle = 50%.
4. When measuring propagation delay times of three-state outputs, switch S1 is open.
5. When measuring pulse widths $t_r = t_f \leq 1$ ns.
6. The outputs are measured one at a time with one input transition per measurement.

FIGURE 4. Switching waveforms and test circuit - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 09-04-14

Approved sources of supply for SMD 5962-86074 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8607401RA	0C7V7	54F322DMQB
5962-8607401SA	0C7V7	54F322FMQB
5962-86074012A	0C7V7	54F322LMQB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

X-ON Electronics

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