REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline "U" to the drawing. Change to parameter tWHAX of table I. Editorial change throughout.	89-10-30	Michael A. Frye
B	Changes in accordance with NOR 5962-R004-91	91-09-20	Michael A. Frye
C	Redrawn with changes. Added device types 19 through 22. Added vendor CAGE 65786 for device types 19 and 20.. Added vendor CAGE 61772 for devices 21 and 22. Corrected errors to Table I. Added pin 1 reference to case outline U. Editorial changes throughout.	93-04-28	Michael A. Frye
D	Boilerplate update, part of 5 year review. ksr	06-08-08	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D	D	D	D	D	D							
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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APPROVED BY
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DRAWING APPROVAL DATE
88-05-11

REVISION LEVEL
D

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 1K X 8 DUAL PORT STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-86875**

SHEET 1 OF 27

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-86875	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		1K x 8 bit dual port CMOS SRAM (Master)	90 ns
02		1K x 8 bit dual port CMOS SRAM (Master)	70 ns
03		1K x 8 bit dual port CMOS SRAM (Master)	55 ns
04		1K x 8 bit dual port CMOS SRAM (Master)	45 ns
05		1K x 8 bit dual port CMOS SRAM (Master)	90 ns (data retention)
06		1K x 8 bit dual port CMOS SRAM (Master)	70 ns (data retention)
07		1K x 8 bit dual port CMOS SRAM (Master)	55 ns (data retention)
08		1K x 8 bit dual port CMOS SRAM (Master)	45 ns (data retention)
09		1K x 8 bit dual port CMOS SRAM (Slave)	90 ns
10		1K x 8 bit dual port CMOS SRAM (Slave)	70 ns
11		1K x 8 bit dual port CMOS SRAM (Slave)	55 ns
12		1K x 8 bit dual port CMOS SRAM (Slave)	45 ns
13		1K x 8 bit dual port CMOS SRAM (Slave)	90 ns (data retention)
14		1K x 8 bit dual port CMOS SRAM (Slave)	70 ns (data retention)
15		1K x 8 bit dual port CMOS SRAM (Slave)	55 ns (data retention)
16		1K x 8 bit dual port CMOS SRAM (Slave)	45 ns (data retention)
17		1K x 8 bit dual port CMOS SRAM (Master)	35 ns
18		1K x 8 bit dual port CMOS SRAM (Slave)	35 ns
19		1K x 8 bit dual port CMOS SRAM (Master)	35 ns
20		1K x 8 bit dual port CMOS SRAM (Slave)	35 ns
21		1K x 8 bit dual port CMOS SRAM (Master)	35 ns (data retention)
22		1K x 8 bit dual port CMOS SRAM (Slave)	35 ns (data retention)

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T48 or CDIP2-T48	48	dual-in-line
Y	See figure 1	48	square leadless chip carrier
Z	CQCC1-N52	52	square leadless chip carrier
U	See figure 1	48	flat pack

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.

1.3 Absolute maximum ratings. 2/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +7.0 V dc
Output sink current	50 mA
Output short circuit duration	10 seconds
Power dissipation (P_D)	1.5 W
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	30°C/W 3/
Case Y and U	12°C/W 3/
Case Z	See MIL-STD-1835
Junction temperature	+150°C 4/
Temperature under bias	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions. 2/

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum input high voltage level (V_{IH})	2.2 V
Maximum input low voltage level (V_{IL})	0.8 V

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

2/ Unless otherwise specified, all voltages are referenced to ground (GND).

3/ When a thermal resistance value for this case outline is included in MIL-STD-1835, that value shall supersede the value specified herein.

4/ Maximum junction temperature may be increased to 175°C during the burn-in and steady state life test.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth tables. The truth tables shall be as specified on figure 3.

3.2.4 Block diagram. The block diagram shall be as specified on figure 4.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_O = -4.0 mA, V_{IH} = 2.2 V, V_{IL} = 0.8 V	1, 2, 3	All	2.4		V
Low level output voltage (I/O_0 - I/O_7 terminals only)	V_{OL1}	I_O = 4.0 mA, V_{IH} = 2.2 V, V_{IL} = 0.8 V	1, 2, 3	All		0.4	V
Low level open drain output voltage ($\overline{BUSY}_L$, $\overline{BUSY}_R$, $\overline{INT}_L$, and $\overline{INT}_R$ terminals only)	V_{OL2}	I_O = 16 mA	1, 2, 3	All		0.5	V
High impedance output leakage current	I_{OZ}	$\overline{CE}$ = V_{IH}, V_O = GND to V_{CC}	1, 2, 3	All	-10.0	10.0	µA
High level input voltage	V_{IH}		1, 2, 3	All	2.2		V
Low level input voltage	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IH}	V_{IH} = 5.5 V	1, 2, 3	All		10.0	µA
	I_{IL}	V_{IL} = GND	1, 2, 3	All	-10.0		µA
Operating supply current (standby)	I_{SB1}	$\overline{CE}_L$ = $\overline{CE}_R \ge V_{IH}$, both ports standby, V_{CC} = 5.5 V	1, 2, 3	01-04, 09-12, 19-20		65	mA
				06-08, 14-16		55	
				05, 13, 17, 18		45	
				21, 22		60	
	I_{SB2}	$\overline{CE}_L$ = $\overline{CE}_R \ge V_{IH}$, one port standby, active port outputs open, V_{CC} = 5.5 V	1, 2, 3	02- 04, 10-12		135	mA
				01, 09, 19, 20		125	
				06-08, 14-16		110	
				05, 13, 17, 18		100	
				21, 22		150	

See footnotes a end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Operating supply current (full standby)	I_{SB3}	$\overline{CE}_L = \overline{CE}_R \ge V_{CC} - 0.2\ V$, $V_{CC} = 5.5\ V$, $V_{IN} \le 0.2\ V$ or $V_{IN} \ge V_{CC} - 0.2\ V$, both ports full standby	1, 2, 3	01-04, 09-12, 17-20		30	mA
				05-08, 13-16, 21, 22		10	
	I_{SB4}	$\overline{CE}_L = \overline{CE}_R \ge V_{CC} - 0.2\ V$, $V_{CC} = 5.5\ V$, $V_{IN} \le 0.2\ V$ or $V_{IN} \ge V_{CC} - 0.2\ V$, one ports full standby, active port outputs open	1, 2, 3	21, 22		140	mA
				04, 12		125	
				03, 11		120	
				02, 10		115	
				01, 09, 19, 20		110	
				08, 16		95	
				07, 15		90	
				06, 14		85	
				05, 13, 17, 18		80	
Operating supply current (dynamic)	I_{CC}	$\overline{CE}_L = \overline{CE}_R = V_{IL}$, $V_{CC} = 5.5\ V$, f = 1MHz, both ports active	1, 2, 3	03, 04, 11, 12, 21, 22		230	mA
				02, 10		225	
				01, 09		200	
				07, 08, 15, 16		185	
				06, 14, 19, 20		180	
				05, 13		160	
				17, 18		150	
V_{CC} for data retention	V_{DR}	$V_{CC} = 2.0\ V$, $\overline{CE} \ge V_{CC} - 0.2\ V$, $V_{IN} \ge V_{CC} - 0.2\ V$ or $V_{IN} \le 0.2\ V$	1, 2, 3	05-08, 13-16, 21, 22	2.0		V
Data retention current	I_{CCDR}		1, 2, 3	05-08, 13-16, 21, 22		4.0	mA
Chip deselect to data retention time 3/	t_{CDR}	$V_{CC} = 2.0\ V$, $\overline{CE} \ge V_{CC} - 0.2\ V$, $V_{IN} \ge V_{CC} - 0.2\ V$ or $V_{IN} \le 0.2\ V$	1, 2, 3	05-08, 13-16, 21, 22	0		ns
Operation recovery time 3/	t_R	$V_{CC} = 2.0\ V$, $\overline{CE} \ge V_{CC} - 0.2\ V$, $V_{IN} \ge V_{CC} - 0.2\ V$ or $V_{IN} \le 0.2\ V$	1, 2, 3	05, 13	90		ns
				06, 14	70		
				07, 15	55		
				08, 16	45		
				21, 22	35		

See footnotes a end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance 4/ 5/	C_{IN}	f = 1 MHz, $V_{IN} = V_{CC}$ or GND, see 4.3.1c, $T_A = 25°C$	4	All		12	pF
Output capacitance 4/ 5/	C_{OUT}	f = 1 MHz, $V_{IN} = V_{CC}$ or GND, see 4.3.1c, $T_A = 25°C$	4	01-20		10	pF
				21, 22		11	
Functional tests		See 4.3.1d	7, 8A, 8B	All			
Read cycle							
Read cycle time	t_{AVAV}	6/	9, 10, 11	17-22	35		ns
				04, 08, 12, 16	45		
				01, 05, 09, 13	90		
				02, 06, 10, 14	70		
				03, 07, 11, 15	55		
Address access time	t_{AVQV}	6/	9, 10, 11	17-22		35	ns
				04, 08, 12, 16		45	
				01, 05, 09, 13		90	
				02, 06, 10, 14		70	
				03, 07, 11, 15		55	
Output hold from address change	t_{AXQX}	6/	9, 10, 11	17, 18	3		ns
				01, 05, 09, 13	10		
				02-04, 06-08, 10-12, 14-16, 19-22	0		
Output enable access time	t_{OLQV}	6/	9, 10, 11	17, 18		15	ns
				01, 02, 05, 06, 09, 10, 13, 14		40	
				03, 07, 11, 15		35	
				04, 08, 12, 16		30	
				21, 22		25	
				19, 20		20	

See footnotes a end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle							
Output enable to output active 3/ 7/	t_{OELZ}	6/	9, 10, 11	All	3		ns
Output enable high to high Z 3/ 7/ 8/	t_{OEHZ}	6/	9, 10, 11	17, 18, 21, 22		15	ns
				01, 05, 09, 13		40	
				02, 06, 10, 14		35	
				03, 07, 11, 15		30	
				04, 08, 12, 16, 19, 20		20	
Chip enable to output active 3/ 7/	t_{CELZ}	6/	9, 10, 11	All	5		ns
Output enable high to high Z 3/ 7/ 8/	t_{CEHZ}	6/	9, 10, 11	17, 18, 21, 22		15	ns
				01, 05, 09, 13		40	
				02, 06, 10, 14		35	
				03, 07, 11, 15		30	
				04, 08, 12, 16, 19, 20		20	
Chip enable to output valid	t_{ELQV}	6/	9, 10, 11	17-22		35	ns
				04, 08, 12, 16		45	
				01, 05, 09, 13		90	
				02, 06, 10, 14		70	
				03, 07, 11, 15		55	
Chip enable low to power up 3/	t_{PU}	6/	9, 10, 11	All	0		ns
Chip enable high to power down 3/	t_{PD}	6/	9, 10, 11	All		50	ns

See footnotes a end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle							
Write recovery time	t_{WHAX}	6/	9, 10, 11	01-20	2		ns
				21, 22	0		
Chip enable to end-of-write	t_{ELWH}	6/	9, 10, 11	17-22	30		ns
				01, 05, 09, 13	85		
				02, 06, 10, 14	50		
				03, 07, 11, 15	40		
				04, 08, 12, 16	35		
Address setup time	t_{AVWL}	6/	9, 10, 11	01-20	2		ns
				21, 22	0		
Write pulse width	t_{WLWH}	6/	9, 10, 11	17, 18	20		ns
				04, 08, 12, 16	35		
				01, 05, 09, 13	60		
				02, 06, 10, 14	50		
				03, 07, 11, 15	40		
				21, 22	30		
				19, 20	25		
Data valid to end-of-write	t_{DVWH}	6/	9, 10, 11	17-20	15		ns
				04, 08, 12, 16	20		
				01, 05, 09, 13	40		
				02, 06, 10, 14	30		
				03, 07, 11, 15, 21, 22	20		
Write enable to output in high impedance state 3/ 7/ 8/	t_{WLQZ}	6/	9, 10, 11	17, 18, 21, 22		15	ns
				04, 08, 12, 16, 19, 20		20	
				01, 05, 09, 13		40	
				02, 06, 10, 14		35	
				03, 07, 11, 15		30	

See footnotes a end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle							
Data hold time	t_{WHDX}	6/	9, 10, 11	All	0		ns
End-of-write to data active 3/ 7/ 8/	t_{WHQX}	6/	9, 10, 11	All	0		ns
Address valid to end-of-write	t_{AVWH}	6/	9, 10, 11	17-22	30		ns
				01, 05, 09, 13	85		
				02, 06, 10, 14	50		
				03, 07, 11, 15	40		
				04, 08, 12, 16	35		
BUSY timing							
Address match to $\overline{BUSY}$ state	t_{BAA}	6/ 9/	9, 10, 11	17, 19		20	ns
				04, 08, 21		35	
				01-03, 05-07		45	
Chip enable to $\overline{BUSY}$ state	t_{BAC}	6/ 9/	9, 10, 11	17, 19		20	ns
				04, 08, 21		30	
				01, 05		45	
				02, 03, 06, 07		35	
Address no match to not $\overline{BUSY}$ state	t_{BDA}	6/ 9/	9, 10, 11	17, 19		20	ns
				21		30	
				04, 08		35	
				01, 05		45	
				02, 03, 06, 07		40	

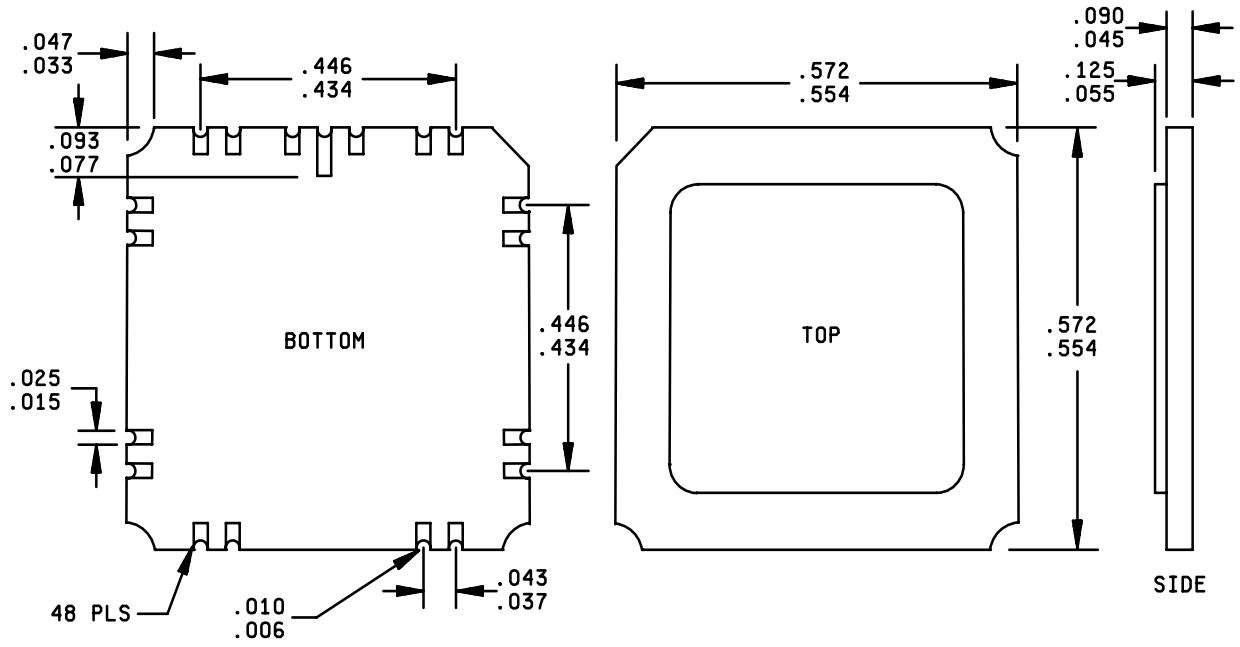
See footnotes a end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
BUSY timing							
Chip disable to not BUSY state	t_{BDC}	6/ 9/	9, 10, 11	17, 19		20	ns
				04, 08, 21		25	
				01, 05		45	
				02, 03, 06, 07		30	
Address arbitration priority setup time	t_{APS}	6/ 9/	9, 10, 11	01-08, 17, 19, 21	5		ns
Interrupt timing							
Interrupt setup time	t_{INS}	6/ 9/ 10/	9, 10, 11	17-20		25	ns
				21, 22		35	
				04, 08, 12, 16		40	
				01, 05, 09, 13		55	
				02, 06, 10, 14		50	
				03, 07, 11, 15		45	
Interrupt reset time	t_{INR}	6/ 9/ 10/	9, 10, 11	17, 18		15	ns
				04, 08, 12, 16		40	
				01, 05, 09, 13		55	
				02, 06, 10, 14		50	
				03, 07, 11, 15		45	
				21, 22		35	
				19, 20		25	

1/ All voltages referenced to GND. Negative undershoots to a minimum of -0.3 V are allowed with a maximum of 50 ns pulse width.
2/ Timing diagrams are as specified on figure 5. Unless indicated under conditions, the switching times test circuit is as indicated on figure 6a.
3/ May not be tested, but shall be guaranteed to the limits specified in table I.
4/ Effective capacitance calculated from $C = \Delta Q/\Delta V$ with $\Delta V = 3$ volts and $V_{CC} = 5.0$ V, or measured with capacitance meter.
5/ Tested only initially and after any design changes.
6/ A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
7/ Transition is measured ±500 mV from low or high impedance voltage with load, reference figure 6b.
8/ Switching times test circuit as indicated on figure 6b.
9/ Switching times test circuit as indicated on figure 6c.
10/ The left port interrupt is set when the right port writes to memory location 3FE (Hex) and is reset when the left port reads from 3FE. The right port interrupt is set when the left port writes to memory location 3FF (Hex) and is reset when the right port reads from location 3FF.

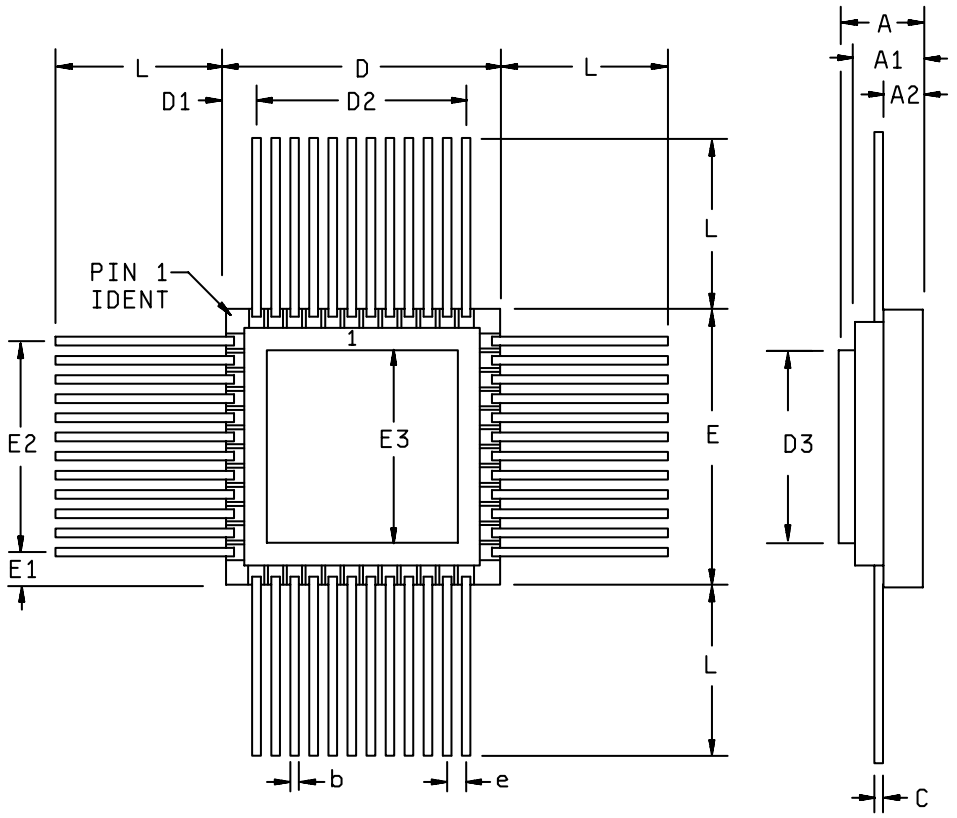
Case outline Y



Inches	Millimeters	Inches	Millimeters
.006	.15	.055	1.40
.010	.25	.077	1.96
.015	.38	.090	2.29
.025	.64	.093	2.36
.033	.84	.125	3.18
.037	.94	.434	11.02
.043	1.09	.446	11.33
.045	1.14	.554	14.07
.047	1.19	.572	14.53

FIGURE 1. Case outline.

Case outline U



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.089	.108	2.26	2.74
A1	.079	.096	2.01	2.44
A2	.058	.073	1.47	1.85
B	.018	.022	0.46	0.56
C	.008	.010	0.20	0.25
D		.750		19.05
D1	.100 REF		2.54	
D2	.550 BSC		13.97	
D3		.630		16.00
e	.050 BSC		1.27	
E		.750		19.05
E1	.100 REF		2.54	
E2	.550 BSC		13.97	
E3		.630		16.00
L	.350	.450	8.89	11.43
ND	12			
NE	12			

FIGURE 1. Case outline - Continued.

Device types	All		Device types	All	
Case outlines	X, Y, and U	Z	Case outline	X, Y, and U	Z
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
1	$\overline{CE}_L$	$\overline{CE}_L$	27	I/O_{2R}	I/O_{0R}
2	$R/\overline{W}_L$	$R/\overline{W}_L$	28	I/O_{3R}	I/O_{1R}
3	$\overline{BUSY}_L$	$\overline{BUSY}_L$	29	I/O_{4R}	I/O_{2R}
4	$\overline{INT}_L$	$\overline{INT}_L$	30	I/O_{5R}	I/O_{3R}
5	$\overline{OE}_L$	NC	31	I/O_{6R}	I/O_{4R}
6	A_{0L}	$\overline{OE}_L$	32	I/O_{7R}	I/O_{5R}
7	A_{1L}	A_{0L}	33	A_{9R}	I/O_{6R}
8	A_{2L}	A_{1L}	34	A_{8R}	I/O_{7R}
9	A_{3L}	A_{2L}	35	A_{7R}	NC
10	A_{4L}	A_{3L}	36	A_{6R}	A_{9R}
11	A_{5L}	A_{4L}	37	A_{5R}	A_{8R}
12	A_{6L}	A_{5L}	38	A_{4R}	A_{7R}
13	A_{7L}	A_{6L}	39	A_{3R}	A_{6R}
14	A_{8L}	A_{7L}	40	A_{2R}	A_{5R}
15	A_{9L}	A_{8L}	41	A_{1R}	A_{4R}
16	I/O_{0L}	A_{9L}	42	A_{0R}	A_{3R}
17	I/O_{1L}	I/O_{0L}	43	$\overline{OE}_R$	A_{2R}
18	I/O_{2L}	I/O_{1L}	44	$\overline{INT}_R$	A_{1R}
19	I/O_{3L}	I/O_{2L}	45	$\overline{BUSY}_R$	A_{0R}
20	I/O_{4L}	I/O_{3L}	46	$R/\overline{W}_R$	$\overline{OE}_R$
21	I/O_{5L}	I/O_{4L}	47	$\overline{CE}_R$	NC
22	I/O_{6L}	I/O_{5L}	48	V_{CC}	$\overline{INT}_R$
23	I/O_{7L}	I/O_{6L}	49	---	$\overline{BUSY}_R$
24	GND	I/O_{7L}	50	---	$R/\overline{W}_R$
25	I/O_{0R}	NC	51	---	$\overline{CE}_R$
26	I/O_{1R}	GND	52	---	V_{CC}

NOTE: An "L" suffix on a terminal indicates it applies to the "left" port, an "R" indicates it applies to the "right" port.

FIGURE 2. Terminal connections.

Noncontention read/write control 1/

Left port inputs			Right port inputs			Flags 2/		Function
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	H	X	X	X	X	H	H	Left port in power down mode
X	X	X	X	H	X	H	H	Right port in power down mode
L	L	X	X	X	X	H	H	Data on left port written in memory
H	L	L	X	X	X	H	H	Data in memory output on left mode
X	X	X	L	L	X	H	H	Data on right port written in memory
X	X	X	H	L	L	H	H	Data in memory output on right mode

See footnotes at end of figure.

Interrupt flag control 1/

Left port					Right port					Function
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A0_L$-$A9_L$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A0_R$-$A9_R$	$\overline{INT}_R$	
L	L	X	3FF	X	X	X	X	X	L	Set right $\overline{INT}_R$ flag
X	X	X	X	X	H	L	L	3FF	H	Reset right $\overline{INT}_R$ flag
X	X	X	X	L	L	L	X	3FE	X	Set left $\overline{INT}_L$ flag
H	L	X	3FE	H	X	X	X	X	X	Reset left $\overline{INT}_L$ flag

See footnotes at end of figure.

FIGURE 3. Truth table.

$\overline{CE}$ arbitration with address match before $\overline{CE}$ 1/ 3/

Left port				Right port				Flags 4/		Function
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A0_L$-$A9_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A0_R$-$A9_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	LBR	X	MATCH	X	L	X	MATCH	H	L	Left operation permitted. Right operation not permitted
X	L	X	MATCH	X	LBL	X	MATCH	L	H	Left operation not permitted. Right operation permitted
X	LST	X	MATCH	X	LST	X	MATCH	H	L	Arbitration resolved
X	LST	X	MATCH	X	LST	X	MATCH	L	H	Arbitration resolved

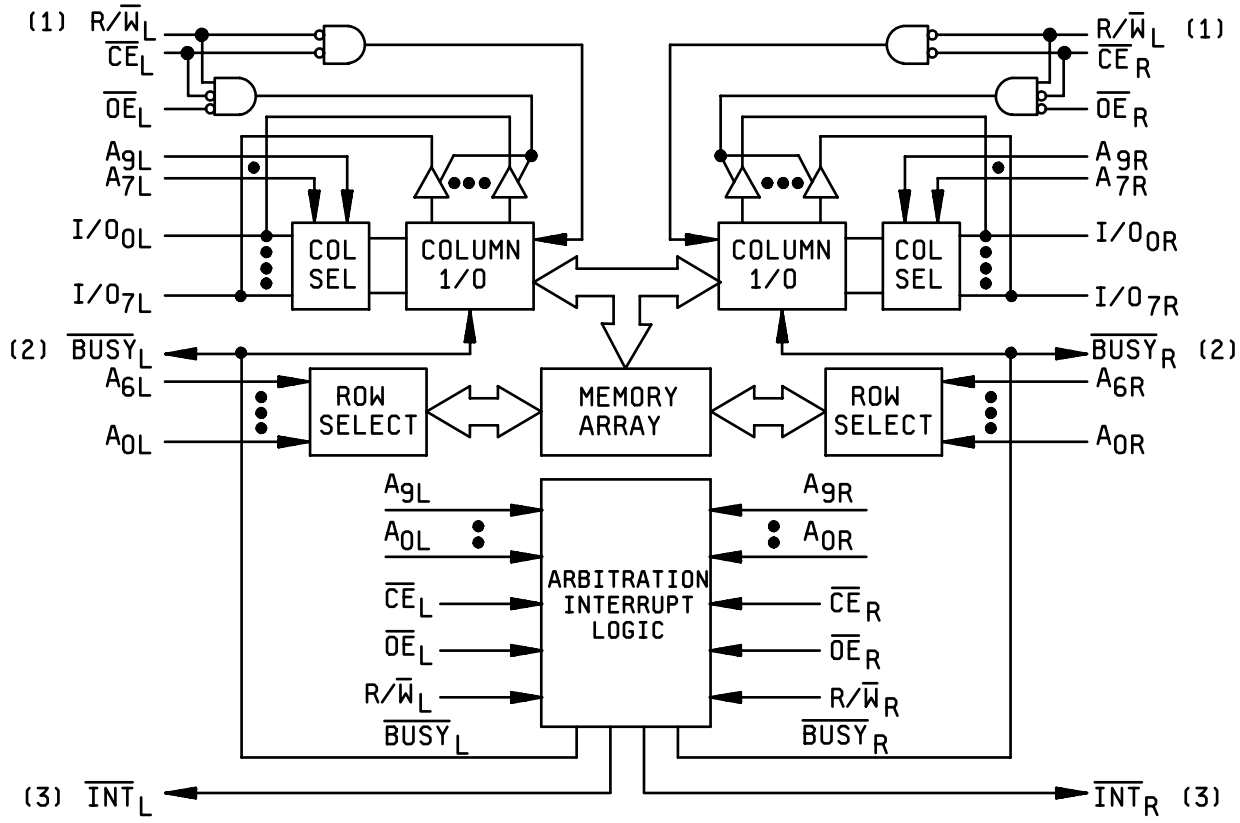
See footnotes at end of figure.

Address arbitration with $\overline{CE}$ low before address match 1/ 5/ 6/

Left port				Right port				Flags 2/		Function
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A0_L$-$A9_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A0_R$-$A9_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	L	X	YBR	X	L	X	VALID	H	L	Left operation permitted. Right operation not permitted
X	L	X	VALID	X	L	X	VBL	L	H	Left operation not permitted. Right operation permitted
X	L	X	VST	X	L	X	VST	H	L	Arbitration resolved
X	L	X	VST	X	L	X	VST	L	H	Arbitration resolved

1/ X = don't care, H = logic 1 state, L = logic 0 state, LST = left and right, $\overline{CE}$ = low within 5 ns of each other.
2/ $\overline{INT}$ flags = logic DON'T CARE state.
3/ LBR = left $\overline{CE}$ = low $\geq$ 5 ns before right $\overline{CE}$. LBL = right $\overline{CE}$ = low $\geq$ 5 ns before left $\overline{CE}$.
4/ $A0_L - A9_L \neq A0_R - A9_R$.
5/ VST = left and right addresses match within 5 ns of each other. VBR = left addresses valid $\geq$ 5 ns before right address.
6/ VBL = right address valid $\geq$ 5 ns before left address.

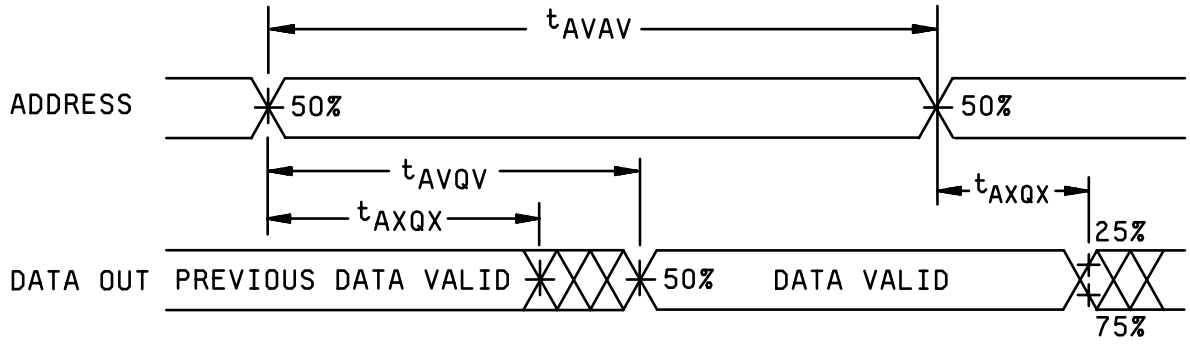
FIGURE 3. Truth table - Continued.



NOTES:
1. An "L" suffix on a terminal indicates it applies to the "left" port, an "R" indicates it applies to the "right" port.
2. These signals are outputs on device types 01 through 08, 17, 19 and 21 and inputs on device types 09 through 16, 18, 20, and 22. On device types 01 through 08, 17, 19, and 21 these signals are open drain and require pull-up resistors.
3. Open drain outputs: Pull-up resistor required.

FIGURE 4. Block diagram.

READ CYCLE 1: SEE NOTES 1, 2, AND 6



READ CYCLE 2: SEE NOTES 1 AND 3

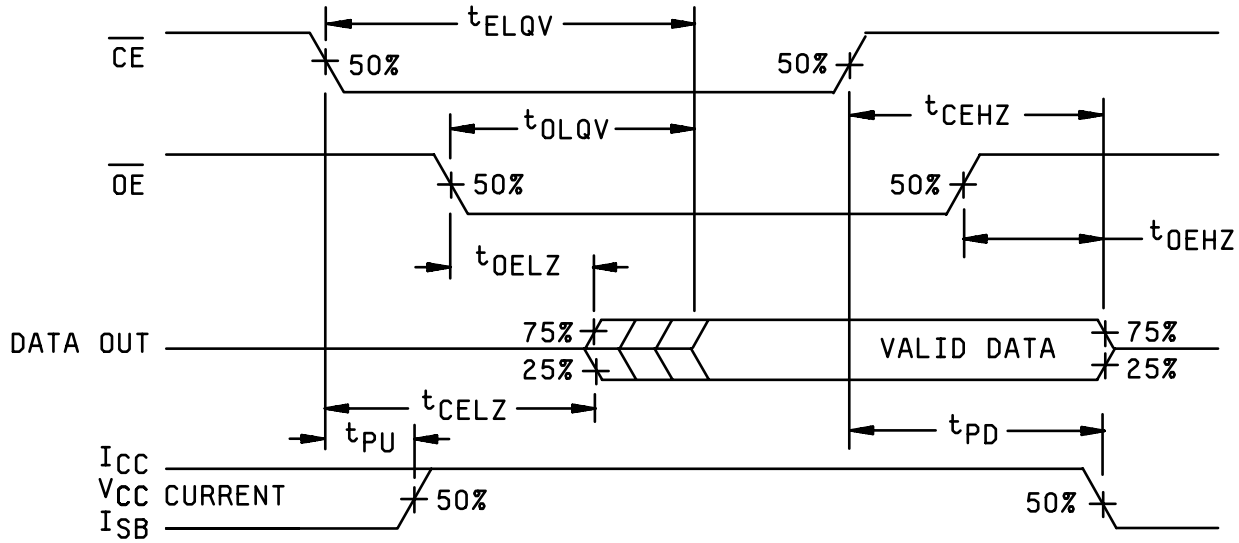


FIGURE 5. Timing waveform diagram.

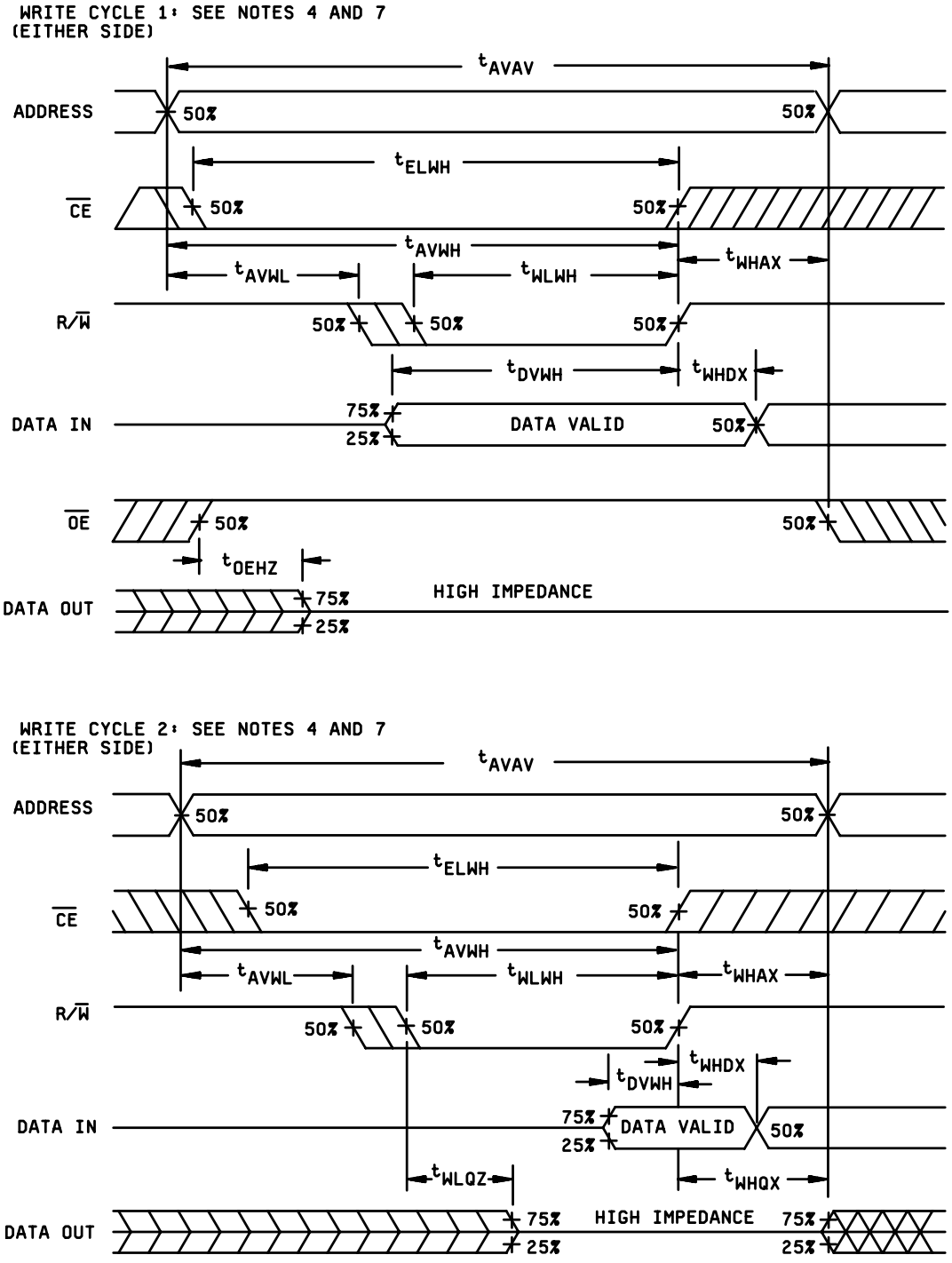
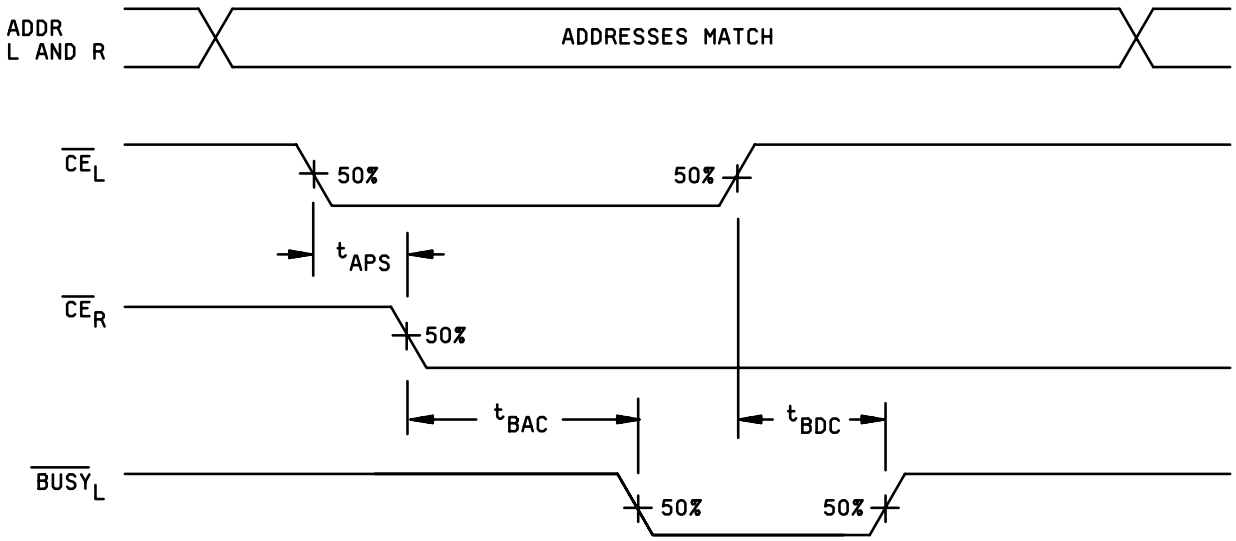


FIGURE 5. Timing waveform diagram - Continued.

CONTENTION CYCLE 1: CE ARBITRATION

$\overline{CE}_L$ VALID FIRST



$\overline{CE}_R$ VALID FIRST

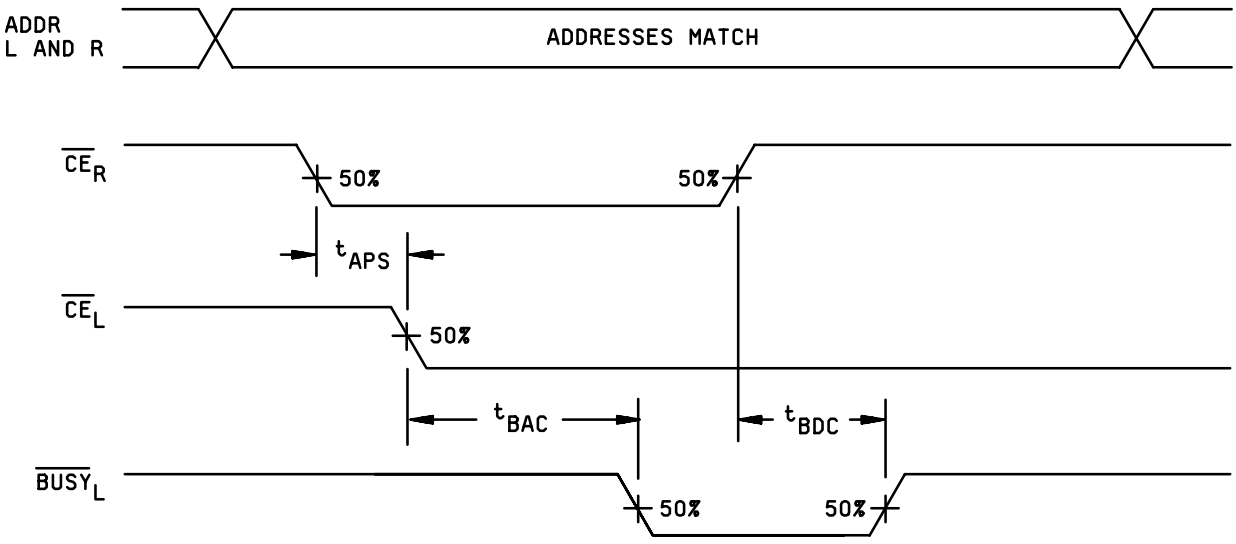


FIGURE 5. Timing waveform diagram - Continued.

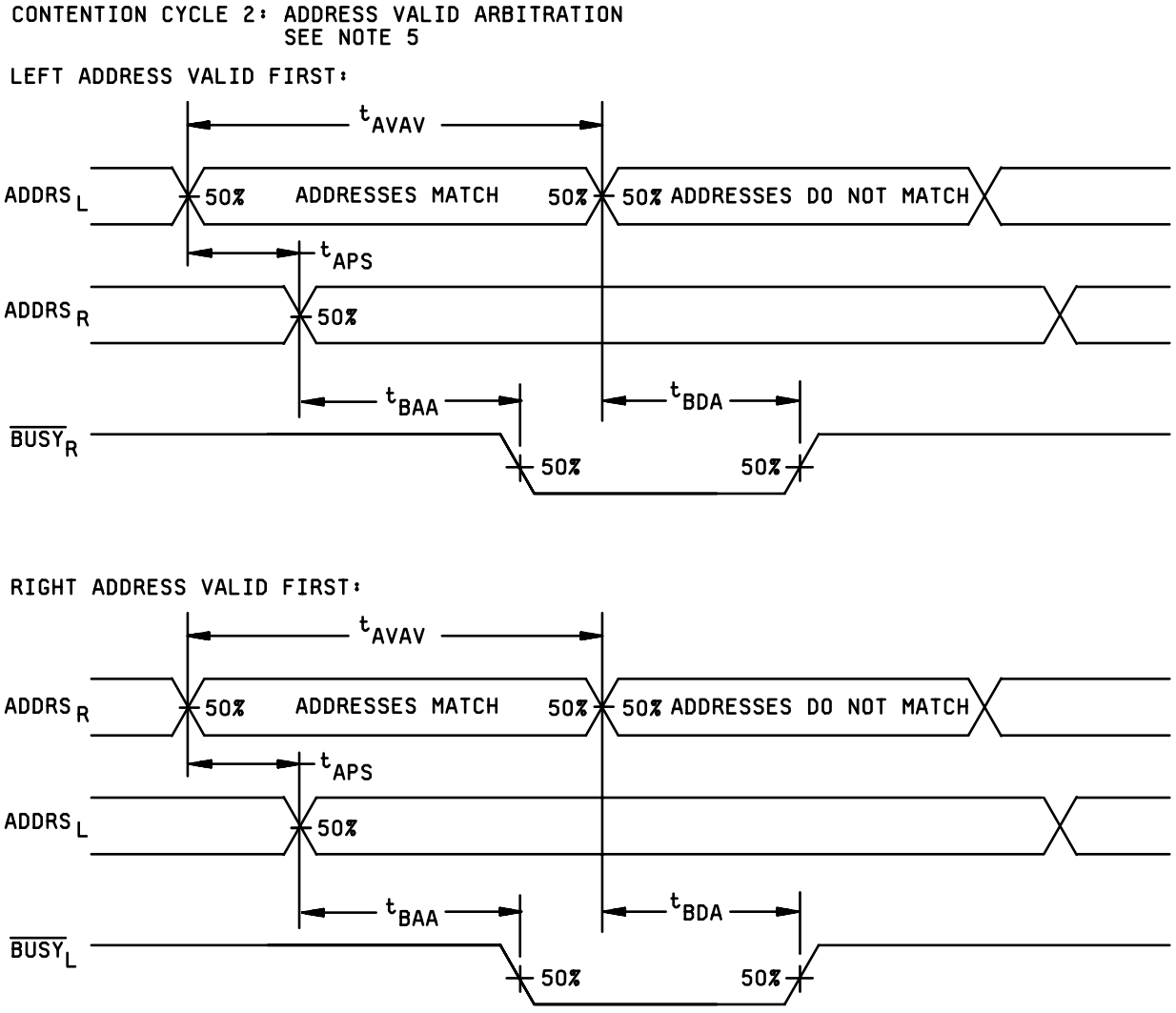


FIGURE 5. Timing waveform diagram - Continued.

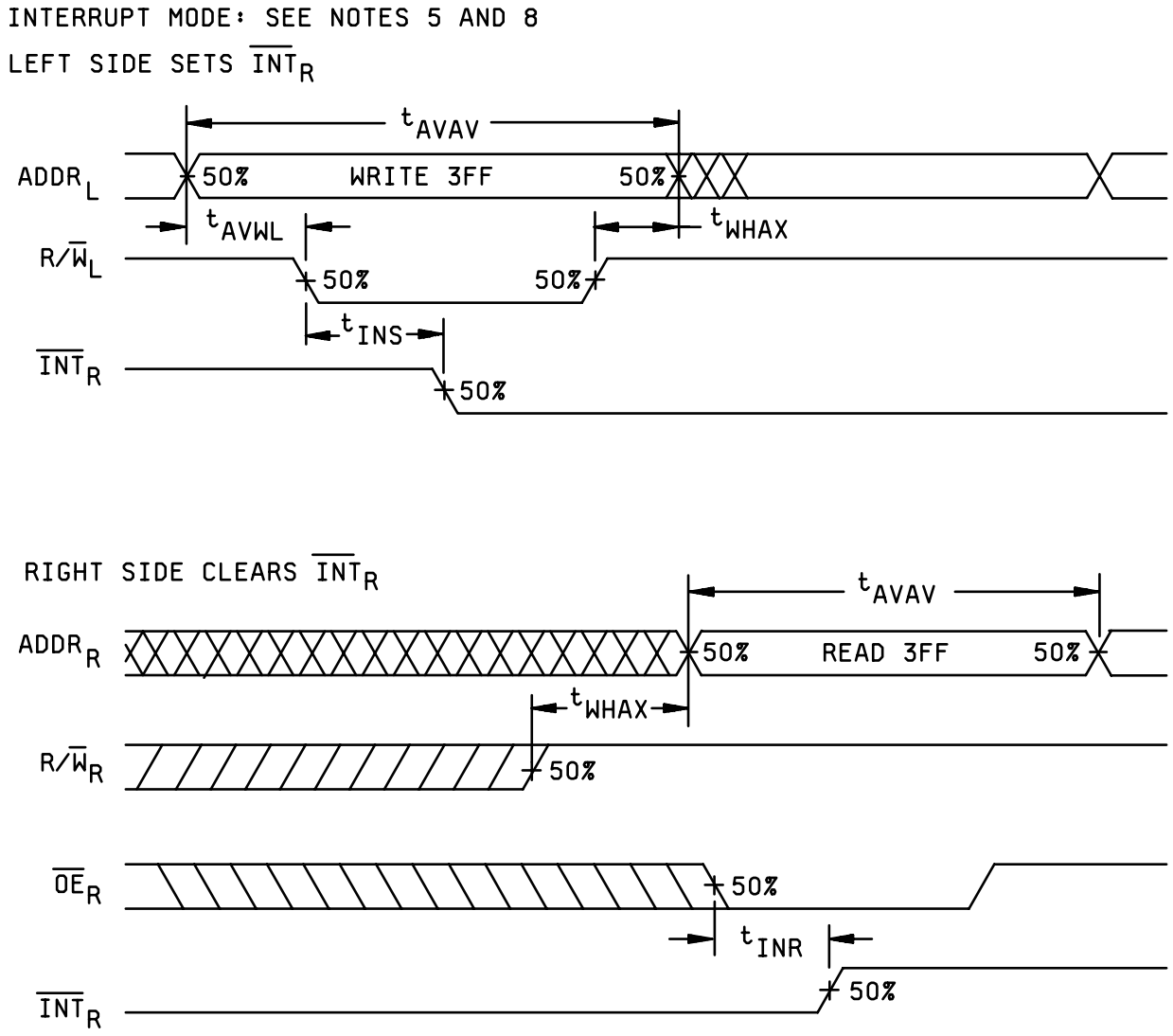


FIGURE 5. Timing waveform diagram - Continued.

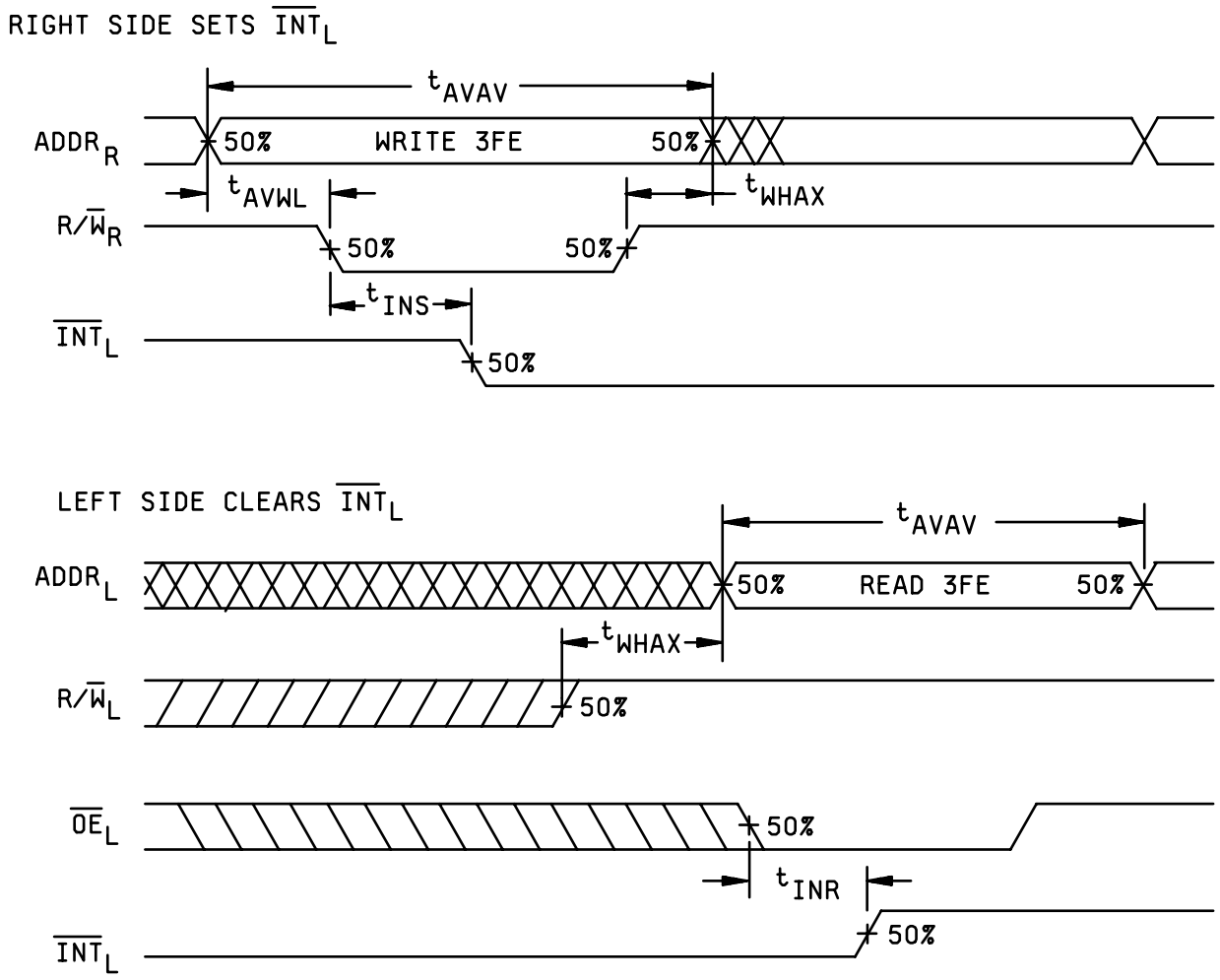
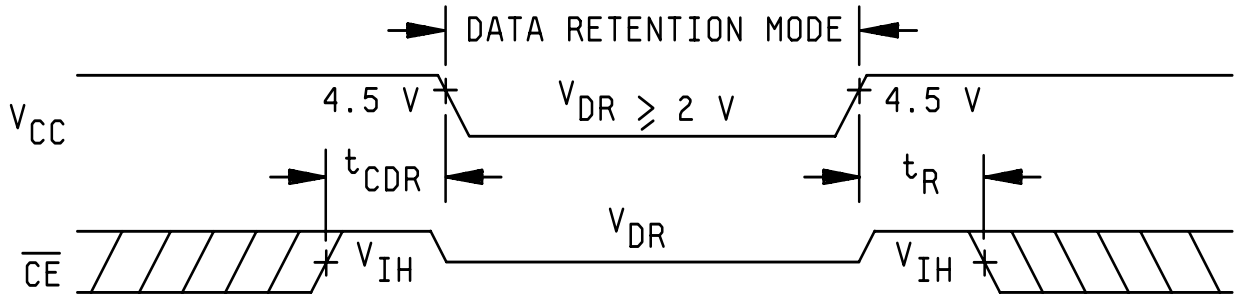


FIGURE 5. Timing waveform diagram - Continued.

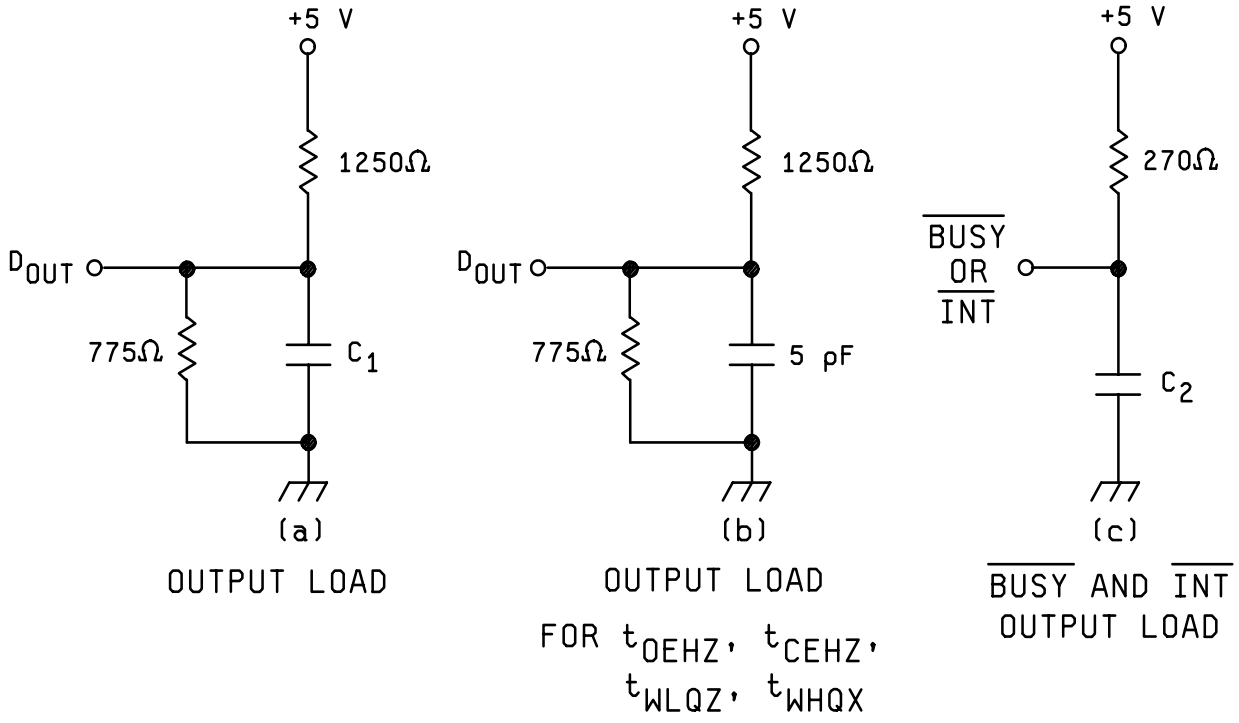
DATA RETENTION WAVEFORM



NOTES:

1. R/$\overline{W}$ is high (logic 1 state) for read cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ transition low (logic 0 state).
4. If $\overline{CE}$ goes high (logic 1 state) simultaneously with R/$\overline{W}$ high (logic 1 state), the outputs remain in the high impedance state.
5. $\overline{CE}_L$ = $\overline{CE}_R$ = V_{IL}.
6. $\overline{OE}$ = V_{IL}.
7. R/$\overline{W}$ = V_{IH} during the address transition.
8. $\overline{INT}_R$ and $\overline{INT}_L$ are reset high (logic 1 state) during power up.

FIGURE 5. Timing waveform diagram - Continued.



NOTES:
1. Tolerances on resistors and capacitors = ±10 percent.
2. Input pulse levels are at GND to 3.0 V.
3. Input rise/fall times are at 5 ns.
4. Input timing reference levels are at 1.5 V.
5. Output reference levels are at 1.5 V.
6. C_1 and C_2 capacitance loads will be 100 pF for all devices, except for device types 04, 08, 12, and 16-22 which will be at 30 pF.

FIGURE 6. Switching times test circuit.

TABLE II. Electrical test requirements. 1/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ Any or all subgroups may be combined when using high speed testers.
* PDA applies to subgroup 1.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen with zero accept and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-08-08

Approved sources of supply for SMD 5962-86875 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8687501UA	61772 0C7V7	IDT7130SA90FB CY7C130-90FMB
5962-8687501XA	61772 0C7V7	IDT7130SA90CB CY7C130-90DMB
5962-8687501YA	61772 0C7V7	IDT7130SA90L48B CY7C130-90LMB
5962-8687501ZA	3/ 0C7V7	IDT7130SA90L52B CY7C131-90LMB
5962-8687502UA	61772 0C7V7	IDT7130SA70FB CY7C130-70FMB
5962-8687502XA	61772 0C7V7	IDT7130SA70CB CY7C130-70DMB
5962-8687502YA	61772 0C7V7	IDT7130SA70L48B CY7C130-70LMB
5962-8687502ZA	3/ 0C7V7	IDT7130SA70L52B CY7C131-70LMB
5962-8687503XA	61772 0C7V7	IDT7130SA55CB CY7C130-55DMB
5962-8687503YA	61772 0C7V7	IDT7130SA55L48B CY7C130-55LMB
5962-8687503ZA	3/ 0C7V7	IDT7130SA55L52B CY7C131-55LMB
5962-8687503UA	61772 0C7V7	IDT7130SA55FB CY7C130-55FMB
5962-8687504XA	61772 0C7V7	IDT7130SA45CB CY7C130-45DMB
5962-8687504YA	61772 0C7V7	IDT7130SA45L48B CY7C130-45LMB
5962-8687504ZA	3/ 0C7V7	IDT7130SA45L52B CY7C131-45LMB
5962-8687504UA	61772 0C7V7	IDT7130SA45FB CY7C130-45FMB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8687505UA	61772	IDT7130LA90FB
5962-8687505XA	61772	IDT7130LA90CB
5962-8687505YA	61772	IDT7130LA90L48B
5962-8687505ZA	3/	IDT7130LA90L52B
5962-8687506UA	61772	IDT7130LA70FB
5962-8687506XA	61772	IDT7130LA70CB
5962-8687506YA	61772	IDT7130LA70L48B
5962-8687506ZA	3/	IDT7130LA70L52B
5962-8687507UA	61772	IDT7130LA55FB
5962-8687507XA	61772	IDT7130LA55CB
5962-8687507YA	61772	IDT7130LA55L48B
5962-8687507ZA	3/	IDT7130LA55L52B
5962-8687508UA	61772	IDT7130LA45FB
5962-8687508XA	61772	IDT7130LA45CB
5962-8687508YA	61772	IDT7130LA45L48B
5962-8687508ZA	3/	IDT7130LA45L52B
5962-8687509UA	61772	IDT7140SA90FB
5962-8687509XA	61772	IDT7140SA90CB
5962-8687509YA	61772	IDT7140SA90L48B
5962-8687509ZA	3/	IDT7140SA90L52B
5962-8687510UA	61772	IDT7140SA70FB
5962-8687510XA	61772	IDT7140SA70CB
5962-8687510YA	61772	IDT7140SA70L48B
5962-8687510ZA	3/	IDT7140SA70L52B
5962-8687511XA	61772 3/	IDT7140SA55CB CY7C140-55DMB
5962-8687511YA	61772 3/	IDT7140SA55L48B CY7C140-55LMB
5962-8687511ZA	3/ 3/	IDT7140SA55L52B CY7C141-55LMB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8687511UA	61772 3/	IDT7140SA55FB CY7C140-55FMB
5962-8687512XA	61772 3/	IDT7140SA45CB CY7C140-45DMB
5962-8687512YA	61772 3/	IDT7140SA45L48B CY7C140-45LMB
5962-8687512ZA	3/ 3/	IDT7140SA45L52B CY7C141-45LMB
5962-8687512UA	61772 3/	IDT7140SA45FB CY7C140-45FMB
5962-8687513UA	61772	IDT7140LA90FB
5962-8687513XA	61772	IDT7140LA90CB
5962-8687513YA	61772	IDT7140LA90L48B
5962-8687513ZA	3/	IDT7140LA90L52B
5962-8687514UA	61772	IDT7140LA70FB
5962-8687514XA	61772	IDT7140LA70CB
5962-8687514YA	61772	IDT7140LA70L48B
5962-8687514ZA	3/	IDT7140LA70L52B
5962-8687515UA	61772	IDT7140LA55FB
5962-8687515XA	61772	IDT7140LA55CB
5962-8687515YA	61772	IDT7140LA55L48B
5962-8687515ZA	3/	IDT7140LA55L52B
5962-8687516UA	61772	IDT7140LA45FB
5962-8687516XA	61772	IDT7140LA45CB
5962-8687516YA	61772	IDT7140LA45L48B
5962-8687516ZA	3/	IDT7140LA45L52B
5962-8687517UA	3/	IDT7130-LA-35CB
5962-8687517XA	3/	CY7C130-35DMB
5962-8687517YA	3/	CY7C130-35LMB
5962-8687517ZA	3/	CY7C131-35LMB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8687518UA	3/	IDT7140-LA-35CB
5962-8687518XA	3/	CY7C140-35DMB
5962-8687518YA	3/	CY7C140-35LMB
5962-8687518ZA	3/	CY7C141-35LMB
5962-8687519UA	0C7V7	CY7C130-35FMB
5962-8687519XA	0C7V7	CY7C130-35DMB
5962-8687519YA	0C7V7	CY7C130-35LMB
5962-8687519ZA	0C7V7	CY7C131-35LMB
5962-8687520UA	3/	CY7C140-35FMB
5962-8687520XA	3/	CY7C140-35DMB
5962-8687520YA	3/	CY7C140-35LMB
5962-8687520ZA	3/	CY7C141-35LMB
5962-8687521UA	61772	IDT7130LA35FB
5962-8687521XA	61772	IDT7130LA35CB
5962-8687521YA	61772	IDT7130LA35L48B
5962-8687521ZA	3/	IDT7130LA35L52B
5962-8687522UA	61772	IDT7140LA35FB
5962-8687522XA	61772	IDT7140LA35CB
5962-8687522YA	61772	IDT7140LA35L48B
5962-8687522ZA	3/	IDT7140LA35L52B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
61772	Integrated Device Technology, Inc. 2975 Stender Way Santa Clara, CA 95054
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

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